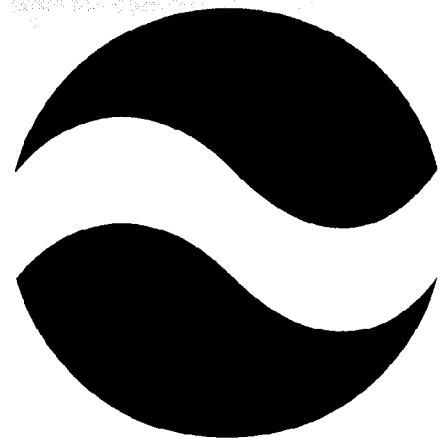


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SURFACE MOUNT COUNCIL WHITE PAPER

Chip Mounting
Technology
(CMT)



**SURFACE MOUNT COUNCIL
WHITE PAPER - STATUS OF THE TECHNOLOGY
CHIP MOUNTING TECHNOLOGY**

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ABSTRACT

This Chip Mounting Technology (CMT) white paper is a status of the technology on various methodologies for mounting and interconnecting bare (unpackaged) active devices to various substrate materials. A review will be conducted of the currently available mounting techniques for Tape Automated Bonding, Wire Bonding, and Flip Chip, followed by an examination of the most commonly used substrate options of laminate, ceramic, and silicon. This paper, which represents the position of the Surface Mount Council, is being presented to describe the emerging integrated circuit chip mounting techniques that are emerging on the technology time horizon.

INTRODUCTION

The purpose of this paper is to investigate emerging chip attachment methods and define and classify the attachment methods for electronic systems designers and manufacturers today. The industry is on the threshold of the next generation of electronic packaging as the component density limitations of fine pitch technology are approached. Chip Mounting Technology is appearing on the technology horizon as a viable option to higher system densities. The name "Chip Mounting Technology" (CMT) was selected in keeping with the conventions of Through Hole Technology (THT), Surface Mount Technology (SMT), and Fine Pitch Technology (FPT). Throughout the paper, the terms "chip" and "device" will be used interchangeably to describe the integrated circuit die.

In the past decade, active device packaging has evolved from Through Hole Technology, with component leads on 2.54mm [.100"] centers, to Surface Mount Technology with leads on 1.27mm [.050"] and smaller centers. This has recently been followed by the evolution of Fine Pitch Technology with component leads on 0.63mm [.025"] and 0.5mm [.020"]. Through these evolutions the component package which contains the silicon die, or chip, has decreased in size while lead counts have increased dramatically. The reduction in die geometries has been the result of semiconductor technology improvements, particularly lithography. The package size reduction has been made possible by improvements in assembly capabilities. Through each evolutionary reduction in package size, component density on the various substrates has increased dramatically. The next evolution will call for simply removing the package, mounting the device to the substrate, and then making the interconnections to the substrate.

We recognize that there are some advanced electronics companies who have been practicing these "new" packaging concepts for years. If it were not for their pioneering efforts, technology would come to a standstill. The objective of this paper is to simply describe, and help bring the results of those innovative packaging efforts into the mainstream of electronic package design and manufacturing.

PACKAGING EVOLUTIONS

CMT as the next generation of

electronic packaging technology is a logical sequel to the series of evolutions of component attachment methods. Electronic packaging began in the 1950's and has evolved through the following technologies to position the industry where it is today:

- Through Hole Technology (THT)
- Surface Mount Technology (SMT)
- Fine Pitch Technology (FPT)
- Tape Automated Bonding (TAB)
- Chip Mounting Technology (CMT)
- Next?

CMT will likely take the industry through the remainder of this decade and into the year 2000.

PACKAGING DRIVERS AND LIMITATIONS

The decision to use Chip Mounting Technology, the next generation of electronics packaging density, is driven by a number of factors. The following list, while not all inclusive, represents the major drivers. They are not ranked in any particular order of importance:

- Higher system operating frequencies
- Higher system packaging densities
- Increased input/output requirements
- Smaller lead pitches on devices
- Higher thermal loads and power dissipation
- Overall system size reductions

The incorporation of CMT does have some limitations which must be considered:

- Acquisition of 100% known good die
- Bare IC die handling
- Specialized assembly equipment Required
- Chip encapsulation and metallurgy
- Manufacturing yields
- Advanced CAD tools required

PACKAGING DRIVERS

HIGHER FREQUENCY

Advantages: One of the primary advantages of CMT in high frequency applications is the reduction of the distance between components. This translates directly to reduced signal propagation time in the system. In Figure 1 it can be seen

that the interconnection between devices is a significant contribution (often over 50%) to system delays. When interconnect delays are reduced, overall system performance in terms of speed and noise reduction is greatly improved. As operating frequencies approach 100MHz, and device rise times shrink to 1 nanosecond and less, it will become necessary to reduce wiring delays.

Disadvantages: None.

HIGHER SYSTEM DENSITY

Advantages: CMT allows a significantly greater number of components or electrical functions to fit in a given space than Surface Mount or Fine Pitch technology. The benefit is a smaller system, or more functions in the same size system. The high density packaging afforded by CMT is also much lighter in weight, should weight be a consideration. Fundamentally, higher system densities result in lower system delays because chip-to-chip distances are reduced.

Disadvantages: This packaging technology may be very difficult or impossible to repair or rework after assembly and test. Therefore many assemblies employing CMT may tend to be modular and disposable in the event of a failure.

INCREASED I/O COUNTS

Advantages: Another obvious advantage of CMT is that the high Input/Output requirements of large chips can be handled with a relative amount of ease through the high density interconnection strategies described in this paper. There is no package level of interconnect available that would require the small I/O pitch of the chip itself to be brought out to the comparatively large lead pitch typically found on a Surface Mount package. Therefore, the maximum I/O counts of chips destined for CMT could be much greater than, for example, those destined for Fine Pitch packages.

Disadvantages: The higher interconnect density will drive substrate geometries down and layer

counts up, both of which make high yield manufacturing more difficult.

SMALLER LEAD PITCHES

Advantages: Most logic device packages with high I/O counts are available in Fine Pitch packages with lead pitches as stated above. In the package geometry trends in Table 1, we see device pitch decreasing over time, forcing substrate geometries down accordingly. Through these decreases, the component packing density can be increased on the substrate in terms of connections per square inch or per square centimeter. The budgetary component density calculations in Table 2 can assist in the decision making process by predicting whether or not the components will fit within the given substrate real estate area. There is a decision point at 160 connections per square inch, or greater, where the design engineer will leave the realm of SMT and cross over into CMT.

There is also a method of calculating the routing density according to Rent's Rule. This method uses a total number of routing channels available per square inch or centimeter and is driven by conductor width and spacing. Smaller geometries will produce greater routing densities. Table 3 and Table 4 list routing density in inches of wire per square inch of substrate.

Currently, the lower lead spacing threshold, or practical limit, is at approximately 0.5mm [.020"] pitch for most SMT packaged devices. A definite advantage of CMT is the ability to cross that threshold into smaller pitches in the range of 0.25mm [.010"] to 0.5mm [.020"] by removing the package and it's limitations.

Disadvantages: The smallest pitch that can be practically utilized is limited by the substrate choice. For example: PCB or ceramic substrates are limited to device pitches greater than 0.25mm [.010"] (0.13mm [.005"] bonding sites on 0.25mm

[.010"] centers), while semiconductor substrates work well with pitches less than 0.5mm [.010"].

HIGHER HEAT GENERATION

Advantages: None.

Disadvantages: CMT is ushering in a whole new dimension of thermal management problems. Thermal requirements must now be thoroughly evaluated very early in the design process, prior to beginning any physical layout efforts.

SIZE

Advantages: The overall substrate level package size can be reduced by 50%, or more, over those using Fine Pitch Surface Mount devices.

Disadvantages: Design, fabrication, assembly, and test becomes significantly more challenging in every aspect with smaller, denser packaging.

CMT MOUNTING METHODS & SUBSTRATE TYPES

CMT MOUNTING METHODS

There are three basic mounting methods within CMT as shown in Figure 2: Tape Automated Bonding (TAB), Wire Bonding (WB), and Flip Chip. Within each of the mounting methods there are several methods which will be described later in the text.

SUBSTRATE TYPES

There are three basic types of substrates that could be used for the different CMT mounting methods. They are MCM-C, MCM-D, and MCM-L. As the different CMT methods are explored, the optimum substrate choices will be recommended. For purposes of this discussion, it is assumed that, by definition, a substrate is termed a Multichip Module whenever bare, or unpackaged, chips are directly attached and interconnected to it.

SUBSTRATE TYPES

MCM TECHNOLOGIES DEFINED

There are three types of Multichip Modules in use today according to

the Institute for Interconnecting and Packaging Electronic Circuits (IPC). They are identified by acronym-letter suffix as follows: MCM-C, MCM-D, and MCM-L. The letter designates the substrate material and it's associated fabrication process.

MCM-C: CERAMIC COFIRE SUBSTRATE

The construction of this substrate is of ceramic or glass ceramic alternatives that have a relatively high dielectric constant greater than 5.0. Conductors with line widths of 0.13mm [.005"] and larger are built up using layers of fired metals. The via interconnections between layers are built up at the same time as the conductors. Resistors may be cofired on the outer layer and laser trimmed to a precise value as the last step. All conductors and resistors are screened onto the substrate.

MCM-D: DEPOSITED THIN FILM SUBSTRATE

This process is similar to that of integrated circuit fabrication except the substrate is large enough to contain several bare die. The base substrate is usually silicon with conductors between 1 micron and 1 mil wide, and vias built up with various suitable metals by vacuum deposition. The dielectric constant is generally less than 3.4.

MCM-L: LAMINATED ORGANIC SUBSTRATE

This is constructed using the common printed board materials and sequential lamination substrate fabrication processes. Line geometries of 0.08mm [.003"] or greater are typically created with copper using the print andetch, or subtractive, method. Blind, buried, and through vias are drilled and plated, also with copper, making connections with various inner layers by design. This type of substrate will typically have higher layer counts of 10 - 50+ layers as needed to complete all of the interconnections. In addition, restraining layers may be incorporated in the layer stackup to control X-Y expansion for Flip Chip applications.

Following substrate fabrication, the integrated circuits may be attached or mounted to the above MCM's by TAB, Wire Bonded, or Flip Chip assembly processes as described later in this paper.

DESIGN FOR MANUFACTURABILITY

DFM VS YIELDS

Design has a much greater influence on the manufacturability of a CMT assembly than on that of a surface mount assembly due to the significant reduction in geometries. All design efforts should take place in a Concurrent Engineering framework with yield optimization as a primary objective. The Concurrent Engineering team should be able to provide the designer with important information on process limitations specific to their fabrication or assembly operation, thus minimizing the risk associated with most emerging technologies. For example, the following design suggestions for MCM-L (printed circuit) substrates may help eliminate some common CMT manufacturing problems:

1. Define end product requirements prior to committing to any design efforts
2. Reassess overall corporate printed circuit board specifications in light of CMT
3. Determine which type of interconnection will be used as this will determine the substrate choice
4. Review all multilayer designs to see if the padcap architecture (pads only on outer layers) would make sense because fine lines can be produced with higher yields on inner layers
5. Make minimum sized features as large as possible
6. Employ grid based design rules to enhance testability
7. Utilize buried and blind vias to reduce high aspect ratio hole drilling and plating through the board
8. Utilize balanced construction from the center of a multilayer substrate out to the surface

layers to promote flatness
9. Provide uniform copper density on the outer layers to promote feature size and thickness control

There are also design rules for ceramic co-fired and thin film substrates.

Continuous process improvements must be implemented throughout the manufacturing process to maintain acceptable yields. This should be accomplished through the joint efforts of designers and manufacturers as they conduct frequent design reviews.

THE MANUFACTURING PROCESS

PROCESS OVERVIEW

The manufacturing processes for TAB, Wire Bonding, and Flip Chip begin after the substrate of choice has been fabricated. Fabrication process details have been intentionally omitted since they are not within the scope of the document. The basic manufacturing process steps are as follows:

- Substrate Fabrication
- Substrate Assembly
- Manufacturing Defects Analysis
- Burn-in & Functional test
- Device Encapsulation

The process details will be defined in the respective CMT categories later in this paper.

CHIP CONSIDERATIONS

INTEGRATED CIRCUITS

The layout of IC chips used for CMT are usually in the same relative form as those packaged in DIP or SMT packages. The chips are simply left unpackaged if they are destined for CMT. Either gold or aluminum chip metallization may be used, with gold or nickel or, in the case of TAB, even solder or conductive polymer on the substrate. The only requirement is that the metallization on the chip be compatible with the substrate for the type of interconnection to be used.

CHIP MOUNTING TECHNOLOGIES

TAPE AUTOMATED BONDING (TAB)

There are basically two types of chips used for TAB or other TAB type lead bonding. Bumped chip bonding requires input/output (I/O) pads plated with gold bumps that will allow the inner lead bonding of TAB tapes, or circuitized TAB to the chip. Alternatively, bumped leads may be used, and the chip can then be identical to those used for wire bonding.

In the bumped chip method, bumps must be applied to the chip by evaporation/deposition. This must be accomplished prior to the dicing of the wafer. Bump application, therefore, is often done at the chip manufacturers location, although some vendors offer chip bumping service along with inner lead bonding. The structure of a typical chip bump is shown in Figure 3.

TAB ADVANTAGES

TAB has some advantages which will benefit users. An IC destined for TAB attach can be tested by the assembler after inner lead bonding, but prior to mounting on the substrate. Bare chips or chips intended for Wire Bonding currently cannot be tested by the assembler prior to assembly, however, much work is being done in this area and solutions should be forthcoming in the next year or two. The TAB package is likely to be the easiest to rework of the three methods which could be useful during prototyping or field service including repair and replacement.

TAB also eliminates the need for gold plating on the substrate since the outer lead bonding normally takes place through soldering. Two mass bonding or soldering methods available for TAB are hot bar or hot gas soldering. The hot bar forces the leads down into the solder and may not make a smooth fillet. Hot gas reflows the solder on the substrate then gently lowers the device leads into the molten solder forming a solder joint with smooth

fillets. There are also different methods for soldering TAB leads individually: laser, focused IR, and single point thermocompression bonding.

When completed, the TAB assembly has advantages over wire bonding including low bond profiles and more compliant leads which enhance long term reliability.

TAB CONSTRAINTS

Historically, TAB lead frames have been costly to develop which made them prohibitively expensive for low volume applications. The lead frames for connection to the chips required application specific designs which prevented them from being used in different applications. This has contributed to the high initial cost associated with TAB. The equipment used to assemble TAB components is less flexible than the equipment used in wire bonding due to the specific tooling requirements. Finally, from a high performance perspective, the TAB leads have higher resistance and lead inductance than wire bond leads.

TAB DESIGN

When designing for TAB CMT application, the method of outer lead bonding is critical to the surface finish applied to the substrate bonding pads. If the outer leads are to be attached with solder, then a solderable coating is required. If it is to be attached by thermocompression, soft gold is required.

Finally, if it is to be outer-lead bonded using one of the newer anisotropic adhesives, a hard gold contact-type finish is desirable and should be readily available. However, if the board is a larger one, care should be taken to ensure that the printed circuit board manufacturer has the capability of selectively plating the entire board with gold, as some manufacturers equipment will not allow gold plating of large areas.

TAB MANUFACTURING

TAB is an assembly technology for connecting semiconductor devices to substrates. Basically, the process uses a specially plated tape etched in the desired conductor pattern. The tape may be single, two, or three layer construction. The conductors are etched into the pattern and are unsupported in the center area where the semiconductor chip is to be attached. TAB accomplishes this by means of a photo-imaged and etched pattern of conductors bonded to a dielectric tape. This carrier tape, which is usually stored on reels similar to movie film in widths from 8 to 70 mm, is commonly made from mylar or polyimide material. Windows are punched at specific locations in the tape and a thin, copper conductive foil is bonded to the tape. A conductor pattern of leads is etched in the foil, thus giving the desired interconnection circuitry with beam-type leads that extend over the window in the tape. Gold bumps are typically formed on either the tape or the chip itself. The IC is aligned on the tape and thermocompression bonded to the inner leads of the tape. The outer leads bonding operation transfers the chip with its leads to the substrate.

INNER LEAD BONDING

Inner lead bonding can be used to simultaneously bond all the leads on a TAB tape to the chip. The leads are optically aligned to the chip. Positioning for this alignment is controlled by specially etched holes previously fabricated in the tape. The lead bonding process is usually a high speed solder or thermocompression bonding technique. The solder process uses immersion tin plated leads and gold bumps on the chip to form a gold/tin eutectic. This method uses a relatively low bonding temperature (284 C) and low bonding pressure (75 grams per lead). Thermocompression bonding uses gold plated leads to join to gold bumps. A typical thermocompression cycle includes preheating the chip (200 C) prior to gang bonding the leads

(approximately 375 C, 2.5 seconds, 200 grams per lead).

BUMPED CHIPS

Bumped chips are chips on which raised gold bumps have been fabricated on the pad areas. This operation seals the pads and provides some protection. The gold bumps are malleable enough to compensate for any non-planarity during inner lead bonding. Bumped chips are more reliable than regular chips, but require extra processing steps and, hence, are more expensive.

At this point, a chip slated for TAB can be processed in one of two ways. Early in the development (of TAB), practitioners learned that reliable bonds could not be obtained unless "bumps" were added to the TAB leads or to the wafer pad area in order to obtain a planar surface. In the basic TAB approach, a barrier metal such as titanium-tungsten is deposited over the passivation on the pad as shown in Figure 3. This plus the addition of 0.025mm [.001"] high gold bumps, helps insure the reliability of the TAB connections to the tape during the inner-lead-bonding process.

The bumps on the chip are evaporated or electroplated onto the barrier metal at each pad position. Copper bumps can also be used, and both copper and gold can be tin plated. This completely seals the chip, and further enhances TAB's reliability as a CMT assembly process.

BUMPED TAPE AUTOMATED BONDING (BTAB)

Another processing approach, puts the bump on the tape rather than on the chip in Figure 4. This approach is known as BTAB. Bumped tape is TAB tape with a copper projection at the end of the lead. The bump is usually gold or immersion tin plated for inner lead bonding. The bump is formed by selective etching of a thick copper foil. This method of tape fabrication is limited to a single layer (copper foil) construction.

In both bumped chip and bumped tape, the bumps elevate the etched tape conductors above the chip to prevent shorting of the leads as well as to provide access to the bonding plane. The bumping process eliminates the need for forming the inner leads of the TAB tape prior to bonding.

OUTER LEAD BONDING (OLB)

The outer lead bonding process connects the chip with its leads to the substrate. OLB is a two step process usually performed sequentially on the component placement machine. The first step is to excise the chip with its leads from the TAB tape and form the leads. A vision system is required for precise alignment of the outer leads to the bonding pads. This is accomplished by referencing the lead pattern and then referencing a fiducial on the substrate. The outer lead bonding process may be completed by thermocompression bonding, reflow solder, or conductive adhesive technology.

WIRE BONDING

The limited availability of bare integrated circuit chips has impeded the use of Wire Bonding technology. Many potential Wire Bond designs have been done using the more expensive packaged device approach because only packaged devices were available. However, as Wire Bond technology gains acceptance as a less expensive and perhaps the only technology which will meet certain physical design requirements. Chip fabricators and assembly houses will form alliances to bring this technology to the market.

WIRE BONDING ADVANTAGES

Electrical interconnections from the device to the board are critical in Wire Bonding manufacturing and long term reliability. The traditional dominance of wire bonding is explained by its advantages over competing technologies:

- Adaptability to diverse metallizations
- Amenability to visual inspection

- Easily performed bond integrity tests
- History of satisfactory reliability
- Extensive base of expertise and equipment
- Relatively inexpensive for prototyping & low volumes

Another advantage of wire bonding is that it can be used in some cases to prototype a circuit designed for TAB prior to investing in a lead frame. Once a circuit is debugged and is operating satisfactorily, a TAB lead frame can be developed and implemented without changing the chip and substrate design.

WIRE BONDING CONSTRAINTS

Wire bonding has fewer constraints than the other CMT mounting methods because it has been established many years. There are, however some constraints that should be listed:

- Substrate interconnections must be made one at a time
- Impedance control is not precise
- Encapsulation is mandatory
- Localized heating must be avoided on laminate substrates
- Selective deep gold plating required on substrates

WIRE BOND DESIGN

Chip areas for die and Wire Bonding substrates should follow guidelines for bond length and angles as shown in Figures 5 and 6. The suggested limits on these features appear in Table 5.

In order to obtain a design for a wire bonded structure that is manufacturable, the type of wire bonding process to be used must be considered a critical factor.

When thermocompression (TC) bonding must be used, the gold plating requirements are similar to those needed for thermosonic bonding. However, selection of the substrate is critical, because organic substrates cannot withstand the high bonding temperatures required.

With thermosonic bonding (TS), some high Tg organics, such as 150C BT epoxy and 260C polyimide, may be

processed. Substrate plating materials and thickness should be 40-50 microinches of soft gold plated over 50-200 microinches of nickel.

If ultrasonic bonding (usually with aluminum wire bonded at room temperature) is to be used, the substrate can be any accepted circuit material, with 5-15 microinches of soft gold plated over 50-200 microinches of nickel.

Whichever style of wire bonding is chosen for these designs, guidelines for the layout of the chip area on the substrate are process dependent and will require verification for each application.

WIRE BOND MANUFACTURING

When shipping bare, unprotected IC chips, one must choose the form in which the chips are transported from silicon fabricator to assembler. With TAB, this form is tape, but with the chip and wire technique, there is a choice of methods: Waffle packs, Wafer form, or chip-in-tape. Automatic pick-and-place systems for chip placement can usually accept dice either in waffle packs or in diced wafer form. In the case of the wafer, defective chips are indicated by the presence of an ink dot placed on each bad chip when tested at the manufacturer in wafer form, or they can have a "wafer map", a paper or software record of defective chip locations on the wafer.

At the assembly site, the chips are picked up by a pick-and-place machine and placed at a bond site on the substrate. The chips must be placed precisely in X-Y, rotational, and Z axes.

Thus, the technology used to make the IC chips for Wire Bonding is less of a concern than the method of shipment. When the chip manufacturer and the substrate assembler are the same, there is no problem. If they are different organizations, a close user-vendor relationship must exist.

Chip attach adhesives are various

bonding agents, listed in Table 6, that are used to bond bare chips to the substrate. Thermoset, one part, thermally and electrically conductive epoxies, are most popular. An alternative to one-part systems is a two-part system which is cured at room or slightly elevated temperature. Once mixed, the two-part epoxy has limited life and must be used quickly. As with other mounting processes, epoxy bonding involves trade-offs. Certain precautions must be taken:

- There are many types of conductive epoxies. Epoxies used for Wire Bonding must be low in ionic contaminants, low in outgassing and formulated for this purpose
- When thermocompression wire bonding a chip, use a bonder with a heated probe tip since the heat associated with some other types of thermocompression wire bonding will soften the epoxy
- Some semiconductor chips have gold backing in order to alloy the gold with the silicon. If the gold is vapor deposited, epoxy can pull it away from the chip and form a high resistance contact

In summary the advantages for using epoxy adhesives include:

- Low temperature cure
- Ease of processing
- Ease of handling
- Ease of repair
- High yield ruggedness
- Bond compliancy

Bonding wire for microelectronics assembly is a precision metallurgical product developed for the semiconductor industry. In order for a device packaging line to operate effectively, the yield of acceptable wire bonds must approach 6 Sigma quality levels. This places stringent quality standards on the wire. In addition, semiconductor manufacturers seek to maximize yields by optimizing wire to their particular chip metallizations, package constructions, and bonding machine configurations; therefore, there is no "standard" bonding wire. Some available bonding wire

diameters are shown in Table 7. Furthermore, the wire from one wire manufacturer is not necessarily interchangeable with that from another. Bonding wire is a highly specialized product made by relatively few producers, each of whom employs guarded proprietary processes.

Despite the maturity of the wire bonding process, it is by no means static. Improvements are continuously being made in all of the variables including the wire, the bonding surfaces, the equipment, and especially the bonding processes themselves. Figure 7 shows a number of bonding variables.

There are three well developed methods for making wire connections: Ultrasonic bonding, thermocompression bonding, and thermosonic bonding as shown in Table 8. THERMOCOMPRESSION (TC) bonding is accomplished by pressing gold wire against the bond site metallization at an elevated temperature. Because of the high temperatures, organic based substrates are not used with this process. ULTRASONIC bonding uses ultrasonic energy to weld wire to the chip pad and circuit pad. The process takes place at room temperature. Aluminum wire is used almost exclusively for ultrasonic bonding, though gold and copper wires have been used successfully. THERMOSONIC (TS) bonding combines the principle features found in ultrasonic and thermocompression bonding. Thermosonic bonding temperatures are lower than in thermocompression bonding. Thermosonic bonding has been particularly successful in attaching wires to hard-to-bond thick film hybrid substrates.

FLIP CHIP

Flip-chip technology avoids conventional chip bonding. No adhesive is used, because the semiconductor chip is "flipped-over" such that its conductive pattern contacts the conductive circuitry of

the substrate. Therefore, the equivalent of chip attach and wire bonding are accomplished in one operation.

FLIP CHIP ADVANTAGES

Flip chip interconnection technique requires a specialized body of knowledge related to solders, their deposition, and the reflow process. However, the use of this technology will be driven by the many advantages of this chip mounting technique which include:

- Efficient use of substrate area
- Shortest interconnect path between devices
- All connections are made simultaneously
- Most dense interconnect method available
- Area array interconnection possible
- Very low device profile
- Fast manufacturing throughput times
- Reworkability is simplified
- Has been in use for over 10 years

The primary advantage of the Flip Chip option is that it provides the highest density of all CMT methods because it requires no additional interconnection scheme.

FLIP CHIP CONSTRAINTS

This method of CMT is the least understood of all the CMT mounting methods. As a result, there are many constraints which must be researched and optimized before Flip Chip can be utilized effectively. Among the constraints are:

- Limited availability of bumped chips
- Requires precise alignment
- Requires matched TCE or SLC encapsulation
- Difficult or impossible to inspect
- Requires precise solder volume
- Cleaning under chip difficult
- Area array design rules must be employed

One solution to the availability problem is to produce the bump as a part of the interconnecting substrate, rather than as a part of the chip. The CMT assembler can then use any device available in bare

chip form without bumps.

A major constraint of the flip chip technique is its limited heat transfer and dissipation. Since the chip is joined to the substrate only by the solder joint interconnection, rather than the entire back side of the chip, there is limited area for heat conduction into the substrate. One remedy is to incorporate non-functional thermal pads onto the silicon chip in presently unused connection areas. These pads would mate with heat sinking pads on the substrate, which could then connect to thermal vias in the substrate.

FLIP CHIP DESIGN

Flip chip or face bonding interconnection technique requires an interconnection substrate capable of very small geometries.

In this technique, multiple plating operations deposit a specific thickness of a given tin-lead composition onto the semiconductor device's interconnection pads, which are typically 0.1mm - 0.25mm [.004" - .010"] square. Matching pads are imaged onto the substrate and are also plated with a solderable surface, i.e. copper (coated with an anti-oxidant), tin-lead, tin or gold. It must be pointed out that the fine pitch of the I/O pads on an IC chip is very difficult to fabricate on the surface layers of a printed circuit (laminate) board substrate. The chip is subsequently "flipped" to mate with the respective pads or "bumps", which are joined during a solder reflow process, thereby completing the connections simultaneously. If gold is used as the metallization on the substrate, keep it very thin (3-10 microinches) in order to provide as much solder volume as possible, and limit the formation of brittle gold-tin intermetallic alloy. If bare copper is the substrate metallization, it may be desirable to coat the pads with molten solder by a solder leveling process in order to improve solderability and increase the volume of solder for a more ductile and forgiving joint;