



3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249

IPC-TM-650 TEST METHODS MANUAL

1 Scope

This test method provides a means to assess the propensity for conductive anodic filament (CAF) growth, a form of electrochemical migration, and similar conductive filament formation (CFF) laminate material failure modes within a printed wiring board (PWB). Conductive anodic filaments may be composed of conductive salts, rather than cationic metal ions, however inadequate dielectric for the applied voltage, component failures, and part use exceeding the maximum operating temperature (MOT) of the laminate can contribute to product failures as well. This test method can be used to assess PWB laminate materials, PWB design and application parameters, PWB manufacturing process changes and press-fit connector applications.

2 Applicable Documents

2.1 IPC

IPC-9253 CAF Test Board Design (Available in the “Drafts” section of the 5-32e Task Group Home Page)

IPC-9254 CAF Test Board Design (Available in the “Drafts” section of the 5-32e Task Group Home Page)

IPC-9255 CAF Test Board Design (Available in Free Downloads in IPC Home Page)

IPC-9256 CAF Test Board Design (Available in Free Downloads in IPC Home Page)

IPC-9691 CAF Test Method User Guide for the IPC-TM-650, Method 2.6.25

IPC J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC J-STD-004 Requirements for Soldering Fluxes

IPC J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

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2.3.25 Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract

2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

Number 2.6.25	
Subject Conductive Anodic Filament (CAF) Resistance Test: X-Y Axis	
Date 05/12	Revision A
Originating Task Group Electrochemical Migration Task Group (5-32e)	

2.2 American Society for Testing and Materials (ASTM)

ASTM D-257 Standard Test Methods for DC Resistance or Conductance of Insulating Materials

3 Test Specimens

The IPC-9254 CAF test board design is the older coupon and has been superseded by the IPC-9253. The new smaller CAF test coupons are IPC-9255 and IPC-9256 and are used for evaluating PTH-PTH spacings only. These smaller CAF test coupons allow users to put a CAF test coupon at the perimeter of their panels for testing. All IPC CAF test coupon design Gerber files are downloadable and are available on the IPC committee and free download web sites.

3.1 CAF Test Board Designs The IPC-9253 and IPC-9254 have 10 layers and dimensions are approximately 125x175 mm [nominally 5x7 in]. Test board designs for evaluating CAF resistance **shall** have varying drilled hole wall to drilled hole wall distances for plated holes. These distances can range from as low as 0.15 mm [0.00591 in] separation for alternate laminate materials expected to have very high CAF resistance and minimal copper wicking out from the plated-through hole (PTH), to as high as 0.89 mm [0.0350 in] separation for evaluating press-fit connector applications. The drilled hole size, rather than the finished hole size, is specified in the chart on the bare board fabrication drawing to ensure consistent spacing. Internal layer thieving may be added to plane layers around the perimeter. Test boards should be manufactured so that the machine/grain direction of the woven fiber reinforcement is perpendicular to the rows of same-net daisy chain vias for A1-A4 (machine/grain direction tends to fail first). Test board designs **shall** have sufficient minimum spacings on outer layers to ensure that surface insulation resistance failures do not occur. Layouts of the IPC-9253 and IPC-9254 test board structures (CAF Test Boards) are shown in Figure 1.

IPC-9253 and IPC-9254 Test Structures A1 through A4

The four structures A1-A4 each have five rows of connected vias. Within each structure each row has 42 vias with alternating rows being tied to positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 1 mm



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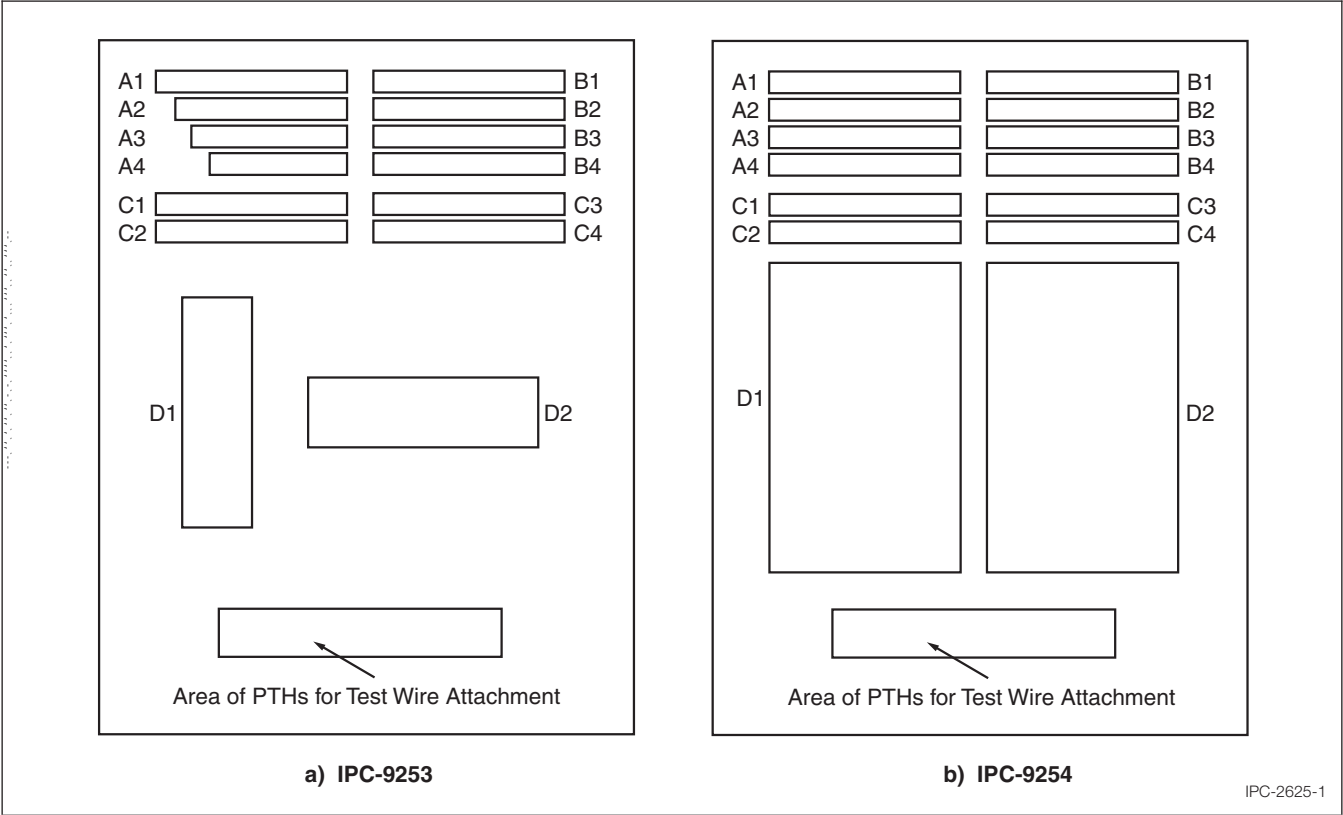


Figure 1 Layouts of Two Versions of the CAF Test Boards

[0.040 in] pitch between rows of daisy chain vias. The resulting via edge to via edge spacings are: 0.27 mm, 0.38 mm, 0.51 mm, 0.65 mm [0.0106 in, 0.0150 in, 0.0201in, 0.0256 in]. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in these four test structures A1-A4 are aligned with the glass fibers. Since A1-A4 evaluate susceptibility to CAF in just one direction, test coupons should be manufactured so that the machine direction of the woven fiber laminate reinforcement is perpendicular to the rows of same-net daisy chain vias (machine direction tends to fail first).

For both A and B test structures the inner and outer layer pads are the same, i.e., the same pad size is consistently used within a given test structure, although it does change from structure to structure. All via to electrode connections are made on layer 2 and are repeated on layer 9 so that a single etch-out will not affect results. Traces from via to electrode are routed on internal layers rather than external layers to minimize potential for surface insulation resistance failure.

Design details for each test structure A1-A4 follows in Table 1. Note: “Manhattan Distance” is the shortest orthogonal distance along the X- and/or Y- axes lines between adjacent drilled hole features (corresponds to the orthogonal nature of the laminate material’s woven glass fiber reinforcement (Figure 2)).

IPC-9253 and IPC-9254 Test Structures B1 through B4

The four “B” test structures have seven alternating rows of vias. Within each structure, alternating rows have either 27 or 26 vias with the alternating rows being tied to either positive or negative electrodes. The via edge to via edge spacing is varied from one structure to the next by using a different drilled hole size on the same 1.52 mm x 1.52 mm [0.05984 in x 0.05984 in] via grid. The 1.52 mm x 1.52 mm [0.05984 in x 0.05984 in] grid has an interstitial via therefore, tipping at a 45° angle results in a square 1.08 mm x 1.08 mm [0.04252 in x 0.04252 in] grid. Note: the sketches do not look square

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Table 1 Test Structures A1 through A4 Design Rules

	A1	A2	A3	A4
Outer layer pad size	0.86 mm [0.0339 in]	0.81 mm [0.0319 in]	0.75 mm [0.0295 in]	0.69 mm [0.0272 in]
Inner layer pad size	0.86 mm [0.0339 in]	0.81 mm [0.0319 in]	0.75 mm [0.0295 in]	0.69 mm [0.0272 in]
Drilled hole size	0.74 mm [0.0291 in]	0.63 mm [0.0248 in]	0.51 mm [0.0201 in]	0.37 mm [0.0146 in]
Via edge to via edge (shortest distance)	0.27 mm [0.0106 in]	0.38 mm [0.0150 in]	0.51 mm [0.0201 in]	0.65 mm [0.0256 in]
Via edge to via edge (Manhattan Distance)	0.27 mm [0.0106 in]	0.38 mm [0.0150 in]	0.51 mm [0.0201 in]	0.65 mm [0.0256 in]
On IPC-9254 only , bias applied between:	J1, J5	J2, J5	J3, J5	J4, J5

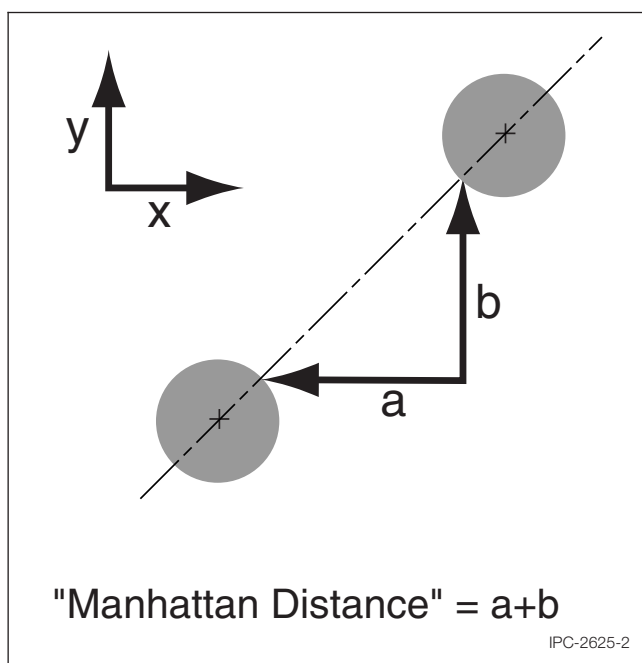


Figure 2 Manhattan Distance (Shortest Orthogonal)

when tipped 45° but, the CAF Test Boards do. The resulting via edge to via edge spacings are: 0.26 mm, 0.37 mm, 0.51 mm, 0.62 mm [0.0102 in, 0.0146 in, 0.0201 in, 0.0244 in]. Other than the use of different drilled hole sizes and a small change in pad sizes, the four structures are identical. The vias in the “B” test structure are not aligned with the glass fibers. If the failure mode is along glass bundles it is reasonable to expect the “B” test structure to perform better than the “A” structure for equivalent via edge to via edge spacings. Within a given test structure, the inner and outer layer pads for all 10 layers are the same, i.e., the same pad size is consistently used within a given test structure although, it does change

from structure to structure. All via to electrode connections are made on layer 1 and are repeated on layer 10 so that a single etch-out will not affect results.

A conceptual representation of the “B” test structure of the coupons in Figure 1 is shown to the upper right. Design details on each of the four “B” test structures follows in Table 2.

3.2 Other Structures Section C is designed to evaluate plated-through hole (PTH)-to-plane layer spacings. It is recommended to use the registration coupon per test board (IPC Test Pattern F) when CAF testing includes this region. Section D in the IPC-9254 design is for layer-to-layer Z-axis CAF testing. Section D in the IPC-9253 is for evaluating CAF resistance in a press-fit compliant pin connector application. The feature in the D region is an optional feature that is present automatically with the design. However, the A, B and C regions **shall** remain as designed in order to provide a standard basis of comparison.

The CAF test board with 10 layers is designated to evaluate thin single-ply constructions typically used on high performance boards. This board construction stackup can be reduced down to: (a) four layers by eliminating layers 3 through 8 and (b) only test structures A and B, when just evaluating differences between laminate materials.

3.3 CAF Test Board Design This 10-layer CAF test board for evaluating the insulation resistance between internal conductors within a printed wiring board has the following key features for evaluating hole-hole CAF resistance (Figure 3).

Holes In-Line (in-line with glass fiber direction): There are two rows of 42 signal-1 vias intermeshed with three rows of 42 signal-2 vias; for a total of 168 potential in-line PTH-PTH failures for each spacing distance.

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Table 2 Test Structures B1 through B4 Design Rules

	B1	B2	B3	B4
Outer layer pad size	0.94 mm [0.0370 in]	0.89 mm [0.0350 in]	0.84 mm [0.0330 in]	0.75 mm [0.0300 in]
Inner layer pad size	0.94 mm [0.0370 in]	0.89 mm [0.0350 in]	0.84 mm [0.0331 in]	0.75 mm [0.0295 in]
Drilled hole size	0.81 mm [0.0319 in]	0.71 mm [0.0280 in]	0.57 mm [0.0224 in]	0.46 mm [0.0181 in]
Via edge to via edge (shortest distance)	0.26 mm [0.0102 in]	0.37 mm [0.0146 in]	0.51 mm [0.0201 in]	0.62 mm [0.0244 in]
Via edge to via edge (Manhattan Distance)	0.37 mm [0.0146 in]	0.52 mm [0.0205 in]	0.72 mm [0.0283 in]	0.88 mm [0.0346 in]
On IPC-9254 only , bias applied between:	J7, J11	J8, J11	J9, J11	J10, J11

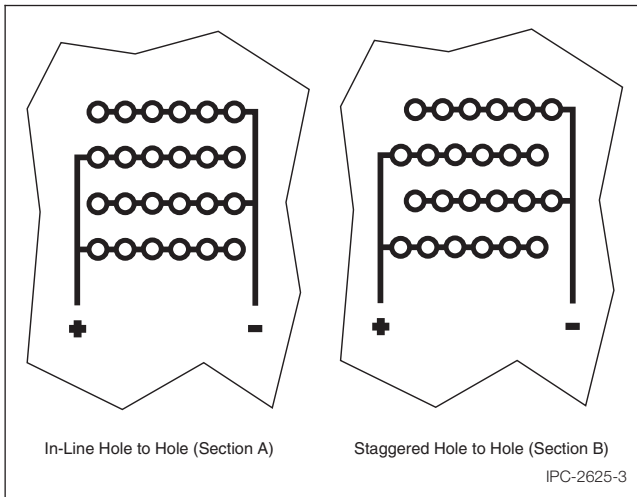


Figure 3 CAF Test Board PTH-PTH Spacing Design

Holes Staggered (closest PTH-PTH spacing in diagonal direction): There are three rows of 26 signal-1 vias intermeshed with four rows of 27 signal-2 vias; for a total of 312 potential diagonal PTH-PTH failures for each spacing distance.

3.4 CAF Test Coupon/Board Quantity The CAF testing data analysis technique recommended for either of these CAF test coupon/board designs requires a minimum 25 CAF test boards to be run per sample lot per bias level for statistical significance. This provides a total of 4,200 potential in-line hole-hole CAF failure sites and 7,800 potential diagonal hole-hole CAF failure sites for each unique sample/condition set.

For comparison, on a 1,428 I/O BGA device (Figure 4) there are about 500 power/ground pins. So with an average of slightly less than two adjacent power/ground pin spacings per pin there are about 1,000 potential in-line hole-hole CAF failure sites per BGA device. For a production board with the

equivalent of three of these BGA devices and about 1200 passives or other components with close power/ground pin spacings, the total number of opportunities for in-line CAF failure would then be about 4,200 (about the same as the entire CAF test board sample lot of 25 pieces).

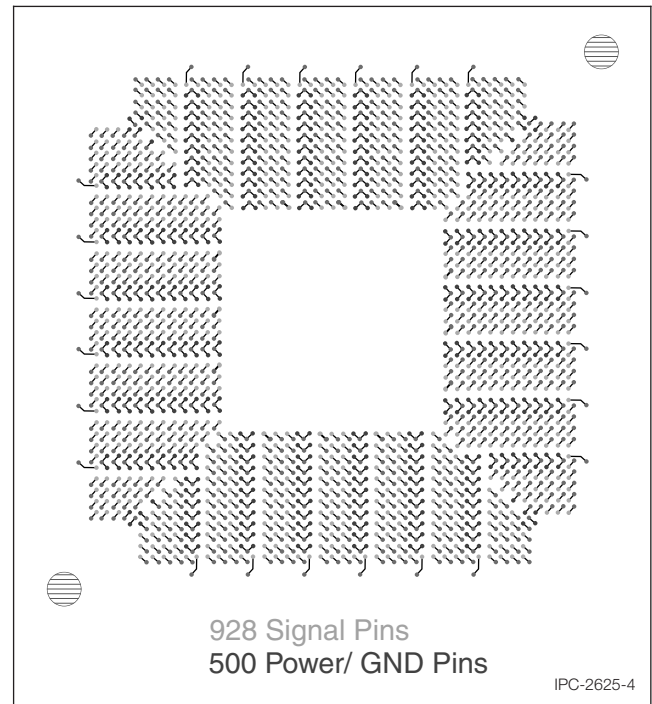


Figure 4 BGA Device I/O Pin Assignment

3.5 CAF Test Small Coupon Designs The IPC-9255 and IPC-9256 CAF test coupon designs (Figure 5) have 10 layers, each approximately 0.7 in x 5 in. Layers 5 and 6 have no trace routing, so removing them provides an 8 layer coupon. Conversely, by duplicating layers 5 and 6, a 14-layer or higher