



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1249

IPC-TM-650 TEST METHODS MANUAL

1 Scope This test method is used to quantify the deleterious effects of fabrication, process or handling residues on Surface Insulation Resistance (SIR) in the presence of moisture. The electrodes are long parallel traces (printed interdigitated comb patterns) on a standardized printed board or assembly. Samples shall be conditioned and measurements taken at a high humidity. Electrodes are electrically biased during conditioning to facilitate electrochemical reactions.

Specifically, this method is designed to:

- Simultaneously assess
 - a) leakage current caused by ionized water films and
 - b) electrochemical degradation of test vehicle, (corrosion, dendritic growth).
- Provide metric(s) that can appropriately be used for binary classification (e.g., go/no go, pass/fail).
- Compare, rank or characterize materials and processes.

2 Applicable Documents

2.1 IPC

IPC-A-24-G-KIT¹ Surface Insulation Resistance - Gerber Kit

J-STD-004 Requirements for Soldering Fluxes

IPC-A-600 Acceptability of Printed Boards

IPC-9201 Surface Insulation Resistance Handbook

2.2 American Society for Testing and Materials (ASTM)

ASTM D 257 Standard Test Methods for DC Resistance or Conductance of Insulating Materials

2.3 American National Standards Institute (ANSI)/NCSL International

ANSI/NCSL Z540-1 Calibration Laboratories and Measuring and Test Equipment - General Requirements

ANSI/NCSL Z540-2 American National Standard for Expressing Uncertainty - U.S. Guide to the Expression of Uncertainty in Measurement

1. www.ipc.org/onlinestore

Material in this Test Methods Manual was voluntarily established by Technical Committees of IPC. This material is advisory only and its use or adaptation is entirely voluntary. IPC disclaims all liability of any kind as to the use, application, or adaptation of this material. Users are also wholly responsible for protecting themselves against all claims or liabilities for patent infringement.

Number 2.6.3.7	
Subject Surface Insulation Resistance	
Date 03/07	Revision
Originating Task Group SIR Task Group (5-32b)	

2.4 International Electrotechnical Commission

IEC-61189-5 Test methods for electrical materials, interconnection structures and assemblies - Test methods for printed board assemblies

3 Test Samples The type and number of test samples (coupons) as well as method of preparation and test requirements should be described in the governing specification (e.g., J-STD-004) or procurement documentation.

If this test method is being used as a stand-alone document, decisions should be made regarding what samples might be the most appropriate for test. This SIR method should not be considered standard unless standard test vehicles are used.

Vehicles prepared for flux qualification shall be handled in a way that minimizes the possibility of ionic contamination. Use of ion-free gloves and wrap/bags is required. If testing a process, standard shipping and handling procedures shall be used.

For further information about sampling and sampling sizes see 7.1 and 7.1.2.

The IPC-A-24-G-KIT artwork package provides the necessary Gerber files for the fabrication of the standard IPC-B-24 test board used with this test method.

3.1 Test Controls Two cleaned bare IPC-B-24 test boards (bare copper on FR-4) shall be used as chamber controls.

3.1.1 Visually inspect the boards for any obvious defects, as described in IPC-A-600. If there is any doubt about the overall quality of any test sample, the board should be discarded.

3.1.2 Clean each control board by using deionized or distilled water and scrubbing with a soft bristle brush for a minimum of 30 seconds. Spray rinse thoroughly with deionized or distilled water. Rinse cleaned area thoroughly with virgin 2-propanol.

An alternative cleaning method is to place the test board in an ionic contamination tester containing 75% 2-propanol, 25% deionized water and process the solution until all ionics have been removed.



IPC-TM-650		
Number 2.6.3.7	Subject Surface Insulation Resistance	Date 03/07
Revision		

During the remainder of the preparation, handle boards by the edges only and use noncontaminating gloves.

3.1.3 Dry the cleaned boards for two hours at 50 °C.

3.1.4 If boards are to be stored before treatment, place the boards in Kapak™ bags or other contamination-free containers (do not heat seal) in a desiccator. (Kapak™ bags are available from Fischer, VWR and other distributors.)

3.1.5 When measured as described in Sections 4 and 5, if the control board readings are less than 1000 MΩ at any point after the initial 24 hours of SIR exposure, a new set of test coupons shall be obtained and the entire test repeated.

3.2 Blank Process Controls If performing process validation testing, two samples from an unprocessed blank should be run with the samples taken from the processed boards. Values obtained from unprocessed board samples are useful when failure is observed within the processed board sample. Failure of the unprocessed samples may indicate a problem with the incoming bare board rather than an assembly process.

4 Equipment/Apparatus It is the responsibility of the user of this method to verify equipment suitability. This method intends for all tolerances to be interpreted as uncertainties with a confidence interval of 95% as referenced in ANSI/NCSL Z540-1 and ANSI/NCSL Z540-2. Quantitative, qualitative and default information follow in the paragraphs below.

4.1 Electrometer Electrometer, High Resistance Meter, Picoammeter or equivalent as described by ASTM D 257.

- System must be capable of taking measurements and controlling the switching automatically (unattended).
- Minimum resistance measurement accuracy (not only meter, but as implemented)
 - 5% of full scale up to $10^{10}\Omega$ @ 5V
 - 10% of full scale up to $10^{11}\Omega$ @ 5V
 - 20% of full scale above $10^{11}\Omega$ @ 5V
- Accuracy with respect to the “true” value requires assessment of stability of the measurement system (after switching from bias voltage to the measurement voltage). Therefore, if the system does not automatically assess stability before logging, use an arbitrary time of one minute.
- The system described in this section must be able to make all measurements required within a 20 minute period and meet the requirements of 5.3.

It is preferred that the resistance reading be stable before acquiring the readings or data. If after one minute the signal remains unstable, a measurement should still be recorded.

4.2 Switching System

- Must have a channel-to-channel isolation resistance ten times greater than the resistance of typical SIR requirements, or a default channel-to-channel isolation resistance of $10^{12}\Omega$.
- <20-minute cycle while obtaining measurements as described above.
- Unique $10^6\Omega$ current limiting capability per channel.

4.3 Wire Attachments

- Single solid copper wire with PTFE insulation.
- Preferred solid wire solders (no flux), or nominally 1% by weight rosin nonactivated. See wire attach section of this document for more information.
- Electrical (EMI) shielding to guard cabling from stray currents.

4.3.2 Alternative Wire attachments such as stranded wire, non-PTFE insulation, edge connectors rather than hard wiring, and guarding techniques may be used provided the system accuracy is not compromised.

4.4 Controlled Temperature and Humidity Chamber

- Produce 40 ± 1 °C at $90 \pm 3\%$ R.H.
- Continuous or semicontinuous recording of this environment. ± 2 °C and $\pm 3\%$ R.H.
- Samples should not significantly impede airflow.
- Adequate mixing of water vapor and air is imperative to ensure condensation does not occur anywhere in the chamber except on/around cooling or dehumidification coils. If any part of interior of the chamber is below the dew point (possibly due to insulation or control issues), condensation will occur. This is not necessarily a problem as long as the samples are kept above the dew point and are shielded from dripping or flying condensate.

4.5 Camera Camera capable of recording color image.

5 Test Procedure

5.1 Interconnect Samples