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FINAL TASK GROUP REPORT

***Solderability Evaluation of
Thick and Thin Fused Coatings***



**THE INSTITUTE FOR INTERCONNECTING
AND PACKAGING ELECTRONIC CIRCUITS**
1717 HOWARD STREET • EVANSTON, ILLINOIS 60202



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IPC TASK GROUP REPORT ON SOLDERABILITY EVALUATION OF THICK & THIN FUSED COATINGS

This document reports on a program undertaken by the IPC to identify and evaluate the effects of thick and thin fused coatings on printed boards.

The importance of providing a protective coating to assure solderability of printed wiring boards prompted two studies undertaken by members of the IPC. The first, "Solderability of Printed Circuit Thin Fused Coatings," was completed in October, 1969 and reports on the solderability of test boards protectively covered by a hot solder dip and subsequently exposed to hot oil spray solder leveling processes. In the early 1970's, the trend was to thick fused coatings which made additional study imperative, to evaluate the results of a change in protective coating technology. "An Evaluation of Solderability of Thick Fused Coatings" was completed in 1978. Because the objectives of both programs are to evaluate the solderability of protective coatings, they are combined in this single report.

Any report about the state-of-the-art in a complex technology draws material from a vast number of sources. While the task group members are shown on the next page, it is impossible to list all of those that assisted and contributed in the evolution of this report. To each of them the IPC extends its gratitude.

Special thanks are in order to the following for their invaluable support and help in supplying materials, manufacture of test boards, fusing, and assistance in the evaluation of results and preparation of this report.

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D. Piper/Photocircuits • P. Bud/Electrovert
J. Hamilton/Hughes Aircraft • D. Bernier/Kester Solder

In addition, the members of the IPC express their appreciation to Hollis Engineering for providing the test soldering service as well as the microsectioning and photo micrographs used for evaluating the test boards.

The work of the two task groups was accomplished under the chairmanship of the following General IPC Committee.

ASSEMBLY METHODS AND JOINING TECHNIQUES COMMITTEE

<i>Chairman</i> P. J. Bud Electrovert	<i>Technical Liaison of the IPC Board of Directors</i> R. W. Mettler Circuit-Wise, Inc.	<i>Vice Chairman</i> D. F. Bernier Kester Solder
<i>Recording Secretary</i> D. J. Novick Englehard	<i>Past Chairman</i> J. A. DeVore General Electric	<i>Soldering Committee Chairman</i> J. D. Keller Motorola

The following is a listing of the two task groups that performed the evaluations defined in this report.

THIN FUSED COATINGS TASK GROUP

Chairman Barry Frederick/Hollis Engineering
 Anthony Orlowski/Army/Fort Monmouth • Ed Golonsbe/Methode Electronics
 Robert Griffith/Raytheon • Joseph Tarnowsky/Alpha Metals • Paul Budd/Electrovert
 Robert Foster/EPEC • Paul Gould/GTE Sylvania • Robert Ruleff/NCR
 Boyd Blaine/Cimron (Lear-Siegler, Inc.) • Joseph Keller/Martin Marietta

THICK FUSED COATINGS TASK GROUP

The following is a listing of the members of the Thick Fused Coating Task Group active during the time of the program. These IPC members have had the major responsibility since the inception of this program in September 1973. Many other people contributed their time and effort. We regret not all can be listed because without their helpfulness a program of this extent would not be possible.

Chairman K. G. Boynton/Hollis Engineering
 C. Bernard/IBM • D. Elliott/Electrovert • J. Faris/Raytheon
 J. Keller/Motorola • J. Long/Tin Research Institute • W. Abbott/Hollis Engineering
 D. Schoenthaler/Western Electric • L. Low/Hughes Aircraft • A. Mondo/General Electric
 R. Woodgate/Hamilton Standards • B. Costello/Argus • T. Allen/Sandia
 D. Novick/Englehard • T. O'Rourke/Hollis Engineering

TABLE OF CONTENTS

SECTION	PAGE
I Objective and Scope	1
II Conclusion and Recommendations	2
Thin Fused Coating Task Group	2
<i>Conclusions</i>	2
<i>Recommendations</i>	2
Thick Fused Coating Task Group	2
<i>Conclusions</i>	2
<i>Recommendations</i>	2
Summary of Both Programs	3
III Details of Thin Fused Coating Program	4
Background Information	4
Test Description and Results	4
<i>General</i>	4
<i>Salt Spray</i>	4
<i>Surface Appearance</i>	4
<i>Evaluation Methods</i>	5
IV Details of Thick Fused Coating Program	6
Background Information	6
Test Description Results	6
<i>General</i>	6
<i>Amendment to Program</i>	6
<i>Phase II Testing</i>	6
Appendix A — Test Board Pattern Drawing	9
Appendix B — Test Plan (Thick Fused Coating)	10
Appendix C — Measurement of Fusing	12
Appendix D — Conductor Surface Evaluation After Fusing	17
Appendix E — Evaluations After Soldering	23
Appendix F — IPC-S-801—Edge Dip Solderability Test	26



SECTION I

Objective and Scope

The following are the objectives and scope of the two IPC task groups formed to evaluate solderability conditions and requirements.

THIN FUSED COATINGS (1967-1969)

The solderability of printed boards was to be examined after copper conductors had been cleaned and protectively covered by a hot solder dip and subsequently exposed to a solder leveling process. Epoxy laminate printed boards processed up to the solder leveling step were all to be prepared by the same process and by one manufacturer, so that testing would be for the one variable, *solderability of the solder leveled surface*.

The boards were to be tested after aging periods of 0-3-6-9 and 12 months. Boards were to be tested after solder leveling where all excess solder was removed from the copper conductor leaving essentially only the intermetallic. A second group of boards were to be tested using solder thickness above the intermetallic as would be obtained from the solder leveling process. The solder leveling operations were to be performed on three different solder leveling machines. Solderability was to be measured by the IPC-S-801 standard and backed by a number of other supporting test techniques such as, hand soldering and wave soldering. Salt spray corrosion testing of leveled surfaces was also to be performed using electrodeposited solder boards as control standards.

THICK FUSED COATINGS (1973-1978)

Many printed boards are subjected to a solder fusing (or reflow) process as a final and additional step in the manufacturing process. Prior to this, the traditional finish has been electroplated tin-lead which serves as an etch-resist as well as a protective coating. An immersion-tin process is sometimes also used to cover exposed copper edges.

The thick fused coatings evaluation program was approved at the September 1973 IPC meeting and was undertaken to determine the shelf life solderability difference between fused and non-fused boards, and how the fusing process affects solder slivers, bridging, plated hole diameters, solder "balling" and exposed copper edges. In essence to determine near and long-term solderability and answer the question . . . "To fuse or not to fuse?"

The primary objective was to determine solderability, as a function of time of unfused tin-lead plating as compared with fused plating. A secondary objective was to determine as peripheral information:

- Effects of removing etch sliver overhang on conductors and/or covering conductor edges or side walls
- Effects of changing diameter of plated-through hole after fusing
- Effects of solder "balling" on narrow conductors

See Figures 1 and 2 for a view of both sides of the board.



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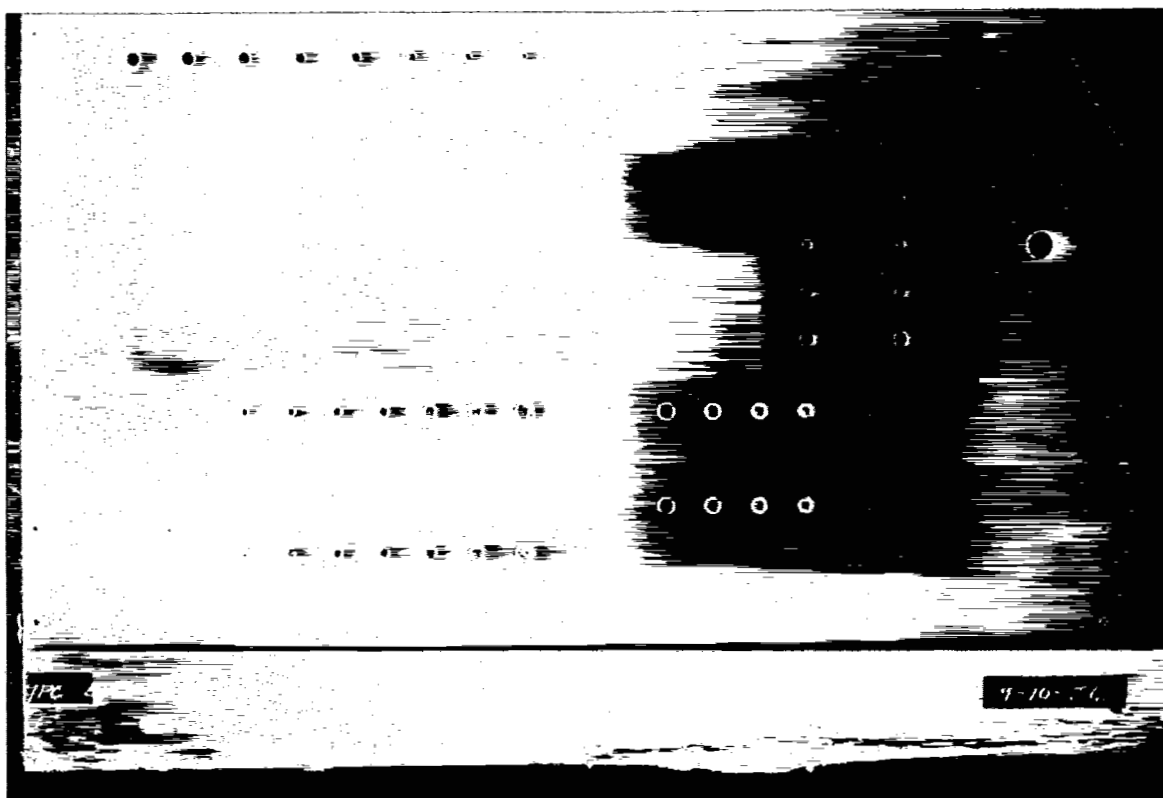
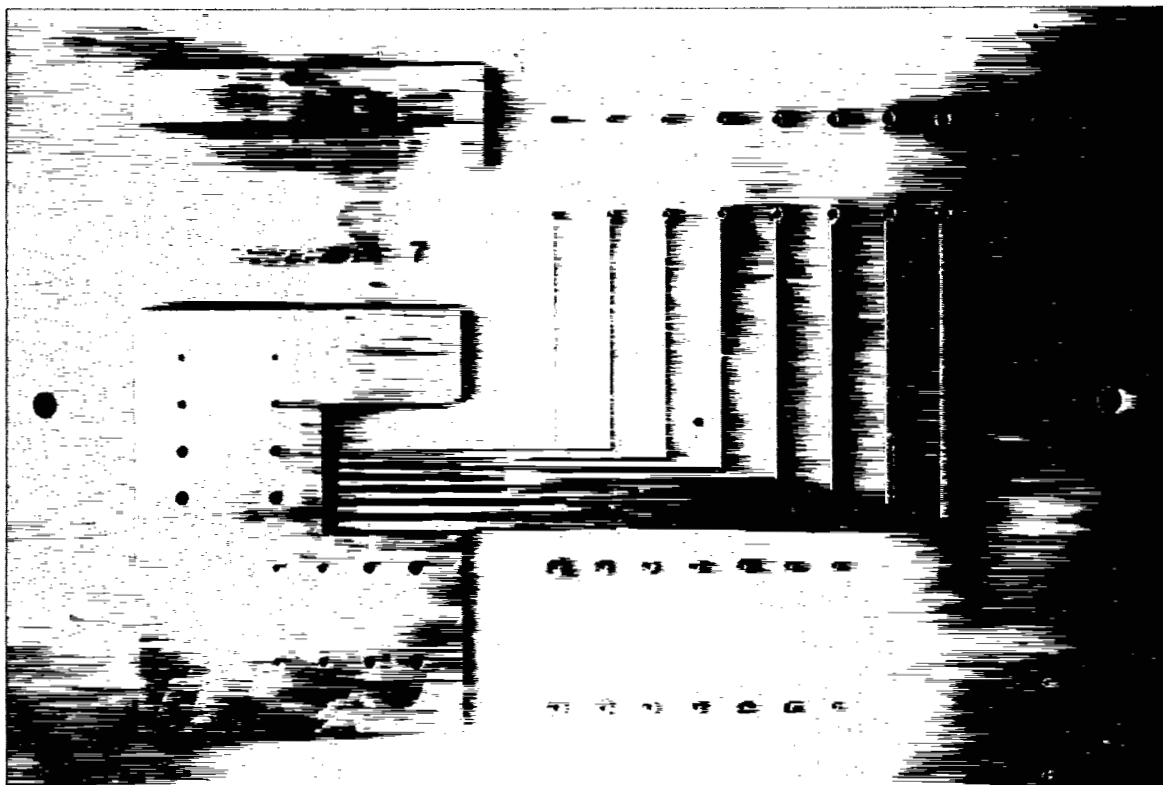


Figure 2.

SECTION II

Conclusion and Recommendations

The following are the conclusions and recommendations reached by the two task groups.

THIN FUSED COATING TASK GROUP**Conclusions**

- Solder leveling solder covered printed boards did not lower conductor solderability after aging periods of 0-3-6-9 and 12 months on all boards tested with thickness obtained by solder leveling processes.
- Neither solder leveled printed boards nor the electroplated control boards failed salt spray tests after 3, 6, and 12 month age periods.
- Drain lines or other surface discontinuities did not affect solderability on solder leveled surfaces.
- As a supplement to test standard IPC-S-801, wave soldering should be included as a solderability test for thin fused coatings with easier to interpret test results.

Recommendations

- Prepare an IPC acceptance specification standard for thin fused coatings.
- Recommend revision to military and other specifications, that may exist, so as to delete minimum solder thickness call out.
- Institute an ad hoc committee to supplement Electrodeposited Solderability Test IPC-S-801 with wave soldering for printed boards.

Note: Since this recommendation was made the IPC has developed a wave solder test method IPC-S-803.

THICK FUSED COATINGS TASK GROUP**Conclusions**

With regard to solderability, the test program demonstrated:

- There is no apparent difference in solderability as a result of aging, at least over the 12 month test period.
- It is not necessary to fuse tin-lead electroplate to improve solderability.
- Fusing indicated proof of solderability.
- Wavesoldering wet all hole surfaces, including top land areas of all boards, fused or unfused, despite the absence of leads to assist or hinder capillary action.

In addition:

- Fusing eliminated solder slivers.
- Fusing revealed conductor discontinuities or reduction in path width caused by overetching.
- Fusing eliminated tin-lead nodules in plated holes.
- Fusing did not assure solder coverage of all conductor edges.
- It is difficult to visually observe the presence of fused solder on conductor edges previously coated with immersion tin.
- Boards solder-dipped/hot air leveled resulted in complete coverage of all conductor surfaces and edges.
- Hot liquid leveling removed all of the protective nascent tin-lead electroplate except for the intermetallic compound.
- All fusing processes, except hot liquid and solder dipped/hot air leveled, resulted in some reduction of hole diameters and filling of some small holes.



Recommendations

The evaluation of thick fused coatings should be considered complete. Since this report was based solely on printed boards manufactured by the subtractive process, the following objectives are proposed for future study.

- Printed boards manufactured by additive, semi-additive, thin foil, tenting, hole plugging, screened solder paste processes and flexcircuits.

- State-of-the-art processes such as condensation solder fusing.
- Formulation of an IPC specification for thick fused coatings and acceptance criteria.
- Redesign of the test board to be typical of current printed board configurations (conductor patterns, spacings, ground planes, solder resist mask, etc.) to be compatible with all processes.
- Test board designed to be used as an IPC standard for use in setting parameters for soldering systems.

SUMMARY OF BOTH PROGRAMS

In summarizing the essential points of thin and thick fused coatings, it is apparent that both have several things in common. Coatings applied over clean copper are readily solderable. Thick or thin solder is effective as a protective coating even after aging of up to one year. Fusing of tin lead electroplate does not necessarily improve solderability but does provide indication of proof of solderability. Wavesoldering served as an effective test for solderability. Both programs recommend the formulation of IPC acceptance specifications and revision of MIL and other specifications to include realistic thicknesses of solderable coatings. It is hoped that the information supplied in the reports prepared by the task groups will help guide the industry in its quest to product high quality, reasonably priced printed wiring boards.



SECTION III

Details of Thin Fused Coating Program**BACKGROUND INFORMATION**

Two hundred and thirty-four printed boards containing 1,872 test configurations were fabricated and prepared taking particular care to chemically clean the copper and solder dip the boards in accordance with the program developed by the "Solderability of Printed Circuit Thin Fused Coatings" committee. All printed boards had good initial solderability after solder dipping, and were then evenly distributed from a central source to three solder leveling machine manufacturers.

Each manufacturer leveled the printed circuit boards in two groups. The first group (B) was leveled to the manufacturer's normal process, while the second group (A) was leveled using a concerted effort to remove all excess solder from the printed circuit board conductors. These boards were returned to the originating point whereupon the boards were stored and aged in accordance with the program guidelines.

The boards were reviewed by the committee at the 0, 3, and 6 month age period, March 3 and 4, 1969. On September 8, 9, and 10, 1969, the 9 and 12 month aged boards were reviewed. A 6-month report was submitted and accepted at the IPC meeting in Washington, April 1969. The final report was drafted by the committee on September 10, 1969.

The program objective to evaluate solderability of solder leveled printed boards was accomplished.

The committee finds that printed boards that had initial solderability before solder leveling retained solderability after solder leveling as tested in this program at 0-3-6-9 and 12 month age intervals. Furthermore, the test results did not indicate any noticeable difference in the solderability between the two groups (A and B) even after aging for 12 months.

In addition to testing for solderability, solder leveled boards were also tested for salt spray corrosion resistance. Control boards of electrodeposited solder when compared to solder leveled boards were no better than the *solder leveled boards after salt spray treatment*. This salt spray corrosion resistance testing was conducted on boards aged for 3, 6, and 12 month periods. While superficial stains did appear on the test specimen surfaces which could be removed by erasing, it was found that solder leveled boards which were leveled in accordance with the manufacturer's process, with

no attempt to remove all excess solder, contained the fewest number of stained spots, and were essentially in a remarkable condition.

TEST DESCRIPTION AND RESULTS**General**

This program included salt spray testing, board surface preparation, solderability testing and board aging. The program also defined, in detail, the methods for cleaning the printed boards and the manner in which the program should be conducted so as to keep variables to an absolute minimum, thus enhancing meaningful test results.

The test specimen consisted of various test configurations which were examined for solderability after solder leveling. A finger test grid on the upper half of the test specimen was not part of the edge dip test although this portion was solder leveled. A test specimen number running from the grid finger identified areas which were used for photomicrographs when solder thickness measurements were made.

Salt Spray

All printed boards passed the salt spray test, including the control pieces which were electrodeposited solder. All boards were stained to some degree. The boards leveled, where no attempt was made to remove all solder, contained the least (almost none) staining.

Surface Appearance

Solder level surfaces after edge dip testing were found to be different in appearance than edge dipped bare copper surfaces or solder coated copper unleveled surfaces. The appearance difference is that leveled surfaces, after edge dipping, may contain "drain lines" that are similar in appearance to dewetted areas, but unlike dewetting, the drain line areas were bright and shiny. This drain line effect appears on printed boards edge dip tested immediately after solder leveling, as well as on boards that were edge dip tested on leveled surfaces and aged for 3-6 month periods. The drain line effect was considerably less noticeable on leveled boards that had been aged for 9-12 months.



Within the 12 month aged board groups, a grainy condition appeared after edge dip testing. Subsequent test showed that this grainy surface condition was due to a contaminated solder dip pot. Furthermore, the drain line or grainy appearance was tested for solderability by other methods in addition to the edge dip test as outlined in IPC-S-801. These additional methods were wave and hand soldering, both with and without inserted wires within the printed board. The drain lines or grainy condition disappeared upon wave soldering, and the wave and hand soldered boards exhibited good solderability. The subsequent testing was conducted on a 9 and 12 month aged group which was not previously dip soldered.

Evaluation Methods

As previously mentioned, the primary solderability test method was the IPC-S-801 method using the photographic aids as shown in Figure 2 of the standard (see Appendix F). All solderability decisions were qualitative in accordance with IPC-S-801. However, in order to complement this test method it has also been mentioned that additional testing was performed by wave soldering and hand soldering and these additional methods were found to be in agreement with the specification.



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