

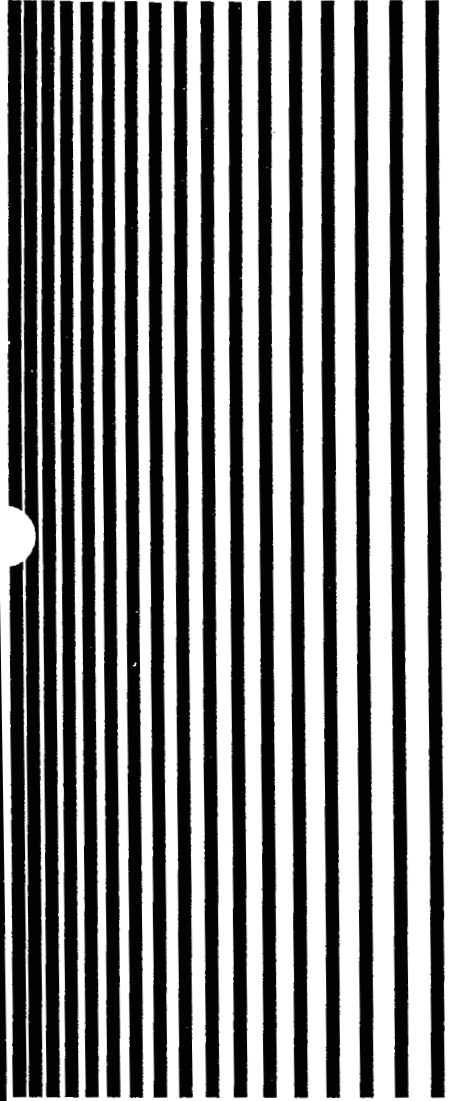
IPC-TR-470

PUBLISHED JANUARY 1974

**TECHNICAL
REPORT**

**THERMAL CHARACTERISTICS
OF MULTILAYER
INTERCONNECTION BOARDS**

PREPARED BY
ROGER N. WILD, IBM
OWEGO, NEW YORK



IPC



Documents

Document Sharing Hub

Material in this Technical Report was voluntarily contributed by a member of the IPC. This material is advisory only and its use or adaptation is entirely voluntary. IPC disclaims all liability of any kind as to the use, application, or adaptation of this material. Users are also wholly responsible for protecting themselves against all claims or liabilities for patent infringement.

© IPC First Printing January 1974 1M
Second Printing July 1984 1M



Documents
Document Sharing Hub

THERMAL CHARACTERIZATION OF
MULTILAYER INTERCONNECTION BOARDS

A Technical Report Prepared By

Mr. Roger N. Wild
Materials Development and Analysis Dept.
IBM CORPORATION
Owego, New York

Presented at the IPC Open Technical
Seminar Sheraton Palace Hotel, San
Francisco, Calif. September 10, 1973

FOREWORD

The material published in this Technical Report is based on the comprehensive presentation by Mr. Roger N. Wild, IBM Corporation, during the IPC Open Technical Seminar held in San Francisco September 10, 1973.

Because of the widespread interest in this document we did not feel it was practical to shorten this data for inclusion in the monthly issue of the Technical Review.

By publishing this report as a separate unabridged document, we are able to make Mr. Wild's entire report available to our members.

This Technical Report is published for informational purposes only. IPC disclaims any liability for the use, application, or adaptation of this material.



TABLE OF CONTENTS

Section	Page
INTRODUCTION	1
THERMAL SHOCK TEST COMPARISONS	2
RESULTS	4
EFFECTS OF SEVERE THERMAL CYCLING	5
SAMPLE PREPARATION	6
FAILURE POINTS	6
THERMAL CYCLE	7
Thermal Cycle Results	7
Added Cycling Tests	9
Comparison of Some Different Thermal Cycle Environments ..	9
FAILURE MODES	11
METALLOGRAPHIC EXAMINATION	11
ELECTRICAL FAILURE MODES	13
ADDED FAILURE COMMENTS	14
SOME THERMAL DESIGN CONSIDERATIONS	15
DESIGN FACTORS	15
MULTILAYER BOARD STRESS CLASSIFICATIONS	16
DESIGN TABLES	17
ACKNOWLEDGEMENTS	19
REFERENCES	19

LIST OF ILLUSTRATIONS

Figure		Page
1	Test Sample	2
2	Thermal Cycling Profile (One Cycle)	7
3	Soldering Effects on Thermal Cycling Reliability ⁽¹⁾ (-62°C to +125°C Cycle)	8
4	Estimated Minimum Life Thermal Cycling Comparisons	10
5	Thermal Comparisons	10
6	Failure After 28 Multiple Hand-Soldering Operations	12
7	Typical PTH Failure Modes	12
8	Inner Plane Cracking and Through-Hole Plating Cracks	13
9	Plated-Through-Hole Mechanical Support	19

LIST OF TABLES

Table		Page
1	Number of Cycles to Failure in Thermal Shock Test Environments (Electrical Failure)	4
2	Thermal Shock Temperature Comparisons (Heating Effects)	5
3	Design-Review MIB Thermal Stress Ratings	17
4	Design-Review MIB Thermal Stress Classifications	18

THERMAL CHARACTERIZATION OF
MULTILAYER INTERCONNECTION BOARDS

by

R. N. Wild

for the

Institute of Printed Circuits
September 1973

ABSTRACT

This study was conducted to better understand the effects of different thermal environments on the reliability of copper plated-through holes (PTHs) in Multilayer Interconnection Boards (MIBs). The study included tests to determine failure points in thermal shock and soldering environments, in addition to the effects of a very severe thermal cycling environment on solder-filled versus unfilled PTHs. Failure modes and some thermal design considerations are also presented.

The results of this study show both the reliability and some limits of Multilayer Interconnection Boards in severe thermal environments. The study also shows that the reliability of properly made PTHs is not generally improved by solder filling, in fact overall reliability is reduced.



Documents
Document Sharing Hub

THERMAL CHARACTERIZATION OF MULTILAYER INTERCONNECTION BOARDS

by

R. N. Wild
IBM Electronics Systems Center
Owego, New York

INTRODUCTION

This study was conducted to better understand the effects of different thermal environments on the reliability of plated-through holes (PTHs) in Multilayer Interconnection Boards (MIBs). This study included tests to determine limits and failure points in different type thermal shock and soldering environments, in addition to determining the reliability difference between solder-filled and unfilled PTHs in a very severe thermal cycling environment. A brief outline of this study is as follows:

- Effects of Thermal Shock Testing
- Effects of Severe Thermal Cycling With:
 - No Solder in PTHs
 - Solder-Filled PTHs
 - Pin in PTHs
- Effects of Production Type Soldering
- Failure Modes
- Thermal Design Considerations.

A special series of electrical test MIBs were fabricated for this study, using normal MIB production processing techniques. These MIBs (Figure 1) contained four rows of 0.024-inch-diameter PTHs electrically connected in series, so that copper PTH continuity could be electrically monitored during the various thermal tests. The electrical series circuit was connected to the top, middle, and bottom internal circuit layers within the boards. The copper plating in the PTH was a ductile 1.2-mil-thick pyrophosphate copper plating. The innerplanes were of 1-oz copper.