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IPC-TR-486

Report on Round Robin Study to Correlate Interconnect Stress Test (IST) with Thermal Stress/ Microsectioning Evaluations for Detecting the Presence of Inner-Layer Separations

IPC-TR-486

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A technical report developed by IPC

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Report on Round Robin Study to Correlate Interconnect Stress Test (IST) with Thermal Stress/Microsectioning Evaluations for Detecting the Presence of Inner- Layer Separations

Developed by the Post Separation Task Group (D-33c) of the Rigid Printed Board Committee (D-30) of IPC

Users of this technical report are encouraged to participate in the development of future revisions.

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REPORT ON ROUND ROBIN STUDY TO CORRELATE INTERCONNECT STRESS TEST (IST) WITH THERMAL STRESS/MICROSECTIONING EVALUATIONS FOR DETECTING THE PRESENCE OF INNER-LAYER SEPARATIONS

SECTION 1 — INTRODUCTION

OBJECTIVE

The objective of this round robin was to provide the industry with a test method that removes the subjectivity of microsection evaluation after Thermal Stress exposure for detecting the presence of inner-layer separations in plated-through holes and gives greater reproducibility than current optical evaluations.

The purpose of this test program is to determine the ability of Interconnect Stress Testing (IST) to induce and measure inner-layer separation and to correlate IST with Thermal Stress/microsection testing. The two specific test methods used were IPC-TM-650, Methods 2.6.26 - DC Current Induced Thermal Cycling Test, and 2.6.8 - Thermal Stress of Plated-Through Holes.

The goal was to assess IST use as a test for incoming inspection in lieu of Thermal Stress.

BACKGROUND

The IPC D-33c Post Separation Task Group was formed in the fall of 1989. It had the following objectives:

- Provide a forum for discussion regarding detection of separation between inner-layers and plated-through hole wall copper.
- Establish a round robin.
- Distribute a questionnaire regarding:
 - Occurrence of inner-layer separation.
 - Microsection processes used to determine presence of inner-layer separation.
- Determine capability of test methods within testers.
- Collect Field Failure information.

The need for such a group was based on the fact many bare boards were found to have inner-layer separation after assembly processing which was not detected by the lot acceptance testing at the board shop level.

From 1989 to 1991 a questionnaire was developed, disseminated and analyzed. It then became apparent that there were many different approaches to making and evaluating microsections.

In 1991 a charter for a subsequent round robin was developed. The charter was to evaluate the use of microsections to find very fine inner-layer separations. Samples were built which were known to have varying degrees of inner-layer separation after Thermal Stress exposure for this round robin. Conclusions from that initial round robin are as follows:

- There was agreement between testers on inner-layer separations $>$ than approximately $2.5\ \mu\text{m}$ [$100\ \mu\text{in}$].
- There was no agreement between testers on inner-layer separations $<$ approximately $0.8\ \mu\text{m}$ [$30\ \mu\text{in}$].
- Microsections must be etched to verify that observations made in the as polished condition are inner-layer separations.
- Agreement between testers is possible when testers evaluate the same mounts.
- The samples prepared of the coupon set without any thermal stress did not show any inner-layer separations. This was consistent for all laboratories involved in the round robin.
- There was no consensus regarding observations in the “as polished” condition.
 - Improper etching can obscure fine-line inner-layer separations.
 - Scanning Electron Microscopy analysis of the same samples did not show a one to one correlation between lines observed as polished and confirmed inner-layer separations after etching.



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- Correlation between testers, when evaluating product with fine-line inner-layer separations, is possible on a lot to lot basis, but not panel to panel.

In the spring of 1992 the task group decided to add more stress to the samples exhibiting “fine-line” ($<0.762\text{ }\mu\text{m}$ [30 μin]) inner-layer separations prior to microsectioning evaluations. It was thought that increased stress would cause the “fine-line” inner-layer separations to open and therefore be more easily detected. Two methods for doing this were:

- Ten cycles of liquid nitrogen at -196°C [-320°F] to oil at 288°C [550°F] (thermal shock)
- Multiple Thermal Stress (1 - 5) per IPC-TM-650, Method 2.6.8, 10 second float on solder at 288°C [550°F]

These additional stress exposures did not result in significant differences in the inner-layer separations noted in the prior round robin. An attack polish method for microsectioning was also developed to aid in detection in the as polished condition.

In 1993 the task group requested the Technical Activities Executive Committee (TAEC) permit the group to run a round robin on actual industry product to determine the amount of inner-layer separation present in the industry. This was denied. The TAEC requested that instead the task group find a test other than microsectioning to detect inner-layer separation.

From 1993 to 1995 the task group investigated the ability of an IBM technique - LATEST TESTER - to detect inner-layer separation. Other round robins were enacted and many more panels of boards were produced with varying degrees of inner-layer separation. These additional round robins included testing holes with and without lands and with multiple Thermal Stress exposures. More than 16 exposures to hot air leveling were required prior to LATEST testing to detect inner-layer separation. This was compared to one thermal stress per IPC-TM-650, Method 2.6.8, followed by microsectioning. While the LATEST tester could detect inner-layer separation after a gross number of exposures to hot air leveling, the group did not want to go to the industry with a test that required a large number of exposures to stress. Please note that the LATEST TESTER was developed to detect dishdowns in conductor runs and has proved to be very adequate in that effort.

Between 1993 and 1998 members of this task group worked to revise IPC-TM-650, Method 2.1.1, Microsectioning, Manual Method and Method 2.1.1.2, Microsectioning - Semi or Automatic Technique Microsection Equipment.

In the spring of 1995, the INTERCONNECT STRESS TEST (IST) was introduced to the task group. In this technique, the test coupon is resistance heated by passing DC current through the internal layer connection to the barrel for three minutes to bring the temperature of the copper to a designated temperature (slightly above the T_g of the laminate in the sample). Switching the current on and off, creates thermal cycles between room temperature and the designated temperature within the sample. This thermal cycling induces cyclic fatigue strain in the plated-through hole barrels and internal layer interconnects and accelerates any infant mortality or latent defects.

Since that time, a multitude of reports of individual testing programs have been presented to various groups regarding plated-through hole reliability as a function of barrel and inner-layer connection performance. Most of that data was presented as an attempt to correlate IST with thermal oven type testing, similar to that performed on final assemblies.

In the fall of 1997, a test program was finalized and boards were to be fabricated. The test program was delayed due to insufficient board shops producing the varying quality levels of inner-layer separations. In the spring of 1999, sufficient panels were received to start the test plan.

This technical report contains detailed information regarding the round robin conducted in 1999 using the IST test method and Thermal Stress testing followed by microsectioning in order to determine the ability of the IST method to be offered as an alternate method to detect inner-layer separation and to determine correlation between the two types of tests. This report details the findings of this study and the recommendations of the task group.

SECTION 2 — CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

The IPC D-33c Post Separation Task Group has identified an alternate test method to Thermal Stress/microsectioning for the detection of inner-layer separations. We have determined that the results of the Interconnect Stress Test (IST) correlate with the results of the Thermal Stress/microsectioning technique.

1. Correlation between IST and Thermal Stress/microsectioning is established on samples with gross inner-layer separations and samples with no inner-layer separation.
2. IST is more consistent between testers than Thermal Stress/microsection method on samples with fine-line inner-layer separations on a sample by sample basis.
3. There is evidence from IST testing that small holes are less likely to exhibit inner-layer separation than larger holes from the same panels. These findings correlate with industry experience.
4. On fine-line inner-layer separations, IST is more sensitive due to the following:
 - a. 100 holes are tested as compared to three holes examined in Thermal Stress/microsections.
 - b. 360 degrees of a hole are tested as compared to two planar views in microsections.
 - c. Results are numerical values rather than the subjective judgment of a technician.

RECOMMENDATIONS

1. The industry should work to develop pass/fail criteria and testing parameters for IST both as a product acceptance test and a product reliability test.
2. The coupons used for Thermal Stress testing should include both the smallest electrically functional holes and the largest component holes found on the panel they represent instead of only the smallest holes as currently required. (This recommendation does not apply to microvias.)
3. The IPC 6-10c Plated-Through Via (PTV) Reliability Task Group should further explore various dependencies pertinent to hole reliability for increased understanding.



SECTION 3 — ROUND ROBIN TEST PROGRAM DETAILS

The complete test plan is included in Appendix D.

It is important to understand that some of the test criteria chosen to determine the presence of inner-layer separation are only directly applicable to this set of samples and test plan. The 150 cycles, maximum temperature, and 2% change in resistance limit were chosen for this round robin and should not be used to establish pass/fail criteria for product. The test plan and the results generated in this round robin are not intended to make reliability or hierarchy-of-failure statements. The manner in which IST was performed should not be assumed to be a recommendation for actual product.

TEST PANELS

Each panel consists of 126 coupons - 48 Thermal Stress coupons and 72 IST coupons. The panel design has coupons both with and without nonfunctional lands.

Design Features

Image Pattern	126 coupons (54 IPC-2221 "A" coupons and 72 IST coupons)
Number of Layers	10
Board Thickness	2.54 mm [0.100 in] $\pm$ 0.25 mm [0.010 in]
Material Properties	Final T_g (TMA) 130°C [266°F] or higher*
Layer 2-3 and Layer 8-9 Dielectric Opening	0.15 mm [0.006 in] - 0.25 mm [0.010 in] thick
Copper Foil - Outer Layers	One-half ounce Grade 1 (not HTE) copper
Copper Foil - Inner-layers	1.0 ounce HTE copper
Internal Land Configuration	Non-functional land and functional lands**
PTH Hole Diameters / Grid Sizes***	0.34 mm [0.0135 in] / 1.3 mm [0.050 in] 0.71 mm [0.028 in] / 1.3 mm [0.050 in] 1.2 mm [0.0465 in] / 2.54 mm [0.100 in]

*Each lot of boards was produced from the same material lots from the same supplier.

**Regardless of the internal land configuration, lands were placed on Layers 1, 2, 3, n-2, n-1, and n on all coupons. Lands at these locations are required for the IST coupon to be functional.

***The diameters and grid sizes apply to both the IPC-2221 "A" coupons and IST coupons.

Panels had the following lay-up:

Layer 1	signal
Dielectric	2 sheets 1080 prepreg 0.127 mm [0.005 in]
Layer 2	signal
Dielectric	core 0.20 mm [0.008 in]
Layer 3	signal
Dielectric	2 sheets 2116 prepreg 0.28 mm [0.011 in]
Layer 4	power/ground
Dielectric	core 0.36 mm [0.014 in]
Layer 5	signal
Dielectric	2 sheets 2116 prepreg 0.28 mm [0.011 in]
Layer 6	signal
Dielectric	core 0.36 mm [0.014 in]
Layer 7	power/ground
Dielectric	2 sheets 2116 prepreg 0.28 mm [0.011 in]
Layer 8	signal
Dielectric	core 0.20 mm [0.008 in]
Layer 9	signal
Dielectric	2 sheets 1080 prepreg 0.127 mm [0.005 in]
Layer 10	signal

Panels were fabricated to insure uniform cure of all panels.

Fabrication Flow

Two manufacturers submitted a total of 24 panels. The board manufacturers were identified as Manufacturer A and Manufacturer B.

The board manufacturers were requested to manufacture panels with different inner-layer interconnect qualities, with expected levels of inner-layer separation after Thermal Stress exposure ranging from “gross” to none. This produced six sets of samples identified as:

A1	Manufacturer A	“Gross” inner-layer separation expected
A2	Manufacturer A	“Fine-line” inner-layer separation expected
A3	Manufacturer A	No inner-layer separation expected
B1	Manufacturer B	“Gross” inner-layer separation expected
B2	Manufacturer B	“Fine-line” inner-layer separation expected
B3	Manufacturer B	No inner-layer separation expected

Drill Process

Panels were drilled one high. The maximum number of drill bit hits per tool is 1,000 holes to reduce hole quality variability. The goal was to produce sufficient hole quality so inner-layer separation would be the primary failure mode rather than barrel cracks.

Desmear/Plating Process

Each fabricator chose the appropriate desmear and/or etchback processes to produce three levels of inner-layer separations - no separations, “fine-line” separation, and “gross” separation.

The suppliers used different metallization systems. Manufacturer A used palladium-based direct metallization and Manufacturer B used low build electroless metallization.

Hole wall plating thickness was to be 0.025 mm [0.0010 in] - 0.051 mm [0.0020 in] when measured anywhere along the barrel of the hole. This plating thickness was chosen so inner-layer separation would be the failure mode rather than barrel cracks. Target average copper thickness was 0.033 mm [0.0013 in]. The actual plating thickness was recorded for each panel and hole size.

Final Finish / Soldermask Process

The use of solder mask on these panels was optional and left to the fabricator’s discretion. Boards supplied by Manufacturer A did not have solder mask; boards supplied by Manufacturer B had solder mask.

All panels were coated with solder by Hot Air Solder Leveling (HASL).

Each fabricator submitted four panels for each level of inner-layer separation.

COUPON DESCRIPTION

Thermal Stress coupons are a three-hole by three-hole matrix similar to that of the “A” coupon found in IPC-2221 (see Figure 1).

Each IST coupon contains two daisy chains of 100 holes each. One daisy chain monitors barrel performance and the other monitors inner-layer connection performance (see Figure 2).

TESTER IDENTIFICATION

The five Thermal Stress/microsection labs were assigned identifications of XLAB1 - XLAB5.

The five IST testers were assigned identifications of IST1 - IST5.

COUPON DISTRIBUTION

Coupons were distributed to all testers by IPC. When the panels were received by IPC, each panel was assigned a number 1 through 24 so all coupons were traceable to an individual panel and the exact location on the panel. The actual record of distribution can be found in the appendix.

One Thermal Stress/microsectioning lab also received and tested IST coupons.

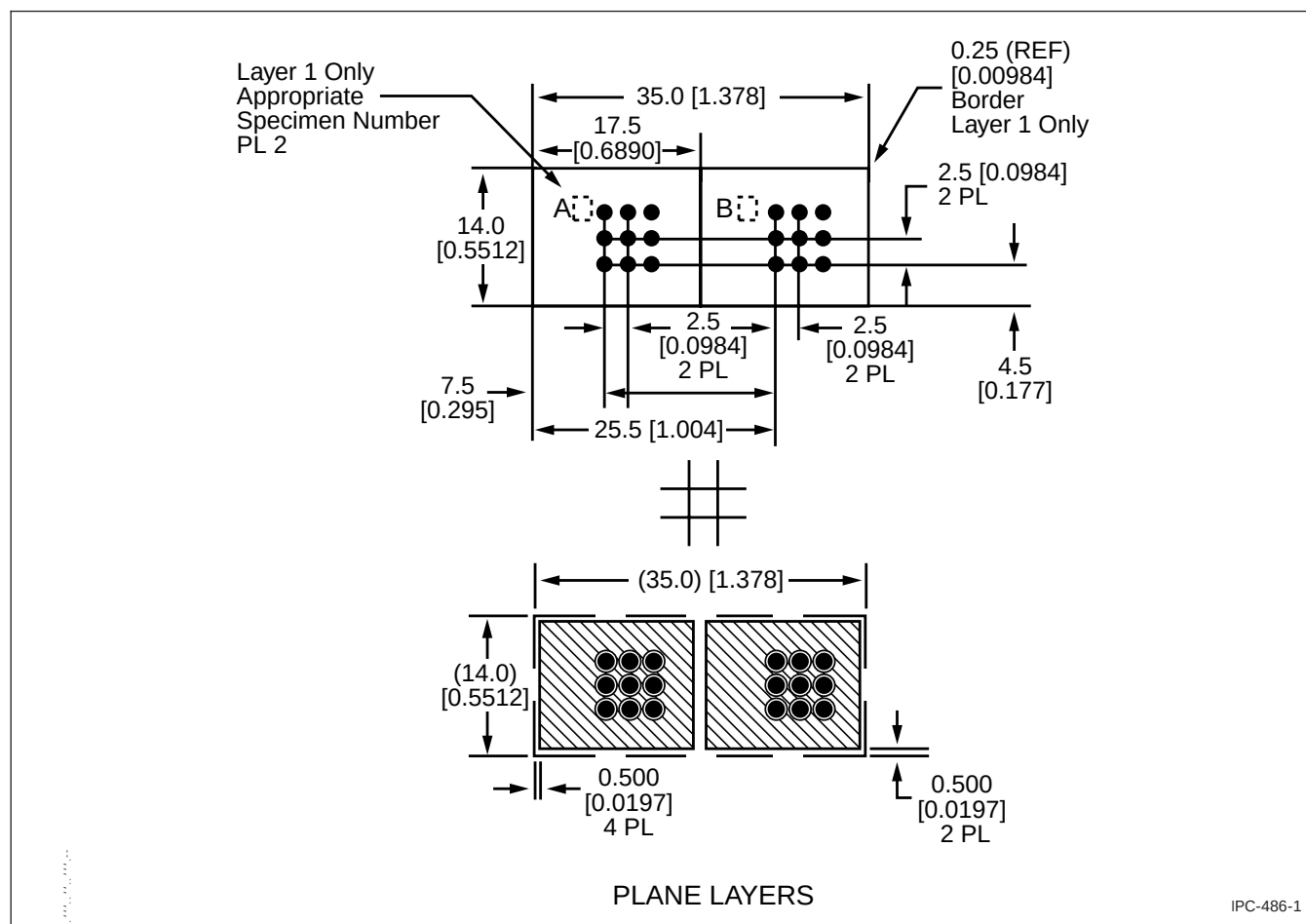


Figure 1 Layout of Thermal Stress Coupons, mm [in]

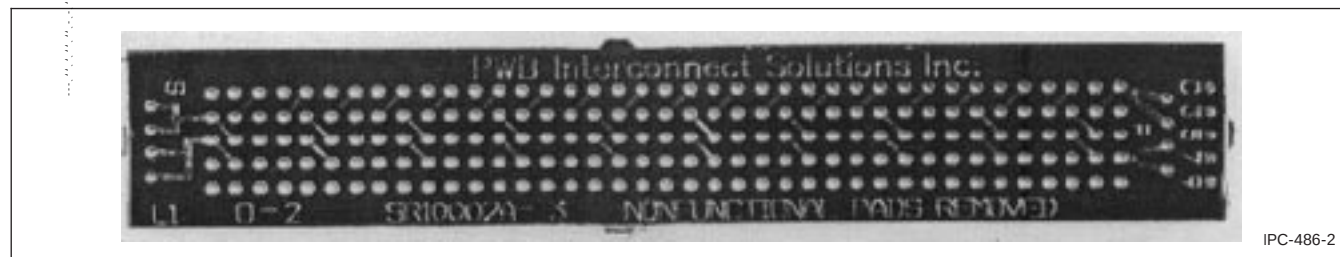


Figure 2 Photograph of IST Coupon

SECTION 4 — TESTS

The data requested on each coupon for both tests was “YES” or “NO” as to the presence of inner-layer separation. This was done because current specifications allow no inner-layer separations for class 2 or class 3 product.

THERMAL STRESS/MICROSECTIONING

Thermal Stress testing is the standard test used by the industry to measure the ability of printed board products to withstand soldering operations during assembly. It has been the standard test for over 25 years. This test requires a preconditioning bake followed by floating the sample on solder and then finally followed by microsectioning.

The Thermal Stress test was performed per IPC-TM-650, Method 2.6.8. (Appendix A)

Preconditioning bake:	6 hours - 0, + hour at 121°C - 149°C [250°C - 300°F]
Solder temperature:	288°C [550°F]
Float time:	10 seconds

Following Thermal Stress exposure, the coupons were microsectioned and evaluated. Each lab was allowed to use their own microsectioning process. This was done in order to capture typical results from a sample set based on the criteria used by each test site lab in daily testing of product.

Testers were requested to submit the results listing each coupon and a “YES” or “NO” to indicate whether inner-layer separation was present.

IST

Interconnect Stress Test (IST) testing was performed per IPC-TM-650, Method 2.6.26. (Appendix B)

Simulated assembly exposures prior to cycling:	None
Heat cycle time:	3-minute
High test temperature:	150°C [302°F]
Cool cycle time:	2 minutes
Low test temperature:	Ambient
Maximum number of cycles:	150
Limit on bulk resistance change:	2% maximum

The test conditions deviate from “typical” IST test conditions in the following:

1. The coupons were cycled to 150 cycles instead of to failure.
2. The failure criteria of 2% resistance change is lower than the more common 10% resistance change.
3. The test results had to be reported in YES or NO format.

The 2% was defined as inner-layer separation for the purpose of this round robin. The 2% value is arbitrary and the IPC 6-10c PTV Reliability Task Group is tasked to determine what percent change is significant for performance acceptance.

Each IST test site was allowed to use their normal IST coupon preparation, defect location after IST testing, and microsectioning procedures. The parameters for the test equipment were the same for the differing hardware configurations and test site locations (United States, Canada, and Germany). This was done in order to capture typical results from a sample set based on the criteria used by each test site lab in typical testing of product.

While the actual test plan called for 150 cycles, some test sites cycled their coupons longer than 150 IST cycles. This was done to assure that the results reported at 150 cycles represented the true quality of the coupons.

All IST test sites were to microsection failures to confirm the presence of inner-layer separations. When the test coupons were not cycled to failure no microsectioning was performed, therefore no photographs were available.

Typical IST graphs are shown in Appendix E.

SECTION 5 — RESULTS

The number of individual data points generated by this round robin was very large - 10 testers x 2 board manufacturers x 24 panels x 3 coupons per panel = 1440 test points. It became evident when examining the entire data set that it would be necessary to separate the data sets from Manufacturer A and Manufacturer B and each expected level of inner-layer separation. Therefore the following sections will separately address each board manufacturer and expected level of inner-layer separation.

The testers were requested to submit data on each coupon tested as “YES” or “NO” as to the presence of inner-layer separation. This was done because current IPC-6010 series performance standards do not allow inner-layer separations for Class 2 or Class 3 product. An instance of an “x” within the tabular results of this technical report indicates that no data was available for that coupon or tester.

TESTER IDENTIFICATION

The five Thermal Stress/microsection labs were assigned identifications of XLAB1 - XLAB5. The five IST testers were assigned identifications of IST1 - IST5.

SET A1 RESULTS (MANUFACTURER A, “GROSS” INNER-LAYER SEPARATION EXPECTED)

Set A1 was identified by the board manufacturer to likely have the most severe inner-layer separation after a soldering process.

One microsection lab failed to detect inner-layer separation on three coupons from two different panels. There were no IST testers that failed to detect inner-layer separation in all samples tested.

The agreement for the XLAB testers was 100% for the “large,” 95% for the “medium,” and 89% for the “small” diameter plated-through holes.

The agreement for the IST testers was 100% for all plated-through hole diameters.

The photographs in this technical report show the severity of the inner-layer separations present in this set of samples. It would appear that the failure to consistently detect inner-layer separation by Thermal Stress/microsection testing might be due to the randomness of the defect and not the microsectioning technique itself.

The cross-correlation agreement between the XLAB and IST testers was 100% for the “large,” 97% for the “medium,” and 94% for the “small” plated-through holes.

For “gross” inner-layer separation, as exhibited by Set A1, the Thermal Stress and IST results are in excellent agreement.

See Figure 3 for an instance of a typical A1 PTV following Thermal Stress.

See Figure 4A and Figure 4B for instances of typical A1 PTV following IST.

THERMAL STRESS

PANEL	HOLE SIZE		XLAB1	XLAB2	XLAB3	XLAB4	XLAB5
1	0.34 mm [0.0135 in]	"small"	YES	NO	YES	YES	X
1	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
1	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES
2	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES
2	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
2	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES
3	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES
3	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
3	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES
4	0.34 mm [0.0135 in]	"small"	YES	NO	YES	YES	YES
4	0.71 mm [0.028 in]	"medium"	YES	NO	YES	YES	YES
4	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES

The overall correlation between XLABS is 95%. [56 YES/59 data=95%; 20/20 "large"=100% for "large;" 19/20 "medium"=95% for "medium;" 17/19 "small"=89% for "small."]

IST

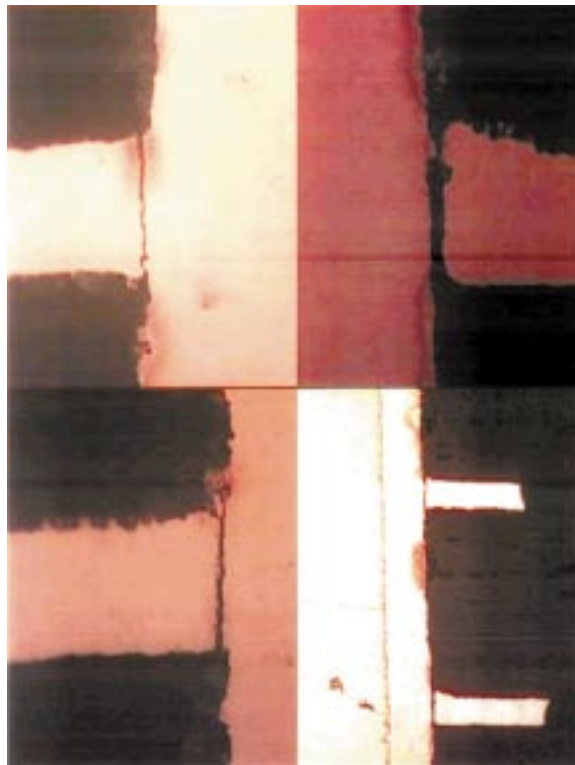
PANEL	HOLE SIZE		IST1	IST2	IST3	IST4	IST5
1	0.34 mm [0.0135 in]	"small"	YES	YES	YES	X	YES
1	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
1	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES
2	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES
2	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
2	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES
3	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES
3	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES
3	1.2 mm [0.0465 in]	"large"	X	YES	YES	YES	YES
4	0.34 mm [0.0135 in]	"small"	X	YES	X	YES	YES
4	0.71 mm [0.028 in]	"medium"	X	YES	X	YES	YES
4	1.2 mm [0.0465 in]	"large"	X	YES	X	YES	YES

Correlation between IST testers is 100%.

BOARD MANUFACTURER A

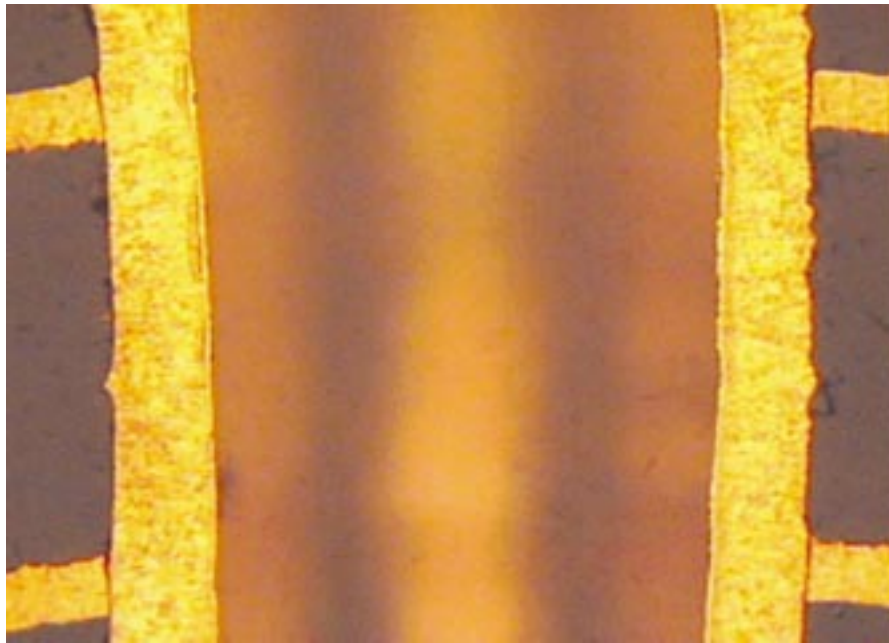
PANEL	HOLE SIZE		XLAB1	XLAB2	XLAB3	XLAB4	XLAB5	IST1	IST2	IST3	IST4	IST5
1	0.34 mm [0.0135 in]	"small"	YES	NO	YES	YES	X	YES	YES	YES	X	YES
1	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
1	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
2	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
2	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
2	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
3	0.34 mm [0.0135 in]	"small"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
3	0.71 mm [0.028 in]	"medium"	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
3	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES	X	YES	YES	YES	YES
4	0.34 mm [0.0135 in]	"small"	YES	NO	YES	YES	YES	X	YES	X	YES	YES
4	0.71 mm [0.028 in]	"medium"	YES	NO	YES	YES	YES	X	YES	X	YES	YES
4	1.2 mm [0.0465 in]	"large"	YES	YES	YES	YES	YES	X	YES	X	YES	YES

The overall cross-correlation between XLABS and IST testers 97%. [108 YES/111 data=97%; 37/37 "large"=100% for "large;" 37/38 "medium"=97% for "medium;" 34/36 "small"=94% for "small."]

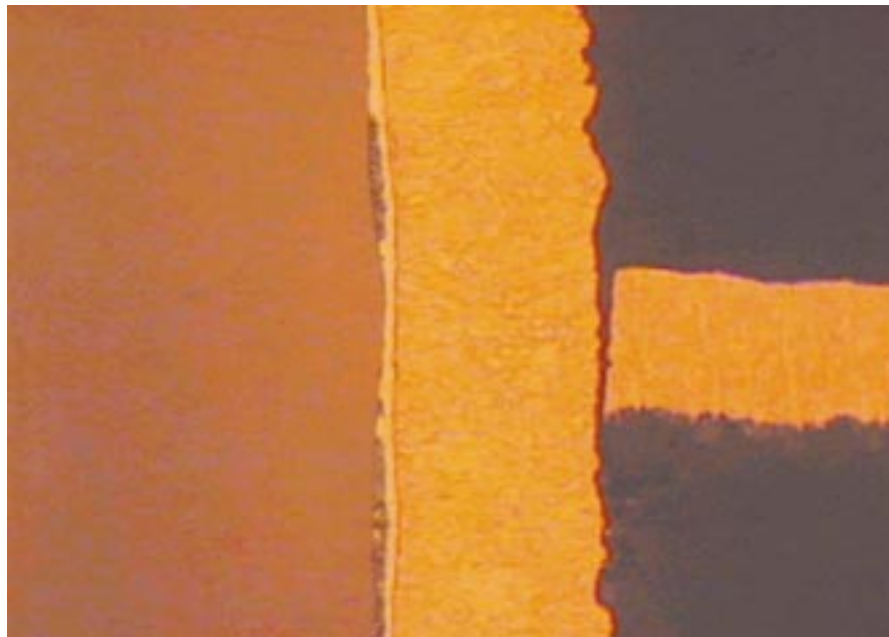


IPC-486-3

Figure 3 Photograph of Typical A1 PTV after Thermal Stress



IPC-486-4a

Figure 4a Photograph of Typical A1 PTV after IST

IPC-486-4b

Figure 4b Photograph of Typical A1 PTV after IST