



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-TR-585

Time, Temperature and Humidity Stress of Final Board Finish Solderability

IPC-TR-585

May 2006

A standard developed by IPC

3000 Lakeside Drive, Suite 309S, Bannockburn, IL 60015-1219

Tel. 847.615.7100 Fax 847.615.7101
www.ipc.org



Documents

Document Sharing Hub

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-TR-585

Time, Temperature and Humidity Stress of Final Board Finish Solderability

Developed by the Alternate Final Finishes Task Group (5-23d) of the
Assembly & Joining Processes Committee (5-20) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1219
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Alternate Final Finishes Task Group (5-23d) of the Assembly & Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Assembly & Joining Processes Committee	Alternate Final Finishes Task Group	Technical Liaisons of the IPC Board of Directors
Chair Leo P. Lambert EPTAC Corporation	Chair Dennis Fritz MacDermid, Incorporated Vice Chair David D. Hillman Rockwell Collins	Peter Bigelow IMI Inc. Sammy Yi Flextronics International
Alternate Final Finishes Task Group		
David C. Adams, Rockwell Collins Sean M. Adams, BOC Gases Richard Arnold, Motorola Inc. Gail Auyeung, Celestica International Inc. Gregory S. Bartlett, Teledyne Electronic Technologies John A. Bauer, Rockwell Collins Martin W. Bayes, Rohm and Haas Electronic Materials James D. Bielick, IBM Corporation David Boggs, Intel Corporation Leroy Boone, Thomson Consumer Electronics Peter Bratin, ECI Technology, Inc. Mark Buechner, BAE Systems Lee Burger, Electrochemicals Inc. Fritz R. Byle, Plexus NPI Plus Thomas A. Carroll, Boeing Space Systems Peter Marc Carter, Rockwell Collins Alan S. Cash, Northrop Grumman Corporation Srinivas Chada, Ph.D, Medtronic Microelectronics Center Phillip Chen, L-3 Communications Electronic Systems Beverley Christian, Ph.D., Research In Motion Limited Quyen Chu, Jabil Circuit, Inc.	Christine R. Coapman, Delphi Electronics and Safety Miguel A. Contreras, Pulse Engineering David J. Corbett, Defense Supply Center Columbus Donald P. Cullen, MacDermid, Inc. Charles Dal Currier, Ambitech Inc. Gordon Davy, Northrop Grumman Corporation Glenn Dody, Dody Consulting Kantesh Doss, Ph.D., Intel Corporation Hugh E. Downs, C.I.T., H. Downs Consultants Inc. Raymond L. DuBois, Teledyne Electronic Technologies Richard M. Edgar, FCT Assembly, Inc. Theodore Edwards, Dynaco Corp. Werner Engelmaier, Engelmaier Associates, L.C. Jing Li Fang, Taiwan Uyemura Co. Ltd. Thomas G. Farrell, Underwriters Labs Inc. Herbert J. Fick, The Bergquist Company, Prescott Robert G. Furrow, Lucent Technologies Inc. Mahendra S. Gandhi, Northrop Grumman Space Technology	Frank W. Gayle, NIST Jack Geibig, University of Tennessee Reza Ghaffarian, Ph.D., Jet Propulsion Laboratory Andrew Giamis, Andrew Corporation Hue T. Green, Lockheed Martin Space Systems Company Michael R. Green, Lockheed Martin Space Systems Company Donald Gudeczauskas, UIC/Uyemura International Corp. Carol A. Handwerker, Sc.D., Purdue University William Holden, Rockwell Collins David H. Hoover, Multek Hana Hsu, Mitac International Corporation Christopher Hunt, Ph.D., National Physical Laboratory Jennie S. Hwang, Asahi Technologies America, Inc Kim Hyland, Solelectron Corporation Neeta Jayaraman, Amphenol TCS Kuldip Johal, Atotech USA Inc. Alden C. Johnson, Speedline Technologies, Inc. Raghu Kacker, NIST Roy M. Keen, Rockwell Collins Cheryl Keenan, ABT Associates Thomas E. Kemp, Rockwell Collins



Frank N. Kimmey, C.I.D.+, PowerWave Technologies, Inc.	Benny Nilsson, Ericsson AB	Joseph T. Slanina, Honeywell Inc.
Vincent B. Kinol, Umicore America Inc.	Gerard A. O'Brien, Photocircuits Corporation	Valerie A. St. Cyr, Teradyne Inc.
Jeffrey F. Koon, Raytheon Company	David H. Ormerod, Enthone Inc. - Cookson Electronics	Eric Straw, Rockwell Collins
Richard E. Kraszewski, Kimball Electronics	Mel Parrish, STI Electronics, Inc.	Daniel R. Tetter, Hughes Network Systems
Fred Kuhlman, Delphi Electronics and Safety	Douglas O. Pauls, Rockwell Collins	Dung Q. Tiet, Lockheed Martin Space Systems Company
Mark A. Kwoka, Intersil Corporation	Michael Pavlov, ECI Technology, Inc.	Michael Toben, Rohm and Haas Electronic Materials
Leo P. Lambert, EPTAC Corporation	Timothy M. Pitsch, Plexus Corp.	John E. Tobin, Underwriters Laboratories Inc.
Anthony W. Lentz, FCT Assembly, Inc.	John W. Porter, Multicore Solders Ltd.	Brian J. Toleno, Ph.D., Henkel Corporation
Boen Li, Photocircuits Corporation	Richard Prendergast, Enthone Inc. - Cookson Electronics	Lenora M. Toscano, MacDermid, Inc.
Deson Lin, Taiwan Uyemura Co. Ltd.	Guy M. Ramsey, R & D Assembly	Crystal E. Vanderpan, Underwriters Laboratories Inc.
Nimal Liyanage, Ph.D., Metallic Resources Inc.	Urmi Ray, Pulse Engineering	William Lee Vroom, Thomson Consumer Electronics
Gary B. Long, Intel Corporation	Jim R. Reed, Dell Inc.	Karen Walters Ebner, Raytheon Company
James F. Maguire, Intel Corporation	Randolph S. Robinson, Raytheon Missile Systems	Malcolm Warwick, Multicore Solders Ltd.
Wesley R. Malewicz, Draeger Medical Systems, Inc.	David Rooke, Research In Motion Limited	Nicholas R. Watts, Intel Corporation
Alfred Mangu, BAE Systems	Gary C. Roper, One Source Group	Michael Weekes, Sopark Corporation
John R. Manning, NIST	William R. Russell, Raytheon Systems Company	Karl F. Wengenroth, Enthone Inc. - Cookson Electronics
Rene R. Martinez, Northrop Grumman Space Technology	Amit Sarkhel, Ph.D., Raytheon Company	George M. Wenger, Andrew Corporation
Tracy Meixensperger, Hewlett-Packard Company	Karl A. Sauter, Sun Microsystems Inc.	Vicka White, Honeywell Inc.
Nicholas C. Mescia, Nanolytics Inc.	David Sbiroli, Indium Corporation of America	Keith J. Whitlaw, Rohm and Haas Electronic Materials
Renee J. Michalkiewicz, Trace Laboratories - East	Hans Jurgan Schreier, Atotech Deutschland GmbH	Dewey Whittaker, Honeywell Inc.
George Milad, UIC/Uyemura International Corp.	Douglas R. Schueller, AbelConn, LLC	Maureen Williams, NIST
Danny Miller, Raytheon System Technology	Tom Scimeca, Ph.D., FCT Assembly, Inc.	Philip W. Wittmer, Delphi Electronics and Safety
Kil-Won Moon, Ph.D., NIST	Eric Timothy Seabaugh, Multek Flexible Circuits, Inc.	Thomas A. Woodrow, Ph.D., The Boeing Company
Kirk D. Mueller, Raytheon Company	Andrew Seman, Endicott Interconnect Technologies Inc	Fonda B. Wu, Raytheon Company
Terry L. Munson, Foresite, Inc.	Jeff Shubrooks, Raytheon Company	Mitchell Wu, Compeq Manufacturing Co. Ltd.
David R. Nelson, Raytheon Company	Dipti Singh, U.S. Environmental Protection Agency	Michael W. Yuen, Foxconn EMS, Inc.
Gary Nicholls, Enthone Inc. - Cookson Electronics		
Marvin Nilson, Telex Communications		

Table of Contents

1 PURPOSE	1	Appendix 4: “Stop Light” Analyses of Wetting Balance Data	25
2 INTRODUCTION	1	Appendix 5: Relative Stoplight and Box-and-Whisker Analysis of SERA Data	27
3 TASK OBJECTIVES	1	Appendix 6: Solderability Visual Exam	33
4 TEST PLAN	1	Appendix 7: Statement of Work for This Project at the Start	34
5 SAMPLE PREPARATION	2	Appendix 8: IPC Dip and Look Test Method	39
6 SURFACE ANALYSIS OF SAMPLES	3	Appendix 9: Further Analysis of the Alternate Final Finishes Task Group Report on Time, Temperature and Humidity Stress of Final Board Finish Solderability	41
7 SAMPLE CONDITIONING (COUPON CONDITIONING)	4		
8 SAMPLE TESTING	4	Figures	
8.1 Wetting Balance Testing	4	Figure 4-1 Box Behnken Test Design	1
8.2 Sequential Electrochemical Reduction Analysis (SERA) Testing	5	Figure 5-1 ENIG Coupons Before Plating	3
8.3 Dip and Look Testing	5	Figure 6-1 Cross Sections of Six “As Fabricated” Alternative Surface Finishes”	4
8.4 Wetting Balance Testing	5	Figure 7-1 Immersion Silver Coupons after Conditioning	4
8.5 SERA Testing	5	Figure 8-1 Alternative Surface Finishes after Dip and Look Solderability Testing	6
9 DATA ANALYSIS	7	Figure 8-2 Cross Section of Alternative Surface Finish Coupons After Dip and Look Solderability Testing	6
9.1 Wetting Balance Results	7	Figure 8-3 Schematic of SERA Apparatus	7
9.2 Visual	8	Figure 8-4 Typical SERA Plot	7
10 CONCLUSIONS		Figure 9-1 Sample Box and Whisker Plot from Data Taken from Reflowed Tin Lead	8
10.1 Conclusions By Finish	8	Figure 10-1 Results from Gold Thickness Survey of IPC 4-14 Subcommittee that wrote IPC-4552	9
10.1.1 Bare Copper	8	Figure 10-2 Wetting Balance Coupon (FR-4, 0.062 in thick, acid copper plated, six 3 mm SMD pads/side)	9
10.1.2 RTL	8	Figure 10-3 Confirmation Run 8 Hour Test Results	9
10.1.3 Immersion Silver	8	Figure 10-4 Confirmation Run 24 Hour Test Results	10
10.1.4 Immersion Tin	8		
10.1.5 Electroless Nickel/Immersion Gold (ENIG)	8	Tables	
10.1.6 OSP	9	Table 4-1 Test Plan	2
10.2 Investigation Confirmation Testing	9	Table 5-1 Coupons and Sources	2
11 RECOMMENDATIONS	10	Table 6-1 Comparison of XRF and Auger Measurements	3
Appendix 1: Coupon Numbering System	11	Table 8-1 Oxide Reduction Potentials	7
Appendix 2 A: Charts for Reflowed Tin Lead	12	Table 8-2 Oxide Thickness Calculation	7
Appendix 2 B: Charts for Bare Copper	13	Table 10-1 Means and Standard Deviations for Figure 10-1	9
Appendix 2 C: Charts for Immersion Silver	14		
Appendix 2 D: Charts for Immersion Tin	15		
Appendix 2 E: Charts for Nickel Gold	16		
Appendix 2 F: Charts for OSP	17		
Appendix 3: Pareto Chart Analysis	18		

This Page Intentionally Left Blank

Time, Temperature and Humidity Stress of Final Board Finish Solderability

1 PURPOSE

The purpose of this investigation is to identify a stress test that will distinguish between robust and non-robust finishes. A robust finish will pass a test for solderability, and a non robust finish will fail. The stress test need not duplicate real world environment (fabrication through assembly), but it must correlate to solderability performance.

2 INTRODUCTION

The IPC 5-23d - Alternate Final Board Finishes Task Group is organized under the IPC Assembly and Joining Committee. Alternate Final Board Finishes Task Group activity began in the mid 1990s under IPC 5-23 Solderability Subcommittee. Surface mount technology was rapidly replacing through-hole construction. Planar surfaces, better than reflowed solder or hot-air-solder-level (HASL), were required. Originally, IPC standards for solderability testing were written around tin/lead surfaces only. It was proposed by committee participants that a whole new standard would be needed for testing the solderability of these new final board finishes.

Adjustments to the J-STD-003 specification allowed for the testing of board finishes other than tin lead. Therefore, committee attention turned to the measurement of stress effects of temperature, humidity, and time on alternative board finishes as measured by a variety of test methods. In addition, the committee tested the finishes with a promising newer technique - Sequential Electrochemical Reduction Analysis (SERA).

The potential exists to use this stress test data as a quality control tool and, perhaps, with correlation to observed individual situation data - to serve as a guideline for board storage or shelf life.

As board assembly facilities are located in various climate conditions, and board storage varies from company to company, no general guidelines can be given. However, to correlate to individual company conditions, a better understanding of alternate finish response to stress can be useful in product planning and supply chain management.

3 TASK OBJECTIVES

The objective of this test program is to determine a relationship between the three environmental stress conditions - temperature, moisture, and time - and the solderability of four alternate final board finishes. Two baseline conditions were used for comparison:

- Reflowed tin/lead electroplate (RTL)

- Bare copper (BC) - sometimes called “nude” copper referring to the “as plated” condition, not the “bare copper” of foil on circuit boards in shipment.

Four alternate finishes were selected - all of which have been used to assemble circuit boards for several years now.

- Organic solderability preservative (OSP)
- Immersion Silver (IS)
- Immersion Tin (IT)
- Electroless Nickel/Immersion Gold (ENIG - within this report the designation NG may be used)

Also the committee is trying to develop a model which can be used to:

- Determine screening test conditions to assess board solderability during production.
- Evaluate solderability process capability for five given surface finishes, plus bare copper baseline.
- Develop a method to evaluate potential new alternative surface finishes and compare predicted solderability performance to current finishes (terminology such as “aging” is not used in deference to “stressing”). For example “steam stressing” is preferred to “steam aging”).

4 TEST PLAN

A test plan was developed in order to investigate various surface stresses on surface finishes. This test plan evolved into a designed experiment approach that allowed investigation of many factors with minimal experimentation. The DOE design was a Box Behnken model (Figure 4-1).

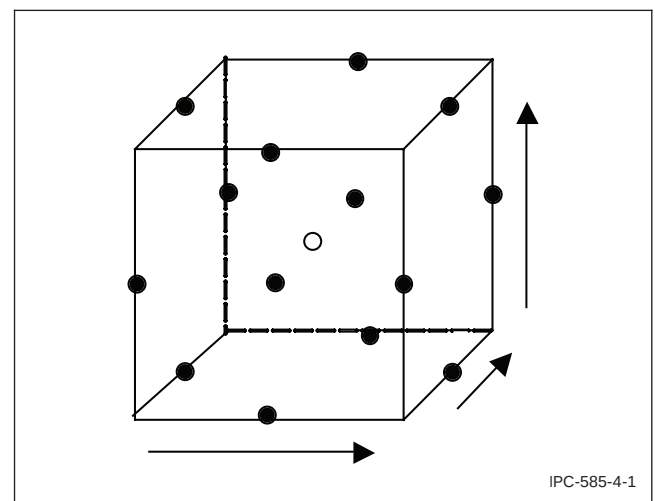


Figure 4-1 Box Behnken Test Design

The Box-Behnken design is an efficient and frequently used test matrix for modeling processes where non-linear effects may be present and all factors are quantitative. The design is a fractional factorial type with a nearly orthogonal matrix, testing each factor at three levels. This allows us to include quadratic terms in the model. The full test matrix is shown in Table 4-1 below. Another feature of the matrix can be seen in Figure 1. The three factors to be tested are shown as the X, Y, and Z axes of the design space. The geometric locations of the test points are then charted. Notice that the Box-Behnken design tests the center of the design space and the center of each edge.

Table 4-1 Test Plan

Run	Temp. (Deg C)	RH (%)	Time (hr)
1	25	25	0
2	50	30	504
3	95	30	504
4	50	95	504
5	95	95	504
6	50	62.5	8
7	95	62.5	8
8	50	62.5	1000
9	95	62.5	1000
10	72.5	30	8
11	72.5	95	8
12	72.5	30	1000
13	72.5	95	1000
14	72.5	62.5	504
15	72.5	62.5	504
16	72.5	62.5	504
17	72.5	62.5	504
18	72.5	62.5	504
19	95	62.5	504

This spherical arrangement allows an adequate quadratic model to be estimated but also avoids the corners of the design space, where factors are at their most extreme values. Test runs at combinations of extreme values often pose conditions that are difficult to maintain, or are infeasible. The Box-Behnken design allows for estimating the effects of all linear effects, two-way interactions and quadratic terms. It does not allow for estimation of quadratic interactions or the three-way linear interaction.

Methodology

- Obtain a model with quadratic terms on quantitative factors by using a fraction of a full factorial
- DOE chosen allows determination of all main effects, two way interactions, and quadratics
 - Avoids the corners of the design space
 - Only useful for 3 or 4 factors

• Conditions chosen:

- Time (0, 8, 504, 1000 hours)
- Temp (50, 72.5, 95C)
- RH (30, 62.5, 95%)

The output variables were derived from wetting balance, SERA and dip-and-look testing. Only two testing sites were used in this investigation.

One tester used “Dip and Look” methodology from the J-STD-003 to judge the finishes on the test coupons. A second tester used wetting balance methodology from J-STD-003.

SERA testing was also conducted by the second tester to characterize the surfaces of the test finishes. The wetting balance tester also inspected the coupons after wetting balance testing for solder wetting characteristics.

Output variable terms:

Wetting Balance

- (T_0) = Time to zero force
- ($T_{2/3}$) = Time to 2/3 max force
- (F_{max}) = Maximum force
- (F_2) = Force at 2 seconds, where data available.

SERA Measurements

- V2 - The voltage at which the metal oxide is being reduced
- Vf - The final voltage of the specimen.

Dip and Look Visual Inspection

- 95% coverage

5 SAMPLE PREPARATION

Test Coupon

The test coupon selected for the DOE was an Oxygen-Free High Conductivity (OFHC) C101 copper coupon, one inch wide by two inches in length, with a thickness of 0.027 inches. Approximately 0.5 mil of electroplated acid copper was deposited on the coupons to simulate the plating conditions used in fabrication of printed circuit boards. Table 5-1 lists the various surface finishes used in the DOE and the companies who provided them.

Table 5-1 Coupons and Sources

Surface Finish	Company Supplying Finish
ENIG	Delphi
Immersion Tin	Plating Chemistry Supplier
Immersion Silver	Delphi
OSP	Delphi
Bare Copper	Raytheon
Reflowed Tin/Lead	Raytheon

The various surface finishes were applied to the coupons using 18” x 12” coupon panels. There were 40 coupons in each panel. Figure 5-1 illustrates a set of 5 ENIG coupons.

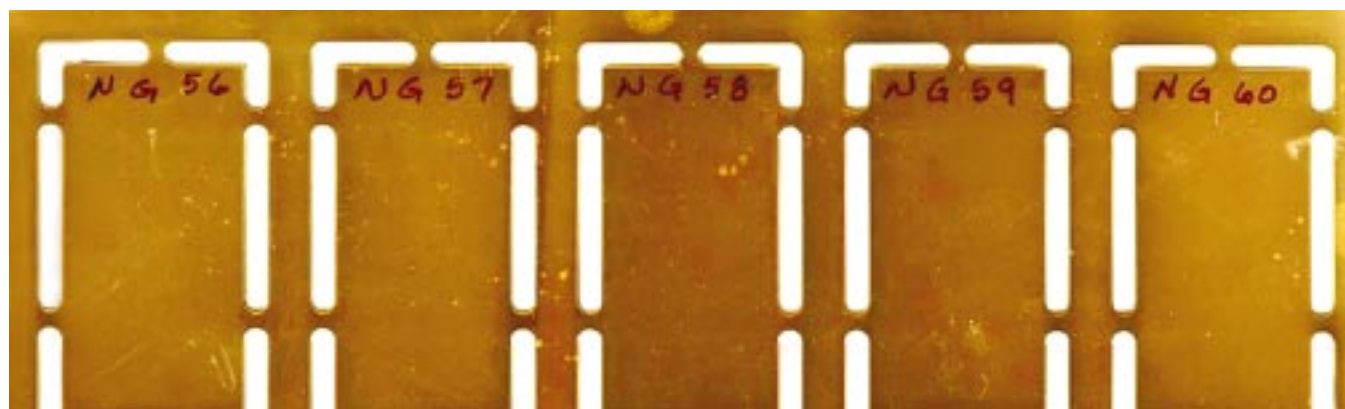


Figure 5-1 ENIG Coupons Before Plating

6 SURFACE ANALYSIS OF SAMPLES

The surface finish thickness on one “as-fabricated” sample from each type of coupon was measured using X-Ray Fluorescence (XRF). Surface finish thickness was measured using an XRF equipped with a 3 mil by 3 mil collimator. Six hundred measurements (i.e., a 40 by 15 matrix across each surface) were made on the top and bottom surfaces of each coupon. Frequency distributions of the XRF thickness measurements showed typical characteristics of these commercially available surface finishes.

Scanning Auger microprobe surface analysis and depth profiling was performed on a portion of each coupon. Auger depth profiling was performed to verify the surface finish thickness measurements and determine surface contamination. Table 6-1 gives a comparison of the XRF thickness measurements to the Auger depth profiling results. They are in good agreement.

Table 6-1 Comparison of XRF and Auger Measurements

Surface Finish	XRF Measurements		Auger Measurements	
	Thickness or Composition	Standard Deviation	Thickness or Composition	Standard Deviation
RTL	62% Sn		61% Sn	
IS	1.5 μin	(0.7)	1.8 μin	(0.3)
IIT	19.0 μin	(2.7)	19.0	(1.0)
NG	3.9 $\mu\text{in Au}$	(0.4)	3.0 $\mu\text{in Au}$	(0.2)
OSP	N/A		7.0 μin	

The Auger analysis determined the Electroless Nickel to contain 7 wt.% phosphorus (P). The Auger analysis also found that the immersion tin finish was the one finish that appeared to have significant surface contamination. It had a surface oxide layer and there was Cu both on the surface and throughout the immersion tin layer.

Cross sections of the baseline coupons as well as scanning electron microscopy (SEM) pictures and energy dispersive

x-ray (EDX) scans showed the structure of the solder on the reflowed tin/lead coupon has a “typical” solder appearance. The solder is approximately 8 microns [320 μin] thick and has a copper-tin intermetallic approximately 1 micron [40 μin] thick at the electrolytic copper interface. Although the EDX analysis indicates that there is silver (Ag) on the surface of the immersion silver coupon, it is difficult to obtain an accurate thickness measurement from the cross section, because the deposit is so thin. The SEM image of the immersion silver cross section showed the immersion silver to be approximately 1 micron [40 μin] thick. The electroless nickel/immersion gold plating was approximately 4 microns [160 μin] thick and the electroless nickel/immersion gold was approximately 0.14 microns [5.6 μin] thick.

The thickness values obtained from the cross sections are greater than from the XRF or Auger measurements. This is due to the inability of the metallurgical cross sectioning to maintain the integrity of the edge of the plating, without additional overplating with nickel. Cross sectional analysis showed no discernible difference between the OSP coupon and the Bare Cu coupon. Cross sections of the “as-fabricated” coupons are presented in Figure 6-1. The cross section of the Bare Copper coupon shows that the OFHC copper base metal was electrolytic plated with about 1.1 mils of acid copper. The reason the acid copper is a few tenths of a mil thinner on the other coupons is because the coupons were microetched before application of the final surface finish.

The preliminary characterization of the “as-fabricated” coupons confirmed that the surface finishes on the coupons used for the alternative surface finish stressing evaluation were typical of the commercially available finishes currently being used in the industry at that time.



Figure 6-1 Cross Sections of Six "As Fabricated" Alternative Surface Finishes"

7 SAMPLE CONDITIONING (COUPON CONDITIONING)

The coupons were conditioned per the DOE parameters listed previously in Table 4-1. All coupons were conditioned using an Espec PRA-2AP temperature/humidity chamber. The humidity was controlled within a tolerance of $\pm 2.5\%RH$ and the temperature was controlled within a tolerance of $\pm 3^{\circ}C$. Upon completion of a conditioning cycle the coupons were allowed to air dry for 15 minutes, labeled, photographed, and sealed in Kapak bags backfilled with ultra-pure dry nitrogen. The coupons were then shipped overnight to the test site for wetting balance and SERA testing. The bagged coupons were placed in a dry

nitrogen atmosphere box until testing was conducted. Changes in coupon appearance were documented. In general, the higher the temperature and humidity parameters, the greater tendency for changes in the coupon appearance were observed. Figure 7-1 illustrates the immersion silver coupon appearance after being subjected to 95%RH/95°C for 504 hours.

8 SAMPLE TESTING

8.1 Wetting Balance Testing As this test program began in 1999, correlation of wetting balances through several



Figure 7-1 Immersion Silver Coupons after Conditioning

rounds of Gage R&R testing had been done. Wetting balance of solid copper coupons was an accepted instrumental method to give numerical values for solderability. Test correlation between environmental variables and numeric results was deemed highly desirable. To give assurance that the test was being done similar to some previous result, the solid copper coupons were selected. These were the same as those in the Wetting Balance Gage R&R testing, so the results for reflowed tin lead and bare copper should be similar to previous results. All wetting balance testing was done at a single site to minimize possible drift and error.

Methodology to Differentiate Solderability by Test Methods

By the time of the writing of this report, much more work has been done using wetting balance coupons made from actual circuit board epoxy glass substrates. The sensitivity of wetting balances has been improved. Also, much more work has been done on various alternate surface finishes to demonstrate process repeatability - resulting in process standards for applying these finishes.

The bulk of the data for this report was taken using test method 4.3.1 of J-STD-003 - Wetting Balance. Variables were:

- Time to zero force (T_0)
- Time to 2/3 max force ($T_{2/3}$)
- Maximum force (F_{max})
- Also, an attempt was made to add Force at 2 seconds to the matrix since many samples did not reach maximum force in the 5 seconds allowed on the wetting balance. Data for this measurement are incomplete as it was not recorded for all samples, so this attempt was abandoned.

8.2 Sequential Electrochemical Reduction Analysis (SERA) Testing SERA was tracked and compared to the dip-and-look and to the wetting balance results. SERA has the potential for quick instrumental readings, and is non-destructive on circuit boards.

V2 – plateau voltage which typically represents the major oxide species of interest for the metallic surface finish under test.

Vf – plateau voltage which typically represents reducibility of all oxide species of interest for the metallic surface finish under test.

8.3 Dip and Look Testing The Alternative Surface Final Board Finishes Task Group started conducting extensive wetting balance solderability tests on stressed coupons, as well as on non-stressed baseline coupons. To confirm instrument readings, it was decided that a manual Dip-&-Look solderability evaluation on portions of the baseline coupons should be made. Specimens approximately 0.5 inch square were sheared from each coupon. The specimens were fluxed with 25% solids water white rosin flux

and immersed to a depth of approximately 1/8 inch for 5 seconds in 235°C Sn60 solder. Photomicrographs of both sides of the solderability tested coupons are presented in Figure 8-1. With the exception of Bare Cu, the coupons soldered well. There are non-wet areas within the immersed portion of the Bare Cu coupon and there is no evidence of positive wetting. Although the ENIG sample passed the Dip-&-Look solderability requirements, the wetting height may be slightly less than the other samples. The solder wetting front also appears horizontal, rather than curved, like the rest of the samples. The other coupons exhibit the typical solder meniscus shape of lower contact on the ends of the coupons (i.e., corner effect). Care was used during solderability testing to insure the edge immersed was the “as-fabricated” edge and not the sheared portion of the coupons. Edge view cross sections of the Dip-&-Look solderability tested coupons are presented in Figure 8-2. These coupons show that the coupons were photochemically etched prior to acid copper plating.

8.4 Wetting Balance Testing Wetting balance data are included in the “box and whisker charts” presented in Appendix 2, A through F of this report. Massive amounts of data are rolled-up together and included in this Appendix 2, A through F.

The operating conditions for the wetting balance were as follows:

Type of Solder - 63/37
 5 mm flux dip
 solder - 245°C
 Clip 20 (MUST II)
 45 second dwell above pot (preheat)
 Speed 10 mm/sec
 Depth 3 mm
 5 sec duration

While the wetting balance does not immerse the coupons nearly as far and as long as IPC's dip and look test method (detailed in Appendix 8), nevertheless, a dip-and-look evaluation of the coupons after the wetting balance test was completed. Conclusions could be made about the appearance of such finishes as immersion silver and ENIG in that the immersion silver seemed to retain minimal solder, and the ENIG appeared to solder better than the wetting balance numbers indicated (see Appendix 6).

8.5 SERA Testing Sequential Electrochemical Reduction Analysis, or commonly referred to as SERA, is a surface analysis tool based on electrochemical techniques. The SERA method uses a small constant cathodic current that is applied to the oxidized surface in a deaerated electrolyte via an inert counter electrode. The cathode voltage versus a reference electrode is recorded as a function of time. A plot of cathode voltage versus charge density (current density x time) yields a characteristic curve. Grouping is

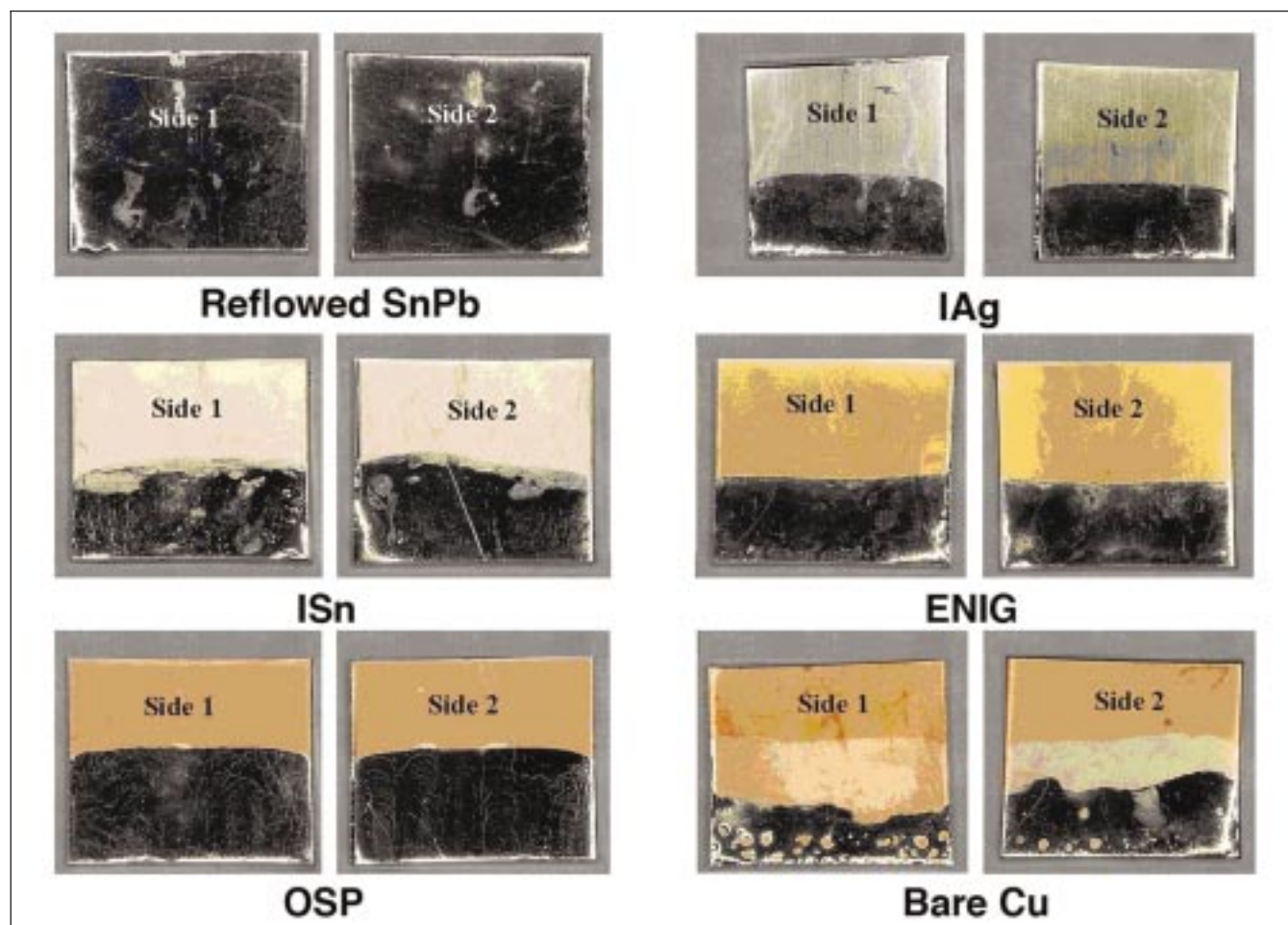


Figure 8-1 Alternative Surface Finishes after Dip and Look Solderability Testing

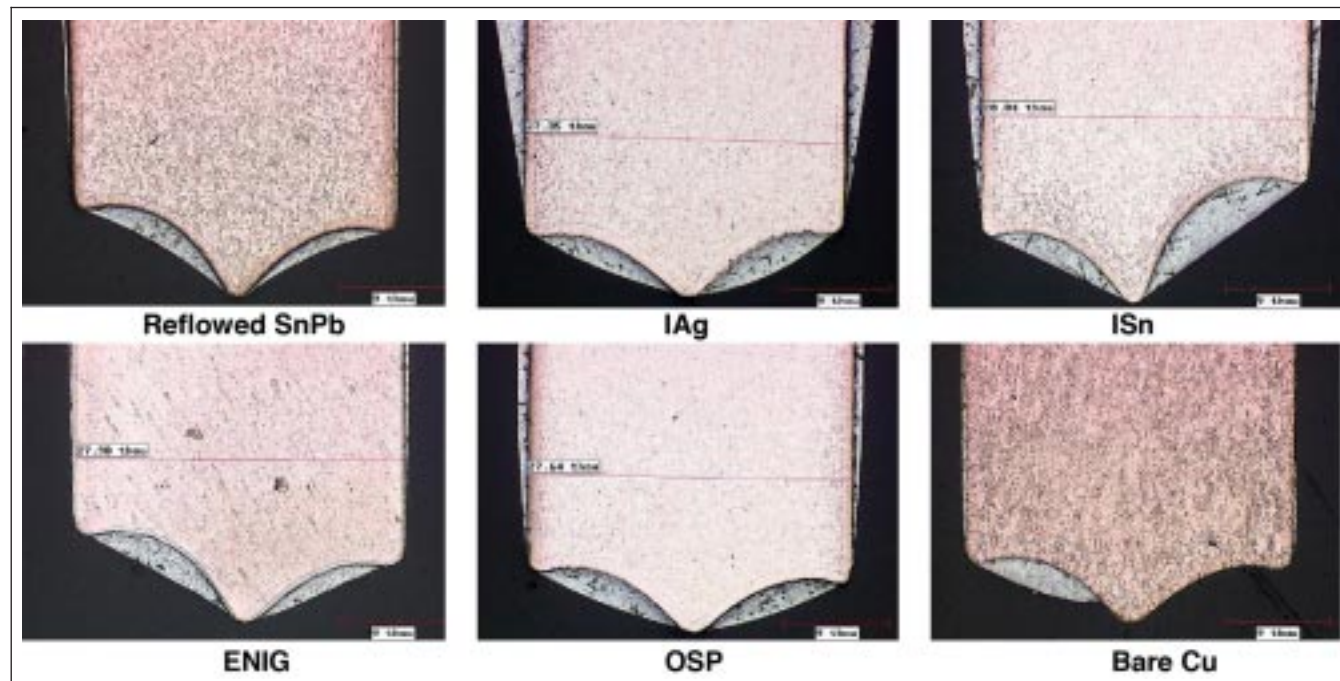


Figure 8-2 Cross Section of Alternative Surface Finish Coupons After Dip and Look Solderability Testing (Some samples show significant amount of adhering solid solder on surfaces after dipping)

sequential reduction of the oxides present on the surface of the sample. A plateau voltage level corresponds to the reduction of a specific species of oxide and the charge (i.e., the plateau width) passed is a measure of the thickness of that oxide present on the sample.

The SERA test electrolyte used is typically a borate buffer solution deaerated by continuous nitrogen gas sparging. A typical reduction current density of $-30 \mu\text{A}/\text{cm}^2$ is used for tin oxide measurements.

Figure 8-3 is a schematic diagram of the apparatus used to make the SERA measurements. The test head contained Viton O-rings (1.6 mm inside diameter) that formed a seal around the sample surface and defined a specific area of analysis. The system was purged with nitrogen and a deaerated borate buffer solution was drawn under partial vacuum from a reservoir, via a small Teflon tube, into contact with the sample surface. All apparatus parts in contact with the buffer solution were either glass, Teflon, or polypropylene except for the stainless steel electrodes. A computer was used to control the SERA tests and capture the test data.

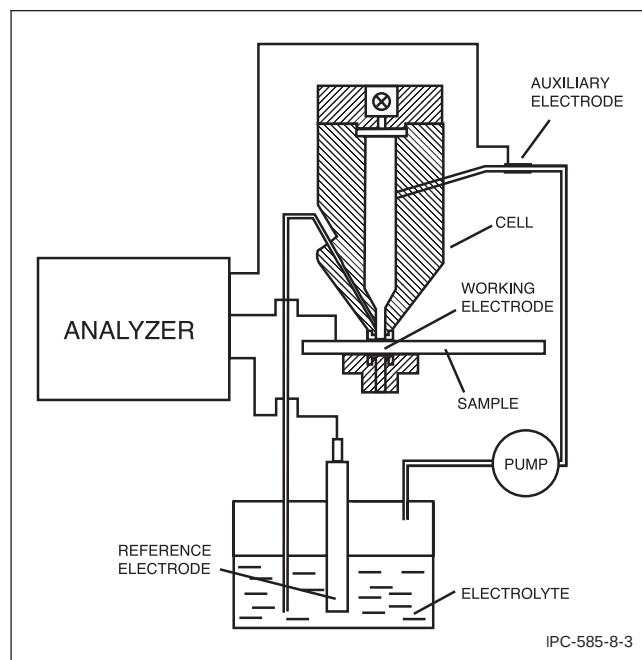


Figure 8-3 Schematic of SERA Apparatus

A representative SERA plot is illustrated in Figure 8-4. SERA analysis software analyzes the SERA data (electrode potential versus charge passed) via differentiation algorithms to determine inflection points. A simple approach to the SERA data interpretation is to look at the plateau potential, the duration of the plateau and the rate of transition between different plateaus. A plateau on the SERA curve corresponds to a specific reduction voltage and, therefore, a specific oxide species. The length of the plateau, measured as units of mC/cm^2 , is a measurement of the amount of that particular oxide species present. A test surface, comprised of well defined oxide species, will have

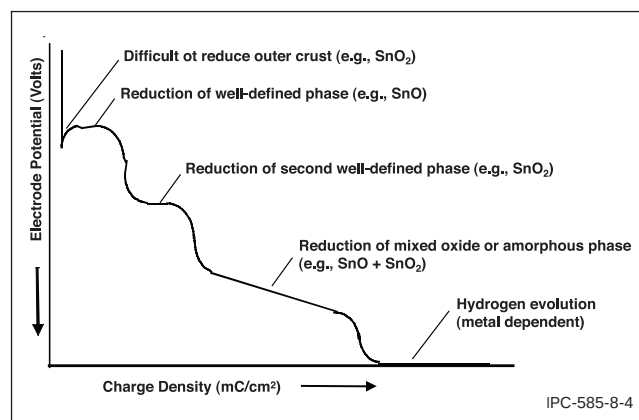


Figure 8-4 Typical SERA Plot

stable, level plateaus with sharp, distinct transitions between the plateaus. Mixed oxide species and/or amorphous phases produce sloping, poorly defined plateau-to-plateau transitions. The plateau voltages for the tin species are listed in Table 8-1 and the oxide thickness calculations are shown in Table 8-2.

Table 8-1 Oxide Reduction Potentials

Oxide	Equilibrium (Volts)	Actual (Volts)
SnO	-0.84	-0.85
SnO ₂	-0.84	
SnO Rich Oxides		-0.85 to -1.0
SnO ₂ Rich Oxides		-1.0 to -1.3

Notes:

- (1) All potentials are versus Saturated Calomel Electrode (SCE) in pH 8.4 borate buffer solution
- (2) Hydrogen Evolution equals -1.3 volts (pH 8.4)

Table 8-2 Oxide Thickness Calculation

Oxide	SnO	SnO ₂
Density (g/cm ³)	6.45	6.95
Molecule Weight (g/mole)	134.7	150.7
Moles/cm ³	0.0479	0.0461
(Coulombs/cm ³ = moles/cm ³ x 96,500C/mole-electrons x no. of electrons transferred)		
C/cm ³	9245	17795
(nm per mC/cm ² = 1/(C/cm ³ x 10 ⁻⁷ nm/cm x 10 ⁸ mC/C)		
nm per mC/cm ²	1.08	0.56
Angstroms per m C/cm ²	11	6

SERA test data was used to evaluate the impact of the conditioning variables on the oxide species of surface finishes. SERA testing of the ENIG surface finish was not conducted due to the use of a borate buffer solution which is not appropriate for evaluation of that specific surface finish. A relative ranking of finishes and grading of this test is included in Appendix 3.

9 DATA ANALYSIS

9.1 Wetting Balance Results A five second wetting time was used for the wetting balance. However, the results

wetting in 5 seconds was encountered in this test, but not encountered in testing to prove the repeatability of wetting balances. Here, the substrates were deliberately stressed, and this caused the finishes to sometimes continue to wet for longer than 5 seconds.

An example of a “box and whisker plot” is shown below.

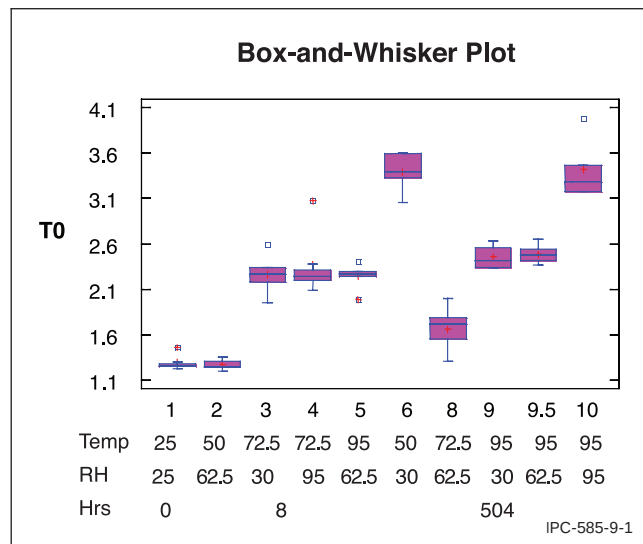


Figure 9-1 Sample Box and Whisker Plot from Data Taken from Reflowed Tin Lead

In the Figure 9-1 example, the data is initially sorted by time.

Each surface finish has the data sorted in the same way. Sorts with the parameter in other orders were also done to better understand the data.

9.2 Visual The visual examination of the coupons is shown in Appendix 6. The compilation is of the number of coupons for each condition which failed the simulated “dip and look” visual examination.

Beverley Christian, Ph.D., Research in Motion, has provided a special analysis of data from this project, and compared it to prior understanding of solderability. That is found in Appendix 9.

10 CONCLUSIONS

Differential solderability results were demonstrated for all finishes. The baseline reflowed tin lead demonstrated gradually decreasing solderability as time, temperature and humidity increased. Bare copper demonstrated the variability in the testing, with inconsistent results in the middle conditions of the test.

Both immersion silver and OSP demonstrated “robust solderability” until they suddenly decrease in solderability. This “decrease in solderability” behavior is not analyzed here - just that longer stress conditions seemed to be required in this test.

Both immersion tin and electroless nickel/immersion gold showed solderability problems with lower than expected levels of environmental stress. It is now known that both finishes were applied with less thickness, or under different recommendations from what are commercially available as this report is written. It is IMPERATIVE that at least these two finishes be re-evaluated with thicknesses in line with accepted commercial specifications.

10.1 Conclusions By Finish

10.1.1 Bare Copper Bare copper was run as a baseline of no surface finish. Tarnish was evident on many coupons. This is evidence of handling damage. Bare copper is not used in industry - but using this gives the effect of flux, instrument noise, etc.

10.1.2 RTL Reflowed tin lead has been the industry standard finish in the past. However, more parts today are Hot Air Solder Level (HASL) than simply reflowed. However, it was judged that electroplated, and then reflowed tin lead would be of more consistent thickness than HASL on these coupons. Reflowed tin lead exhibited a gradual reduction in solderability with increases of temperature and humidity.

10.1.3 Immersion Silver Immersion silver was just beginning market penetration at the time of selection for this test. Market penetration has continued at a steady pace. The immersion silver finish seems to survive stress well, until some surface phenomenon such as oxidation or sulfidation occurs. The amount of silver deposited for this test is less than that considered normal at the time of writing this report. Standard IPC-4553 has been developed for processing immersion silver. The thicknesses used in this demonstration vehicle are thinner than those expected to be specified in IPC-4553. Industry studies have shown that surface phenomena can reduce the robustness of immersion silver finishes under certain environments.

10.1.4 Immersion Tin Immersion tin finishes have been used in circuit board fabrication both at the start of the program and at the conclusion. However, immersion tin showed degradation from either temperature or humidity stress. SERA analysis should show whether the quality of the finish used in this test are up to the standards of today. IPC-4554 is being developed for processing immersion tin. The thicknesses used in this demonstration vehicle are not now regarded as optimum.

10.1.5 Electroless Nickel/Immersion Gold (ENIG) Electroless nickel/immersion gold finish is widely used for attachment using wire bonds and solder connections to board surfaces. For example, for the latter, ENIG is used to attach area array devices to boards (BGAs, etc.) It must be remembered that the gold dissolves essentially

solder connections, and testing with a wetting balance is examining the solderability of the underlying electroless nickel. The wetting force readings obtained with the wetting balance are low. However, the visual solderability results of ENIG present a better picture than the instrument readings. The reason for this is not known.

As ENIG process understanding has progressed, a better understanding of process parameters for ENIG finished circuit boards has been obtained over the years. IPC has now released IPC-4552 for plating this surface finish on boards. For instance, a better understanding of the importance of the nickel layer under the final gold has resulted in specification of this layer. No attention was paid to the nickel thickness in the samples used in this study.

Also, the 3.0 to 3.9 microinch thickness of the plated gold is on the thin side of the preferences of contributors to the IPC-4552 specification - shown below in Figure 10-1, and Table 10-1. The “as plated” thickness numbers are found in the review of the plating analysis later in this report.

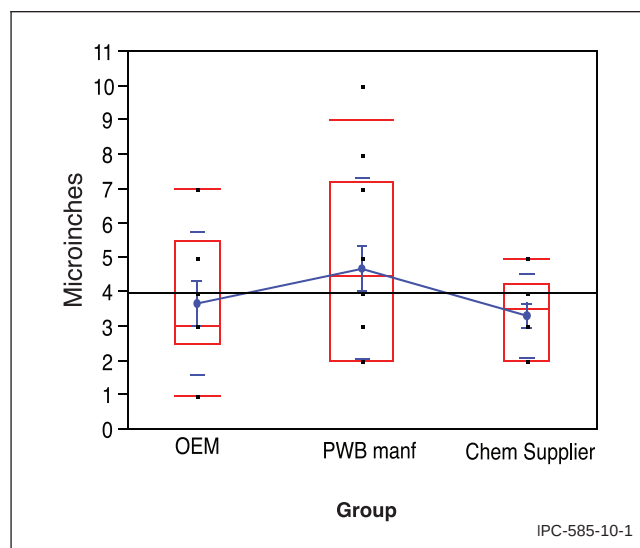


Figure 10-1 Results from Gold Thickness Survey of IPC 4-14 Subcommittee that wrote IPC-4552

Table 10-1 Means and Standard Deviations for Figure 10-1

Survey Member Categories	Number	Mean	Std Dev	Std Err Mean
OEM	10	3.7	2.1	0.67
PWB Manufacturers	14	4.7	2.6	0.71
Chemical Suppliers	10	3.3	1.3	0.40

10.1.6 OSP Substituted alkyl benzimidazole chemistries make up the majority of commercial OSP coatings. These coatings show durability to heat stress, and moderate durability to humidity stress. However, when the coating fails to protect the copper, drastic solderability failure takes place.

10.2 Investigation Confirmation Testing The task group conducted a confirmation run to validate the overall new conditioning parameters. The confirmation run parameters were:

- Time variables - 0, 8 hours, 24 hours
- Fixed temperature of 72.5 degrees Celsius
- Fixed humidity of 85%
- Alternate Finishes - same as this study - ENIG, IT and IS

The test coupon used in the confirmation run is illustrated in Figure 10-2. All testing was conducted at one test facility.

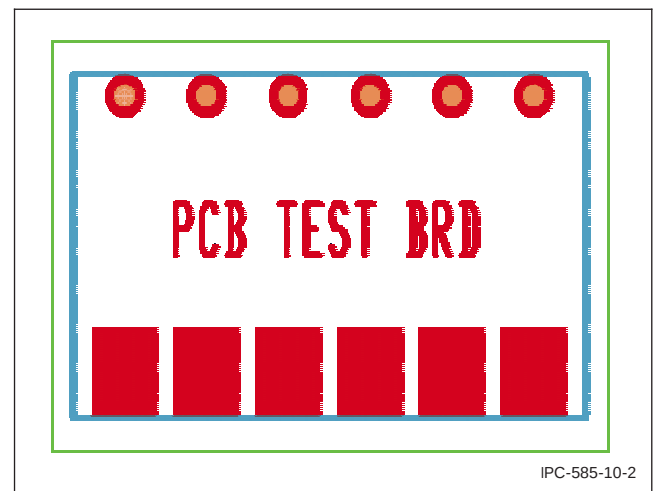


Figure 10-2 Wetting Balance Coupon (FR-4, 0.062 in thick, acid copper plated, six 3 mm SMD pads/side)

Figures 10-3 and 10-4 show the wetting balance results of the confirmation run for the ENIG, IT and IS PCB finishes. The confirmation test results reproduced the original testing effort.

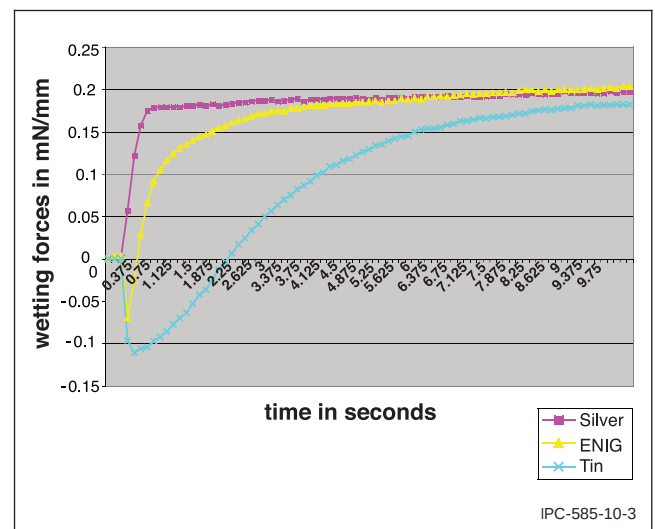


Figure 10-3 Confirmation Run 8 Hour Test Results (Effect of 8 hours of 72°C/85%RH on 3 surface finishes. Alpha 25 flux, average of 14 readings/group)

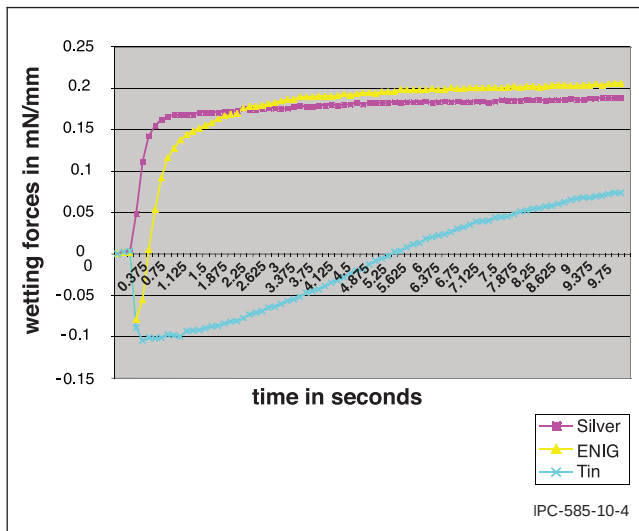


Figure 10-4 Confirmation Run 24 Hour Test Results

(Effect of 24 hours of 72°C/85%RH on 3 surface finishes. Alpha 25 flux, average of 14 readings/group)

11 RECOMMENDATIONS

The task group's recommendation to the J-STD-003A PWB Solderability Committee is to use screen test conditions of:

- 8 hours
- Fixed temperature of 72.5 degrees Celsius
- Fixed humidity of 85%

Appendix 1: Coupon Numbering System

Run	Step	Description	IT	OSP	NG	RTL	IS	
		50°C, 30% RH, 504 Hours (21 Days)	39-43	1-5	17-21	17-21	17-21	17-21
2	6	95°C, 30% RH, 504 Hours (21 Days)	67-71	61-65	50-54	72-76	78-82	56-60
3	3	50°C, 30% RH, 504 Hours (21 Days)						
4	17	95°C, 30% RH, 504 Hours (21 Days)	1-5	39-43	6-10	6-10	39-43	34-38
5	2	50°C, 62.5% RH, 8 hours	6-10	28-32	28-32	28-32	12-16	12-16
6	7	95°C, 62.5% RH, 8 hours	34-38	17-21	39-43	23-27	28-32	23-27
7	13	50°C, 62.5% RH, 1000 hours (41 d, 16 h)						
8	11	95°C, 62.5% RH, 1000 hours (41 d, 16 h)						
9	5	72.5°C, 30% RH, 8 hours	89-93	89-93	89-93	89-93 (1)	89-93 (4)	89-93
10	9	72.5°C, 95% RH, 8 hours	12-16	12-16	23-27	1-5	23-27	28-32
11	16	72.5°C, 30% RH, 1000 hours (41 d, 16 h)						
12	15	72.5°C, 95% RH, 1000 hours (41 d, 16 h)						
13	1	72.5°C, 62.5% RH, 504 hours (21days)	56-60	56-60(3)	34-38	39-43	1-5	50-54 (2)
14	14	72.5°C, 62.5% RH, 504 hours (21days)	78-82 (5)	72-76	56-60	56-60	50-54	56-60
15	12	72.5°C, 62.5% RH, 504 hours (21days)	83-87	24-27	83-87	45-49	56-60	83-87
16	8	72.5°C, 62.5% RH, 504 hours (21days)	23-34	78-82	78-82	50-54	67-71	1-5
18	18	As Received	105-108	105-109	105-109	105-109	105-109	105-109
19	10	95°C, 62.5% RH, 504 hours (21days)	72-76	83-87	45-49	67-71	45-49	45-49

Notes:

1. RTL 34-38 deleted
2. Samples 1-5 replaced
3. OSP 24-27 replaced
4. IS 34-38 deleted
5. IT 23-27 replaced



Appendix 2 A: Charts for Reflowed Tin Lead

