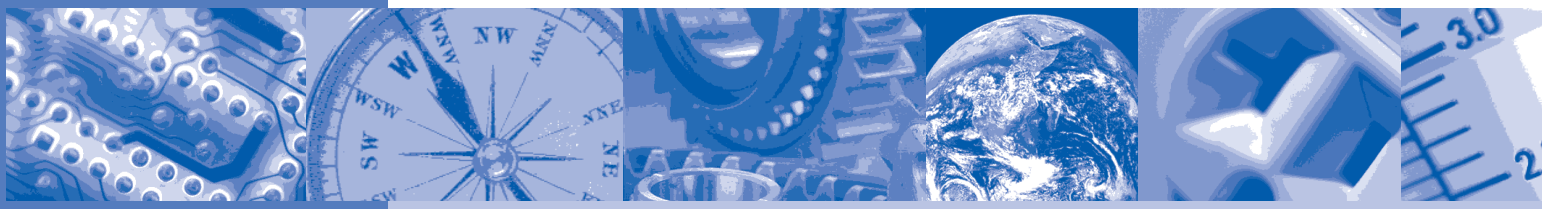
RECOMMENDED PRACTICE

ISA–RP55.1–1975 (R1983)



Hardware Testing of Digital Process Computers

Reaffirmed 30 October 1983

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Preface

This Foreword, all footnotes and all Appendices are included for informational purposes and are not part of Standard ISA-RP55.1-1975 (R1983).

This Recommended Practice has been prepared as a part of the service of ISA toward a goal of uniformity in the field of instrumentation. To be of real value this document should not be static but should be subjected to periodic review. Toward this end the Society welcomes all comments and criticisms and asks that they be addressed to the Standards and Practices Board Secretary, ISA, 67 Alexander Drive, P.O. Box 12277, Research Triangle Park, North Carolina 27709. Telephone (919) 549-8411, e-mail: standards@isa.org.

During the 22nd Annual ISA Conference and Exhibit (Chicago, September, 1967) a workshop consisting of users experienced in digital process control convened under the auspices of the ISA Chemical and Petroleum Industries Division. The product of the workshop was a document titled "Consensus of Process Computers Users Workshop — Factory Hardware Witness Test Guidelines for Digital Process Computers." (References to the factory and witnessing were subsequently eliminated considering that the tests could be alternatively performed at the user's site and that documentation or other forms of compliance may be agreed upon.) The document was then mailed to digital process computer vendors, soliciting their comments.

Some of the underlying causes and needs that led to writing of that document were explained in a talk by Mr. Kirwin Whitman (workshop secretary) at the 9th National ISA Chemical & Petroleum Instrumentation Symposium (Wilmington, Delaware, April, 1968). This talk was subsequently published in the June, 1968, issue of *INSTRUMENTATION TECHNOLOGY*, and considerable industry response resulted. Therefore, a second workshop was held at the 23rd Annual ISA Conference and Exhibit (New York City, October, 1968) and included both users and vendors. The workshop resulted in consensus between users and vendors that a digital process computer hardware test standard was needed and what the scope and objective of the standard should be. A working committee composed of both users and vendors was formed to write the desired standard. The National Committee began meeting bimonthly starting in December, 1968; and six subcommittees (later increased to eleven) met in alternate months. In January, 1969, the ISA Standards and Practices Department gave official sanction to the committee, designating it as SP-55, Hardware Testing of Digital Process Computers.

The purpose has been to create a standard to serve as a guide for technical personnel whose duties include specifying, testing or demonstrating hardware performance of digital process computers. Basing engineering and hardware specifications, technical advertising and reference literature on this standard (or by referencing portions thereof, as applicable) will provide a uniform interpretation of the digital process computer's performance capabilities and the methods used for evaluating and documenting proof of performance. Adhering to the terminology, definitions and test recommendations developed will result in clearer specifications which should further the understanding between vendors and users.

The ISA Standards and Practices Department is aware of the growing need for attention to the metric system of units in general, and the International System of Units (SI) in particular, in the preparation of instrumentation standards. The Department is further aware of the benefits to users of ISA Standards in the USA of incorporating suitable references to the SI (and the metric system) in their business and professional dealings with other countries. Toward this end this Department will endeavor to introduce SI and SI-acceptable metric units as optional alternatives to English units in all new and revised standards to the greatest extent possible. *The Metric*

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Practice Guide, which has been published by the American Society for Testing and Materials as ASTM E380-70, and future revisions, will be the reference guide for definitions, symbols, abbreviations and conversion factors.

The ISA Standards Committee on Hardware Testing of Digital Process Computers, SP55, operates within the ISA Standards and Practices Department, L. N. Combs, Vice-President. The persons listed below served as members of this Committee:

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The assistance of those who aided in the preparation of this Standard, by their critical review of the first draft, by offering suggestions toward its improvement, and in other ways, is gratefully acknowledged. In addition to SP55 committee members, the following have reviewed this Standard in its draft version and have thus served as a Board of Review. They have indicated their general concurrence with this Standard; however, it should be noted that, they have acted as individuals and their approval does not necessarily constitute approval by their company or facility.

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1 Scope

This ISA Recommended Practice establishes a basis for evaluating functional hardware performance of digital process computers. A process computer is typically characterized by the capability to acquire real-time data from a process in analog or digital form. In addition, a process computer generally has the capability to provide analog and digital control signals to the process.

This Recommended Practice covers general recommendations applicable to all hardware performance testing, specific tests for pertinent subsystems and system parameters, and a brief glossary defining terms used in this Recommended Practice. It identifies the tests to be considered and, in most cases, provides recommended procedures. Detailed specifications are necessary to define system acceptance criteria. Such specifications shall be negotiated between the vendor and user before the system is contracted.

The tests may be performed at the vendor's factory, the user's site or other suitable location. Furthermore, alternate methods of compliance such as certification or documentation of tests may be considered in place of directly performing the tests. Only equipment provided by the computer system vendor is within the scope of the Recommended Practice. Generally, this includes that equipment from the input terminations to the output terminations of the computer system.

The scope of this Recommended Practice does not include computer software testing, although certain software is necessary to perform the hardware tests. The tests do not evaluate reliability or availability. Destructive testing shall not be performed unless specifically agreed to by the vendor and user. It is also not intended that the Recommended Practice encompass interconnected multi-computer systems. These systems involve unique complexities, primarily in their software and interconnecting hardware, which were not specifically considered in the preparation of this Recommended Practice.

2 Factors to be considered

2.1 Use of the standard

The main intent of this Recommended Practice is to develop a common basic medium of communication between vendor and user. This is why it consists of the framework for a basic nucleus of tests. It is not the intent of this document to establish specifications or to set specific acceptance criteria because of the many differences which exist both in vendor product design and in user requirements.

All details of testing a specific computer system shall be negotiated before the system is contracted. A vendor's response to the requirements of this standard should be evaluated very carefully. Computer technology and methods of testing vary greatly between vendors and are continually changing. It is not the intent to label these recommended tests as the "State of the Art" or to use the Recommended Practice to prejudge a vendor or product.

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2.2 Methods of compliance

The intent of the Recommended Practice may be satisfied in several ways. This could range from testing the complete system at the factory or the installation site, testing individual subsystems, use of demonstration systems, or other alternates such as certification and performance guarantees.

There are many factors which should be considered when negotiating the methods of compliance. Examples are as follows:

1) User's experience with the vendor's product
2) Vendor's normal testing methods and documentation
3) Past performance of vendor's equipment
4) Vendor's experience in the specific equipment design
5) Costs associated with each method of compliance

Witness testing may be specified as a means of compliance. This usually means the performance of tests in the presence of the user. This approach may not conform to the vendor's normal procedures and in most cases will result in some duplications of testing. This duplication, as well as the factors cited above, should be considered when negotiating compliance to this standard.

2.3 Sequence, duration, and location of tests

Vendors generally establish normal testing patterns which define sequence, duration, and location of tests. Obviously, these patterns vary from vendor to vendor. Careful consideration must be given to all deviations from these normal patterns of testing since deviations may increase or decrease the effectiveness of the testing and could involve extra costs.

2.4 Acceptance criteria for tests

Each test should have acceptance criteria based on conformance to the specifications referenced in the systems contract.

It is important to know which specifications apply to particular hardware testing configurations. Subsystem specifications often apply to individual devices or assemblies and may not be measurable or applicable at the system level. For the purposes of this Recommended Practice, the system specifications determining out-of-limit conditions shall be the subsystem specifications unless the vendor has separate system specifications.

Any special acceptance criteria or tests shall be negotiated and included in the system contract. The subsystem and system specifications must be altered to reflect all special acceptance criteria.

When a series of tests are performed, there should be agreement on how the failure of one test affects the others. Usually this can only be determined after the cause of the failure is known. Requirements for documentation of failure data should be established in accordance with 10, Documentation.

2.5 Quantity of hardware tested

These tests do not specify the quantity of similar hardware to be tested. For example, multiple peripheral devices and many process input and output channels are typically included in a system. The quantity and identity of such devices or channels to be tested shall be specified.

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The manufacturing process may justify sample testing techniques at specific subsystem or system levels of assembly.

The testing of partially implemented, spare, and expansion functions should be considered. Specific tests and acceptance criteria for these functions should be defined.

2.6 Special functions

This Recommended Practice addresses tests which apply to typical digital process computers in today's marketplace. Where equipment configurations and functions differ from those outlined in this Recommended Practice, the test procedures shall be modified to reflect the individual equipment specifications.

2.7 Test equipment

Selection and certification of testing and measuring equipment is normally at the discretion of the vendor. Variations from this procedure should be negotiated when the system is contracted.

2.8 Cost of testing

Several areas throughout this Recommended Practice note that extra costs might be involved. As a general guide, extra costs may be incurred whenever a vendor is expected to deviate from his normal testing pattern.

Typical factors affecting the cost of testing are:

1) Number of separate test configurations required
2) Methods of compliance (See 2.2)
3) Sequence, duration, and location of tests (See 2.3)
4) Quantity of hardware tested (See 2.5)
5) Special programming requirements
6) Special testing equipment
7) Effort required to prepare and perform tests
8) Documentation requirements (See 10)

The additional testing costs may be justified through factors such as reduced installation costs, more timely installation, and early identification of application problems.

3 Recommended test, central processing unit

3.1 Objectives

The Central Processing Unit (CPU) tests are designed to demonstrate the capability of the CPU to perform all of its specified functions.

3.2 Equipment to be tested

Tests for the following CPU functions are included in this section:

1) Arithmetic and Control

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2) Input-Output (I/O)

3) I/O Direct Storage Access

4) Hardware Interrupt

5) Hardware Timer

6) Main Storage

In cases where the CPU configuration differs from that described in this Recommended Practice, the test procedure shall be modified accordingly. Depending upon the storage capacity of the CPU subsystem, additional main storage hardware may be housed in a separate enclosure. For the purpose of the CPU test, all main storage is considered to be an integral part of the CPU subsystem.

Bulk storage, often considered as an extension of main storage for the storage of programs and data, may conveniently be tested concurrently with the CPU tests. Similarly, testing of consoles and certain other I/O devices are closely related to CPU functions. Test procedures for bulk storage and these I/O devices are described in 4, Data Processing Input-Output Subsystems.

3.3 Test procedures

Each of the following functions shall be tested individually and subsequently in combination as permitted by CPU configuration.

3.3.1 Arithmetic and control

All instructions, with all modes and options, shall be tested for operation in accordance with their specifications. Testing should be performed in a logical sequence, such as starting out with the basic load, store and transfer operations; progressing through the arithmetic, branch, and shift operations; logical, control operations, etc. I/O related operations such as direct storage access and interrupt tests are described in 3.3.3, I/O Direct Storage Access Channel, and 3.3.4, Hardware Interrupts.

3.3.1.1 Instruction load

A basic subset of instructions may be loaded through the computer control console or through any other conveniently available input medium. If the CPU has single cycle available, the basic subset of instructions can be executed in single cycle and the appropriate registers examined for correct results. If these instructions are entered through the control console, the switches and associated indicators (if any) should be examined for proper operation. Typical instruction complement may include:

1) Transfer Instructions

   a) Load-Store Accumulator

   b) Load-Store Index Register

   c) Register-to-Register Transfer

   d) Storage-to-Storage Transfer

2) Arithmetic

   a) Add

   b) Subtract

   c) Multiply

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d) Divide

e) Arithmetic and Logical Shifts

3) Logical

a) OR (Logical Sum)

b) And (Logical Product)

c) Compare

d) Exclusive OR (Logical Subtract)

4) Control

a) Set Sign of Accumulator Positive-Negative

b) No Operation

c) Pause or Halt

d) Jump

e) Skip

3.3.1.2 Instruction execution

For testing efficiency, after the few basic instructions are tested by entering them through the control console keyboard or console switches, all other instructions can be checked by executing a program which manipulates all the instructions. The execution times of the instructions may be verified during this test. The program should be written so as to indicate the area of failure. For example, the program may automatically restart after completing a pass if no errors occur, or stop on an error condition. If an error is encountered, the area which failed should be identifiable from the stop address, program counter contents, or similar indication.

3.3.2 Input-Output (I/O) adapter(s)

3.3.2.1 Device address

A typical I/O requirement for the computer is to sense when devices are ready for transfer, to transmit control pulses to the peripheral devices, and to transfer data. The I/O channels generally operate on a party-line basis so that many devices may be connected to one channel. The peripherals are assigned device addresses which allow the computer to identify them. Each peripheral device address shall be generated and the test shall verify that only the addressed device responds.

3.3.2.2 BYTE manipulation

If hardware data packing or unpacking (byte assembly) capability is provided in the CPU or I/O devices, it should be tested by transferring data and verifying that the CPU or I/O device assembles or disassembles them correctly.

3.3.2.3 Device ready

In subsystems where data are transferred only when the device is ready, this operation shall be verified.

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3.3.2.4 Error checks

Simulation of an error condition shall result in an interrupt or other action as specified in the subsystem specifications. Status or error functions of all devices should be checked using software where possible. If the subsystem has a status register that indicates the status or error condition of a device on the I/O channel, the register contents shall be examined for the proper indication. Status or error functions on a magnetic tape transport, for example, may indicate that the tape is being rewound or that a read error has occurred.

3.3.3 I/O Direct Storage Access Channel (DSAC)

This test verifies the complex of data paths, registers and controls which allow high speed I/O devices, such as magnetic tapes, drums, or disk files, to transmit data to and from main storage on a cycle-stealing basis.

3.3.3.1 Typical functions of the DSAC

Programmed subroutines shall test the following typical functions of the DSAC:

1) Initiation of DSAC operation by the specified I/O instructions

2) Independent I/O data transfer to and from the DSAC concurrent with mainline program operation. Multi-ported storage systems should be tested with all ports operating simultaneously.

3) Delay of the mainline program while DSAC data are transferred to and from main storage.

3.3.3.2 DSAC termination

Hardware termination methods may include transfer until the word count is zero (with or without a subsequent hardware interrupt), or transfer until a higher priority hardware interrupt is encountered. These and any other hardware DSAC termination methods should be tested to verify proper operation.

3.3.4 Hardware interrupts

If a hardware interrupt function is provided, all levels of interrupt are tested for proper sequencing and handling of hardware priorities. This can be accomplished using hardware or software simulation that sequentially causes each of the interrupt conditions to occur.

3.3.4.1 Interrupt acknowledge

A test shall be performed to verify that both internal and external hardware interrupts are properly acknowledged. By using software or hardware simulation, all interrupts shall be singly activated and the status of the system shall be verified to determine that proper acknowledgement occurs. If hardware functions are provided which automatically store or otherwise save the contents of registers, indicators, etc, in the correct operation of this function shall be verified.

3.3.4.2 Interrupt enable-disable

The master interrupt enable-disable (mask-unmask) controls and the enabling and disabling of individual interrupts (if provided)shall be tested. Through hardware or software simulation of interrupts on all available levels, it should be verified that hardware interrupts are acknowledged if and only if the proper combination of master and individual enable-disable conditions exist. If console or other indicators are provided to indicate the status of the interrupt structure, their proper operation shall be verified.

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3.3.4.3 Multi-level interrupts

In typical hardware multi-level (priority) interrupt structures, the occurrence of an interrupt on a level higher than that currently being processed by the program results in a hardware initiated transfer to a storage location predefined by either hardware or software. In addition, the hardware initiated action may temporarily disable the interrupt structure and may provide automatic storage or other means of saving the contents of registers and indicators. When provided, these features shall be verified by an appropriate test. Using hardware or software simulation, interrupts may be simultaneously generated on various interrupt levels and the system status examined to verify that the interrupts were properly acknowledged. If automatic hardware disabling is provided, this may be tested by causing a series of interrupts such that a higher level interrupt occurs while the interrupt structure has been disabled by the hardware. Such an interrupt should not be acknowledged until the end of the disabling interval.

3.3.4.4 Power failure interrupt

In systems providing this feature, an interrupt is generated prior to the total failure of the primary power source. As a result of the interrupt, certain hardware initiated actions are performed to insure an orderly shutdown of the computer. During this shutdown procedure, automatic hardware or programmed subroutines may be used to save the contents of certain registers and system indicators. The purpose of this test is to verify that the specified hardware actions are accomplished prior to complete shutdown of the system. A power failure shall be simulated and the appropriate system parameters shall be observed to insure that the specified hardware actions have occurred. If a hardware save feature is provided, the saved data shall be verified after power is reapplied to insure that they have not been altered.

3.3.4.5 Auto-restart interrupt

If provided in the system, this feature provides for automatically restarting the CPU after a power failure. Although many of the actions required for auto-restart are software functions, certain hardware actions are required. A power failure shall be simulated and during the restart action the hardware functions shall be verified for proper operation.

3.3.4.6 Miscellaneous interrupt features

Other hardware interrupts or task control features shall be tested to verify proper operation.

3.3.5 Hardware timers

3.3.5.1 Interval timers

Hardware interval timers shall be checked to insure that they start and stop properly under program control. A specified number of time intervals shall be tested to verify timing accuracy. If the timer has hardware interrupt capability, a test shall be performed to check that the timer interrupts at the proper time. If provision is made for an external time base, an appropriate signal generator shall be connected to the timer input and the timer tested for proper operation.

3.3.5.2 Watchdog timer

If a watchdog timer is provided in the CPU, a test shall be performed to verify the activation of the alarm and reset functions. Under program control, a specified I/O instruction is executed to insure that the watchdog timer resets. Operation of the alarm function is tested by blocking or by-passing the I/O instruction and verifying that all specified timer functions operate properly.

3.3.5.3 Real-time timer

If a hardware real-time timer which is not software dependent is included in the CPU, a test shall be performed to compare the timer against a calibrated time base.

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3.3.6 Main storage

3.3.6.1 Addressing

Addressing shall be tested by loading a specified number of main storage locations with their own addresses. Read out these storage locations and compare to verify correct addressing.

3.3.6.2 Worst case pattern test

This test, sometimes referred to as the Delta Noise or Checkerboard Test, shall be performed by storing into main storage the worst case data pattern for the particular storage design and addressing scheme used by the vendor. Such a test normally loads a major segment of main storage with this pattern so as to produce the worst possible signal-to-noise ratio. The data are written, read back, complemented, and written again on repeated storage cycles. The test should be executable for more than one segment of main storage. When this option is available, the entire main storage can be tested for stability.

3.3.6.3 Circuit load test

This test is designed to identify circuit loading and adjacent bit noise problems. The main storage shall be tested using a "floating one" and a "floating zero" pattern. The "floating one" test is performed by loading one word with all zeros except for a one in the most significant bit position. The word is read, compared to its expected bit pattern and, if correct, is shifted one position to the right and restored in the next higher storage location. The procedure is repeated until all storage locations have been tested. The "floating zero" test is identical except that a word containing only a single zero is used.

3.3.6.4 Storage protect

This test is designed to verify that protected areas of main storage are not violated when hardware storage protection is provided. A preselected area of main storage shall be loaded with a known data pattern and storage protection of the selected area activated by means of the appropriate mechanism (bit, area code, etc.). An attempt to violate the protected area shall result in a violation signal, indicator, or interrupt. It shall be verified that the protected data were not modified. A test shall be performed to verify that storage protection can be deactivated so that the selected area is restored to the unprotected status. All areas capable of being hardware protected shall be tested in a similar manner. If the hardware protection can be program controlled, the control instructions shall be tested to verify proper operation. All other hardware protect features shall be tested.

4 Recommended tests, data processing input-output subsystems

4.1 Objectives

Data Processing Input-Output (DP I/O) Subsystems tests are directed at insuring proper function of I/O subsystems which are part of typical digital process computer systems. These tests are designed to verify functions at the subsystem level only. They do not cover interacting systems testing which is defined in 8 Interacting System.

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For the purposes of this standard, the elements of the Data Processing Input-Output Subsystem include:

1) The attachment circuitry, which is housed in the CPU and which furnishes logic controls along with data links to the I/O bus.

2) The controller, which provides the buffer between the I/O bus and the I/O device itself. The controller may provide a variety of functions to minimize the requirement for a direct interaction between the I/O device and the main CPU data paths. Typical functions provided in the controller include control of cycle-stealing operations, error checking, and device address coding. The controller is not a necessary part of the subsystem: many subsystem designs specify direct connection of the device to the CPU.

3) The I/O devices, which provide bulk storage, card or paper tape processing, printed output, terminal communication, and other data processing functions.

4.2 Equipment to be tested

In cases where the I/O equipment configurations differ from those described in this standard, the test procedure should be modified or additional tests defined to conform to the equipment specifications. Tests for the following I/O subsystems are included in this section:

1) Card Readers and Punches

2) Paper Tape Readers and Punches

3) Disk Storage Devices

4) Drum Storage Devices

5) Magnetic Tape Devices

6) Typers and Line Printers

7) Video Display Stations

8) Data Collection Terminals

9) Data Modems

10) Keyboards and Consoles

4.3 Test procedures

4.3.1 Card readers and punches

The device to be tested may be a reader only, a punch only, or a combination reader-punch unit. Hollerith or various binary codes may be used as specified for the particular I/O subsystem.

All specified functions shall be tested. Typical functions include:

1) Interlocks

2) Operational Keys, Switches, and Indicators

3) Punch and Read Operations

4) Card Transport

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4.3.1.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

1) Failure to feed from input hopper
2) Empty input hopper
3) Punch die not seated
4) Card jam detection
5) Full stacker condition
6) Door and cover interlocks
7) Full chad box
8) Chad box not installed
9) Crank interlock
10) Last card feed operation

4.3.1.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators to be tested include:

1) Keys and Switches
   a) Start Key
   b) Stop Key
   c) Runout Key
   d) Load Key
   e) Single-Cycle Switch
   f) Reset Key
   g) Power-On Switch
   h) Duplication Key
2) Indicators
   a) Ready or Go Indicator
   b) Halt or Not-Ready Indicator
   c) Power-On Indicator
   d) Error Indicators

4.3.1.3 Punch and read operations

Read and punch speed shall be tested in accordance with specifications (cards processed per minute in a continuous feed mode).

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All alphanumeric or binary characters shall be tested in accordance with the character configurations defined in the specifications. Illegal characters shall cause the specified error indications. A typical pattern (alphanumeric) may include the following character configuration:

ABCD . . . Z0123 . . . 9@–$+. . .*ABCD. . .

Various character configurations (in a random mode, sequential mode, etc.) shall be used to test for multiple or missing reads and for multiple or missing punches. Typical patterns may include:

Card #1 - ABCD.....9@$+

Card #2 - BCDE.....@$+–

Card #3 - CDEF.....$+–#

etc.

Card #1 - IQXHPWGOVFNVEMTDLSCK...

Card #2 - QXHPWFOVFNVEMTDLSCKI...

Card #3 - XHPWFOVFNVEMTDLSCKIQ...

Vertical and horizontal read registration shall be tested by verifying the ability to read prepunched cards whose punch holes are at the prescribed specification limits for this parameter.

The punched card output of the punch shall be tested with a card gage or similar device to verify proper vertical and horizontal registration of the punched holes. Consistency of registration shall also be examined.

4.3.1.4 Card transport

Cards shall be examined for marks, tears, and bends on faces or edges which may indicate improper card transport or mechanical interference. Corner cut cards with various corner cut configurations shall be used to verify proper card transport and feed.

If there are multiple stackers, stacker select operations shall be tested for all specified commands. Individual stackers may be selected as a function of error conditions, character coding, and other selection instructions identified in the specifications.

4.3.2 Paper tape readers and punches

Paper tape readers and punches may specify the use of 5-, 6-, 7-, or 8-channel tape. Depending upon the specifications, the device may be required to process tape made of oiled or non-oiled paper, of a metalized plastic material, or a combination of the above.

The tape may be either chad or chadless. Chad tape is defined as tape which has all holes completely punched out. If chadless tape is used, all chad shall be on the side of the tape away from the reading mechanism. The test method shall allow for configurations of feed mechanisms which are designed to handle strip feed, center-hole feed, or reel feed.

All specified functions shall be tested. Typical functions include:

1) Interlocks

2) Operational Keys, Switches, and Indicators

3) Punch and Read Operations

4) Paper Tape Transport

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4.3.2.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified.

All specified indicators shall be activated. Typical interlock conditions include:

1) Empty supply reel or tape runout
2) Tape guide arms not seated
3) Tape tension detection
4) Door and cover interlocks
5) Full chad box
6) Chad box not installed

4.3.2.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators include:

1) Keys and Switches
   a) Delete Key
   b) Feed Key
   c) Reset Key
   d) Start Key
   e) Stop Key
   f) Reel or Strip-Select Switch
   g) Single-Cycle Switch
   h) Power-On Switch
2) Indicators
   a) Ready or Go Indicator
   b) Halt or Not-Ready Indicator
   c) Power-On Indicator
   d) Error Indicators

4.3.2.3 Punch and read operations

Punch and read speed shall be tested in accordance with specifications (characters read or punched per second in a continuous mode).

All alphanumeric or binary characters shall be tested in accordance with the character configurations identified in the specifications. Illegal characters shall cause the specified error indications. A typical test pattern (alphanumeric) may include the following character configurations:

ABCD . . . Z0123 . . . 9@–$+. . .*ABCD. . .

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Various character configurations (in a random mode, sequential mode, etc.) shall be used to test for multiple or missing reads and for multiple or missing punches. Typical test patterns are described in 4.3.1.3, Punch and Read Operations.

The punched tape output shall be examined to verify proper longitudinal registration. A standard tape gage or similar device may be used.

The punched tape shall be tested to verify that all feed holes are punched as blank tape advances through the punch station, If so specified, duplicate feed hole punching shall not occur during a backspace or reverse operation.

4.3.2.4 Paper tape transport

Tapes shall be examined for marks, tears, elongated holes, and raised edges on feed and channel holes which may indicate improper tape transport or mechanical interference at the punch or read station. Tape dispensing and take-up functions shall also be tested using various amounts of tape on the tape reels.

Forward and reverse tape motion during punch and read operations shall be tested by verifying that a specified backspace/forward routine is initiated on command.

Various combinations of short and long tape motions shall be used to test for proper tape feed, tape registration, and read-punch functions.

4.3.3 Disk storage devices

These tests apply to single or multiple disk configurations which use fixed disks or customer-removable cartridges. The tests are also applicable to fixed head or moveable head devices. (A fixed head device has its heads permanently located over specified track locations. A moveable head device has its heads mounted on a moveable access mechanism which may be positioned opposite any track location on the disk surface.)

All specified functions shall be tested. Typical functions include:

1) Interlocks
2) Operational Keys, Switches, and Indicators
3) Read and Write Operations
4) Seek or Access

4.3.3.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

1) Cartridge or Disk-Pack Removal Interlock
2) Cover Interlock
3) Read or Write Circuit Protect
4) Over- or Under-Voltage Detection
5) Speed Detection
6) Head Load, Unload, or Position Interlock
7) Pressurization Interlock

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4.3.3.2 Operational keys, switches, and indicators

The operation of all keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and indicators include:

1) Keys and Switches

   a) Head-Select Switch

   b) Incremental Step Switch

   c) Incremental Direction Switch

   d) Head-Load Switch

   e) Reset Key

   f) Power-On Switch

   g) Start Key

   h) Stop Key

2) Indicators

   a) Head-Select Indicator

   b) Power-On Indicator

   c) Ready Indicator

   d) Drive-Number Indicator

   e) Cartridge/Pack Status Indicator

   f) Read/Write Protect Indicator

   g) Error Indicator

4.3.3.3 Read and write operations

Data shall be transferred to and from the entire recording surface of the disk storage device to verify the operation of specified read and write functions. Cross-talk tests shall be performed to verify read and write functions on adjacent tracks. Various data patterns and record lengths shall be used to simulate worst-case bit patterns if so specified. Interchangeability of disk packs between disk storage devices shall also be verified. Typical functions to be tested in this type of device include:

1) Accessing to all track addresses in a serial access mode (including return to zero or home).

2) Random accessing to track addresses so that the access mechanism is required to make both long and short movements. Random accessing verifies such functions as:

   a) Forward Fast

   b) Forward Slow

   c) Reverse Fast

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d) Reverse Slow

e) Stop and Detent

f) Access Time (Average and Maximum)

4.3.4 Drum storage devices

Drum storage devices may be configured with a magnetic drum unit which is vertically or horizontally mounted. The read/write heads are typically fixed at a specified track location over the drum surface.

All specified functions shall be tested. Typical functions include:

1) Interlocks

2) Operational Keys, Switches, and Indicators

3) Read and Write Operations

4.3.4.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

1) Thermal Overload

2) Speed Detection

3) Pressurization Interlock

4) Over- or Under-Voltage Detection

5) Head Position Interlock

6) Read or Write Protect

4.3.4.2 Operational keys, switches, and indicators

The operation of all keys, switches, and interlocks shall be tested according to specification. Typical keys, switches, and indicators include:

1) Keys and Switches

   a) Head-Select Switch

   b) Power-On Switch

   c) Head-Load Switch

2) Indicators

   a) Head-Select Indicator

   b) Power-On Indicator

   c) Head-Load Indicator

   d) Error Indicator

4.3.4.3 Read and write operations

Data shall be transferred to and from the entire recording surface of the drum storage device to verify the operation of specified read and write operations, including the write protect function.

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Cross-talk tests shall be performed to verify read and write function on adjacent tracks. Various data patterns shall be used to simulate worst-case bit patterns if so specified. Typical functions tested during read and write operations include:

1) Proper head and address selection as a function of the unique address associated with the identifying bits or bytes.

2) End-of-record recognition using variable data lengths.

3) Data transfer rate in a continuous read mode.

4.3.5 Magnetic tape devices

The individual specifications for the magnetic tape device may permit the use of seven- or nine-track magnetic tape. The grades or types of tape may be specified in accordance with the tape bit densities and other characteristics of the device. The test method shall allow for configuration of magnetic tape devices which are designed to handle full reels, miniature reels, or cartridges of magnetic tape.

All specified functions shall be tested. Typical functions include:

1) Interlocks

2) Operational Keys, Switches, and Indicators

3) Read and Write Operations

4) Tape Transport

4.3.5.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

1) Reel, Door, and Tape Mechanism Interlocks

2) Thermal Overload

3) Over- or Under-Voltage Detection

4) Tape or File Protect

5) Tape Tension Detection

6) Head-Unload or Load Failure

4.3.5.2 Operational keys, switches, and indicators

The operation of keys, switches, and indicators shall be tested according to specifications. Typical keys, switches, and interlocks include:

1) Keys and Switches

   a) Start Key

   b) Stop Key

   c) Reset Key

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d) Tape-Load Key

e) Tape-Rewind Key

f) Reel-Release Switch

2) Indicators

a) End-of-Tape Indicator

b) Tape or File Protect Indicator

c) Select or Drive Number Indicator

d) Ready Indicator

e) Thermal or Voltage Failure Indicator

f) Error Indicator

4.3.5.3 Read and write operations

To verify proper function of the read or write operation, data shall be transferred to and from the magnetic tape device. Interchangeability of magnetic tapes between magnetic tape devices shall also be verified. Worst-case bit patterns and timings shall be used if so specified. Typical functions tested during the read and write operations include:

1) Horizontal Validity Check

2) Record Validity Check

3) Write Check

4) Load Point (Start Read or Write)

5) End-of-Tape

6) Data Block Recognition

7) Read Backwards

8) Backspace (no data transferred)

9) Erase Tape

4.3.5.4 Tape transport

The tape transport is activated when commands to read, write, read backward, rewind, or unload are received by the tape device while it is in a ready status. Short and long records shall be read and written to test for proper functions of drive clutches and tape positioning mechanisms. High and low speed rewind functions shall also be verified along with start-stop time if so specified.

4.3.6 Typers and line printers

This procedure defines the test requirements to verify proper function of the output printing devices. The output printer may be a teletypewriter, a typewriter, or a line printer.

All specified functions shall be tested. Typical functions include:

1) Interlocks

2) Operational Keys, Switches, and Indicators

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3) Print Operations

4) Carriage and Forms Transport

4.3.6.1 Interlocks

Simulation of all specified interlock conditions shall result in a subsystem interrupt or other action as specified. All specified indicators shall be activated. Typical interlock conditions include:

1) Cover Interlocks

2) Print-Protect Shield Not In Place

3) Forms Runout

4) Forms Jam

5) Platen Not Installed

6) Printer Not Ready

4.3.6.2 Operational keys, switches, indicators, and manual controls

All keys, switches, indicators, and manual controls shall be tested according to specifications. Typical keys, switches, indicators, and manual controls include:

1) Keys and Switches

   a) Start Key

   b) Stop Key

   c) Forms-Runout Key

   d) Space Key

   e) Carriage-Restore Switch

   f) Reset Key

   g) Power-On Switch

   h) Program Interrupt Key

2) Indicators

   a) Ready or Go Indicator

   b) Halt or Not-Ready Indicator

   c) Power-On Indicator

   d) Error Indicators

3) Manual Controls

   a) Carriage Clutch

   b) Forms Thickness Adjustment

   c) Paper Release Lever

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4.3.6.3 Print operations

Printer speed shall be tested in accordance with specifications (lines-per-minute or characters-per-second in a continuous print mode).

All alphanumeric or binary characters (in a random mode, sequential mode, etc.) shall be tested in accordance with the character configurations identified in the specifications. Worst-case test patterns shall be used if so specified. A typical test pattern may include the following character configuration:

ABCD . . . Z0123 . . . 9@–$+. . .*ABCD. . .

Various character configurations are to be tested as a function of the parallel or serial mode of the individual printer and as a function of the device specifications. Each line of print shall be checked to insure that the specified number characters are printed within the margins. Typical character configurations may include:

Line #1 - ABCD.....9@$+

Line #2 - BCDE.....@$+–

Line #3 - CDEF.....$+–#

etc.

Line #1 - IQXHPWFOVFNVEMTDLSCK...

Line #2 - QXHPWFOVFNVEMTDLSCKI...

Line #3 - XHPWFOVFNVEMTDLSCKIQ...

etc.

A printer output test shall be performed to verify that all specifications for print quality are met. Typical print quality specifications include:

1) Character Alignment
2) Spacing Between Adjacent Characters
3) Uniformity of Character Impressions
4) Multiple Copy Legibility

4.3.6.4 Carriage and forms transport

Forms shall be checked for marks, tears, bends, or burred edges which may indicate improper forms transport or mechanical interference. Pin feed platens shall be checked to insure that pins operate properly and that forms tension conforms to specifications.

Carriage spacing, skipping, and other specified functions shall be tested. Typical specified functions include:

1) Ribbon Color Control
2) Carriage Return
3) Tabulate
4) Space and Backspace
5) Double and Triple Space
6) Space Suppress

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