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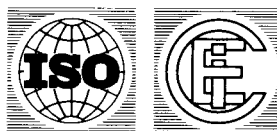
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Information technology — Intelligent Peripheral Interface

Part 2:

Device specific command set for magnetic disk drives

*Technologies de l'information — Interface pour les périphériques intelligents —
Partie 2: Jeu de commandes spécifiques appareil pour les unités disques
magnétiques*



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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 9318-2 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*.

ISO/IEC 9318 consists of the following parts, under the general title *Information technology — Intelligent Peripheral Interface*:

- *Part 1: Physical level*
- *Part 2: Device specific command set for magnetic disk drives*
- *Part 3: Device generic command set for magnetic and optical disk drives*
- *Part 4: Device generic command set for magnetic tape drives*

Annex A forms an integral part of this part of ISO/IEC 9318. Annexes B, C and D are for information only.

Introduction

This part of ISO/IEC 9318 does not replace any existing standard, but it does complement other Intelligent Peripheral Interface (IPI) standards (see clause 2).

This part of ISO/IEC 9318 provides a definition of the device specific interface portion of a series of standards called the Intelligent Peripheral Interface (IPI) ISO/IEC 9318, a high performance, general-purpose parallel peripheral interface. This part of ISO/IEC 9318, responds to an industry market need (expressed both by users and manufacturers) to limit the increasing costs in hosts associated with changes in peripherals.

Information technology — Intelligent Peripheral Interface

Part 2:

Device specific command set for magnetic disk drives

1 Scope

This part of ISO/IEC 9318 describes the Logical Level 2 (device level) Interface for disk drives. See clause 6 of ISO/IEC 9318-1 for explanation of the levels.

The physical, electrical, and configuration characteristics and the transmission protocol of this interface are in accordance with ISO/IEC 9318-1. The interface is capable of handling data rates from 0 to at least 10 Mbytes/s, depending on driver and receiver classes.

The purpose of this part of ISO/IEC 9318 is to facilitate the development and utilization of a device level interface which permits the interconnection of disk slave peripherals to a controller.

This part of ISO/IEC 9318 does not replace any existing standard, but it does complement other Intelligent Peripheral Interface (IPI) standards (see clause 2).

This part of ISO/IEC 9318 provides a definition of the device specific portion of a family of standards called the Intelligent Peripheral Interface (IPI), a high performance, general-purpose parallel peripheral interface.

The intent of the IPI is to isolate the host (CPU), both hardware and software, from changes in peripherals by providing a "function generic" command set to allow the connection of multiple types of peripherals (disks, printers, tapes, communications). To smooth the transition from the current methods to the generic approach, the IPI supports device-specific command sets, such as this one, to aid in bridging the gap between the two approaches.

To accomplish this set of goals, the design of the IPI includes device-specific and device-generic command sets, both utilizing a common physical bus. The device-specific command set provides:

- Device-oriented control;
- Physical Data Addressing;
- Timing Critical Operations;
- Lower Device Cost.

The device-generic command set provides a higher level of functionality and portability. It includes:

- Host/Device Independence;
- Logical Data Addressing;
- Timing Independence;
- Command Queuing Capability.

A system is not restricted to the use of one level of command set or the other. It is possible that both levels of command sets will be utilized with a given system's architecture to balance such parameters as system performance, cost, and

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peripheral availability. It is also possible for the host to provide for migration from device-specific to device-generic levels while still retaining the same physical interface.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this part of ISO/IEC 9318. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this part of ISO/IEC 9318 are encouraged to investigate the possibility of applying the most recent editions of the standards listed below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO 646:1983, *Information processing - ISO 7-bit coded character set for information interchange*.

ISO/IEC 9318-1:—¹⁾ *Information technology - Intelligent Peripheral Interface
Part 1: Physical Level*

1) To be published.

3 Definitions and conventions

3.1 Definitions

For the purpose of this part of ISO/IEC 9318, the following definitions apply:

3.1.1 Bus Control: The physical-level octet placed on BUS A by the master during the Bus Control sequence. It is used to define the bus configuration and information type for the subsequent Information Transfer. The three Bus Control types are: Command Control, Response Control, and Data Control.

3.1.2 Bus Exchange: The Bus Control sequence (initiated by the master) and the Ending Status sequence (initiated by the slave), which are used to frame an Information Transfer.

3.1.3 Busy: Busy indicates that the slave is unable to respond to the master's request and may be reported at either the Physical Interface (Selection Sequence) or at the Logical Interface (Ending Status Sequence).

3.1.4 Command: The information transferred from the master to the slave following a Command Control. The information contains command-specific parameters.

3.1.5 Command Control: A Bus Control that specifies that command information is to be transferred from the master to the slave during the Information Transfer and identifies the command type.

3.1.6 Data Control: A Bus Control that specifies that data information is to be transferred during the Information Transfer, and specifies various data transfer requirements, including the orientation of the data on the disk.

3.1.7 Defect Map: A list of the defects recorded by the drive manufacturer on the slave.

3.1.8 Format Specification: An ordered list of parameters that specify the format of the tracks and sectors on the disk.

3.1.9 Information Transfer: The Physical Interface transfer of commands, responses, and data that are framed by a Bus Exchange.

3.1.10 Level 2: A device-level-protocol interface in which the master is aware of the specific characteristics of the device under its control.

3.1.11 Level 3: An intelligent interface oriented to the generic characteristics of devices, but not the characteristics unique to the device.

3.1.12 Logical Interface: All operations above the Physical Interface.

3.1.13 Master Status: The status placed on BUS A by the master during the Ending Status sequence after the Information Transfer.

3.1.14 parameter: The information octets transferred after a Command or Response Bus Control. Command parameters further define a command or contain specific information about a command, such as head number, cylinder number, etc. Response parameters contain information on the state of the slave, such as status, current head, current cylinder, etc.

3.1.15 Physical Interface: The mechanical, electrical, and bus protocol characteristics specified in ISO/IEC 9318.

3.1.16 physical sector: This term refers to the sectors identified by the disk drive, relative to index, with zero as the first.

3.1.17 response: The information transferred from the slave to the master following a Response Control. The information contains parameters specific to the response type.

3.1.18 Response Control: A Bus Control which specifies that information about a response type is to be transferred from the slave to the master during the Information Transfer and identifies the type of response.

3.1.19 RPS: This is an abbreviation for Rotational Position Sensing, a means for the slave to notify the master of the relative head position with respect to index.

3.1.20 RPS Pulse: The time defined by the master on Load Position and Load RPS Target Sector Address commands during which the Class 2 RPS Interrupt shall be asserted.

3.1.21 Slave Status: The status placed on the BUS B by the slave during the Ending Status sequence after an Information Transfer.

3.1.22 status response: The status supplied to the master when executing a Read Status Response that contains the exception status bits.

3.1.23 Target Sector: The physical sector designated by the master during the Load Position command or Load RPS Target Sector Address command using the RPS Target Sector Address parameter.

3.2 Conventions

Certain terms used herein are the proper names of signals. These are printed in uppercase to avoid possible confusion with other uses of the same words (e.g., ATTENTION IN). Any lowercase uses of these words have the normal American-English meaning.

A number of conditions, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lowercase (e.g., In, Out, Selective Reset, Bi-directional, Bus Control, Operation Response). Any lowercase uses of these words have the normal American-English meaning.

4 General description

4.1 Application environment

The master (controller) provides control of one to eight slaves (disk drives) with a device level set of commands and data transfers. The master and slave of a level 2 environment are the slave and facility of a level 3 environment. There are no facilities in the level 2 environment.

4.2 Logical Interface characteristics

4.2.1 Slave Control

Control of a slave is exerted by the master through the Bus Controls that initiate the Bus Exchanges for command, response, and data transfers. The Bus Controls incorporate coding that identifies the particular command, response, or data type. The Command Control codes specify the command type being sent to the slave, whereas the Response Control codes specify the response to be read from the slave. The Data Control codes specify the operation on fields of a disk sector and their orientation with respect to the start of a sector.

4.2.2 Information transfer

The interface uses the Double Octet mode to transfer 16-bit information. Data is transferred in the Data Streaming mode; Commands and Response are transferred in the Interlocked mode.

4.2.3 Data transfers

The master reads and writes on the disk by issuing Data Controls while staying oriented with the rotation of the disk. No addresses or octet counts are involved with the Data Controls. Operations are on whole fields and include field read, write, and skip operations. Field sizes include any master-managed Error Correcting Codes (ECC) and Cyclic Redundancy Codes (CRC).

4.2.4 Format Control

The organization of sectors and the number of sectors per track is controlled by a Format Specification, which may be mutually derived by both the slave and the master. This specification dictates the number of fields per sector, the length of each field, and the number of sectors per track.

4.3 Responsibility

4.3.1 Master

The master performs the following functions:

- Data buffering;
- Data management — Interleaving;
- Header management;
- Defect management — defect skipping, revectoring, spare sectors;
- Error detection and/or correction — Retries, ECC, CRC;
- Command generation.

4.3.2 Slave

The slave performs the following functions:

- Sectoring — Hard, soft, or both; variable or fixed;
- Formatting — Multiple fields, variable or fixed;
- Gap management — Phase Lock Oscillator (PLO), pads, interfield gaps, write-read recovery;
- Read Gate and Write Gate control;
- Phase Lock Oscillator (PLO), bit, and octet synchronization and pattern writing;
- Header verification for write (Format 1 only);
- Command execution;
- Response generation;
- Error detection and/or correction (optional);
- Dual port (optional).

5 Physical Interface Considerations

The Physical Interface is used as defined in ISO/IEC 9318-1, with the interpretations and additions defined in the following sub clauses.

5.1 Information transfer

5.1.1 Octet Mode

All Information Transfers (Commands, Responses, and Data) are transmitted in the double octet (16-bit) mode. Even-numbered octets are transmitted on BUS A and odd-numbered octets are transmitted on BUS B; i.e., the octet on BUS A is considered as being transmitted before the octet on BUS B.

For Command and Response information, bit 7 of an octet is the most significant bit (MSB) and bit 0 is the least significant bit (LSB). The most significant octets are transferred first in multioctet numeric parameters.

For data information, there is no definition of significance to the ordering of bits or octets. The order in which the octets are read is the same as that in which they are written.

Bit 7 on BUS A is the first recorded bit on the disk.

5.1.2 Transfer Mode

Command/Response information is always transferred in the Interlocked mode. Data information is always transferred in the Data Streaming mode. The transfer modes cannot be changed.

The Request Transfer Settings octet response reflects capabilities and settings of command/ response transfers in Double Octet and Interlocked modes.

5.1.3 Termination of transfers

The Information Transfer sequence may be terminated by either the slave or master.

5.1.4 Data streaming

Data streaming enables high transfer rates over long cables and is well suited to data transfers by synchronous disk. This is accomplished by not interlocking the SYNC IN and SYNC OUT, which eliminates a round-trip transmission delay.

Data streaming shall be used for data transfers as defined in ISO/IEC 9318-1, with the following interpretations:

- The SYNC IN pulses occur at the data rate of the disk and are generated at the rate of one per double octet.

- The nominal duty cycle of the SYNC IN is 50%.
- Upon recognizing a SYNC IN, the master returns a SYNC OUT after a delay not exceeding one double octet time at the maximum cable length measured at the slave connector.

During data output transfers, the slave shall prefetch data by initiating the SYNC IN pulses n octet times prior to the writing of the first data octet on the disk in order to account for transmission and master delays.

The value of n is dependent on master, slave, and transmission delays and the data rate of the slave. The slave shall require at least an n octet first in, first out (FIFO) buffer to account for delays less than maximum (n octet times). If data is not available in the slave when it must be written on the disk, a data underrun condition exists, the transfer is terminated and the Successful Information Transfer bit in the Slave Status octet may be set to zero.

Drives that support ECC/CRC and have that feature enabled shall complete the sector and write uncorrectable ECC/CRC if a data underrun condition occurs during a disk write.

5.2 Bus Octets

The bus octets defined in ISO/IEC 9318-1 shall be used as described, with the additions described in this sub clause. All valid state transitions shall be implemented by the slave.

5.2.1 Unsupported Bus Octets

The following bus octets are not supported:

- Facility Selection. Slave does not acknowledge selection;
- Request Facility Interrupts. Slave does not acknowledge request for facility interrupts;.
- Bus Acknowledge. Slave transmits zeroes on BUS B.

5.2.2 Bus Control Octet

The Bus Control octets define the direction and type of information transfer in bits 7-6 and the command to be executed in bits 5-0.

Bit	Description
7	0 = Operation Command/Operation Response 1 = Data
6	0 = Information Out 1 = Information In
5-0	Encoded Bus Control Command and Response Controls; see 7.1 Data Controls; see 7.2 and 7.3.

5.2.3 Master Status Octet

If the Master Status Octet indicates an unsuccessful information transfer following a Read Status Response, the slave shall not clear the pending Status Response conditions.

Bit	Description
7	Successful Information Transfer
6	Bus Parity Error
5-0	0

5.2.4 Slave Status Octet

The Slave Status provides information to the master on the results of the preceding Information Transfer in bits 7-5 and the command in bits 4-0 and 6. See 8.1 for further details on the Slave Status octet.

Bit	Description
7	Successful Information Transfer
6	Bus Parity Error
5	Odd Octet Transfer
4	Time-Dependent Operation
3-0	Encoded Operation Ending Status

5.2.5 Request Interrupts Octet

The organization of the Request Interrupt Octet is as follows:

Bit	Description
7	0
6	<u>Report Busy Status</u> : All slaves that are Busy shall place their bit-significant Address Octet Response on BUS B.
5	<u>Report Ready Status</u> : All slaves that are Ready shall place their bit-significant Address Octet Response on BUS B.
4	<u>Master Power Fail Alert</u> : The master is informing the slaves that it has detected that power is failing. The slaves shall acknowledge by placing their bit-significant Address Octet Response on BUS B after they have taken appropriate action to permit a graceful termination of activity.
3	<u>Power On Status Request</u> : All slaves with power on (but not necessarily ready) shall place their bit-significant Address Octet Response on BUS B.
2	<u>Status Pending Interrupt</u> : Slaves with Class 3 Interrupt pending shall respond by placing their bit-significant Address Octet Response on BUS B.
1	<u>RPS Interrupt</u> : Slaves with Class 2 Interrupt pending shall respond by placing their bit-significant Address Octet Response on BUS B.
0	<u>Command Completion Interrupt</u> : Slaves with Class 1 Interrupt pending shall respond by placing their bit-significant Address Octet Response on BUS B.

The slave shall respond to a Request Interrupt Octet with a bit-significant Address Octet Response (defined in 5.2.6).

5.2.5.1 Types of Interrupts

The slave asserts three interrupt classes defined in ISO/IEC 9318-1. The assertion of interrupt bit settings upon receipt of a Request Interrupts or Request Slave Interrupts sequence shall not be disabled by the Load Slave Functions.

5.2.5.1.1 Class 1 Command Completion Interrupt

This interrupt is asserted when a command is completed successfully and the Time-Dependent Operation bit of the Slave Status following the transfer of the command was set. The Command Completion Interrupt is not asserted for a Load Position command if the RPS Interrupt is to be asserted because of a valid RPS Target Sector Address parameter. The assertion of a Command Completion Interrupt is disabled by any of the following:

- Slave accepts any Bus Control;
- Slave is reset with a Selective Reset octet from this port with bit 1 (Reset Logical) set;
- Slave is reset with a Selective Reset from either port with bit 2 (Reset Slave) set.

5.2.5.1.2 Class 2 RPS Interrupt

This interrupt is asserted on each disk revolution during the time specified by the Load Position command or Load RPS Target Sector Address command. The assertion of the RPS Interrupt shall be disabled by any of the following:

- Setting X'FFFF' as the RPS Target Sector Address parameter;
- Slave accepts a Data Control;
- Slave accepts a Load Format Specification;
- Slave is reset while in neutral with a Selective Reset from either port with bit 1 (Reset Logical) set. If switched to the alternate port the assertion of the RPS Interrupt shall not be affected;
- Slave is reset with a Selective Reset from either port with bit 2 (Reset Slave) set.

5.2.5.1.3 Class 3 Status Pending Interrupt

This interrupt is asserted when there is a status exception in the Status Response that must be reported to the master. The assertion of Status Pending Interrupt is disabled by any of the following:

- Read Status Response with a Successful Information Transfer bit set in Master Status;
- Slave is reset with a Selective Reset Octet from this port with bit 1 (Reset Logical) set;
- Slave is reset with a Selective Reset Octet from either port with bit 2 (Reset Slave) set.

5.2.6 Address Octet Response

The slave shall respond to a Request Interrupt Octet or Selection Octet with an Address Octet Response that has the following organization:

Bit	Description
7	Slave 7
6	Slave 6
5	Slave 5
4	Slave 4
3	Slave 3
2	Slave 2
1	Slave 1
0	Slave 0

5.2.7 Selective Reset Octet

The receipt of this octet causes a Selective Reset of the type defined in bits 3-0. The following Reset Controls are defined:

Bit	Description	
7	Indicates Selective Reset Octet	
6-4	Slave address	
3	Slave Release	The slave shall release its interface drivers in the same manner as it would upon recognition of the MAINT state. The drivers are to remain released on the port over which the Reset was received until recognition of another Reset with this bit cleared.
2	Reset Slave	The slave shall be reset in the same way as when power on.
1	Reset Logical Interface	The Logical Interface for the port shall be reset. The slave's common resources that are not switched to the alternate port shall be reset. The Format Specification is not affected.
0	Reset Physical Interface	The Physical Interface for the port shall be reset.

5.2.8 Selection Octet

The Selection Octet bits 6-4 specify the slave address. Bits 3-1 are not supported and shall be set to zero. If bit 0, Priority Select, is set, the slave shall cease any operations with the alternate port, cancel any reserve on the alternate port, and attempt to honor selection from the selecting port.

Bit	Description
7	0
6-4	Slave Address
3-1	0
0	Priority Select

5.2.9 Request Transfer Settings Octet

The slave shall respond with a Transfer Settings Octet when it receives a Request Transfer Settings Octet that has the following organization:

Bit	Description
7	1
6-4	Slave Address
3-0	0

5.2.10 Slave Transfer Settings Octet

The slave shall respond to a Request Transfer Settings Octet from the master with a Transfer Settings Octet that has the following organization:

Bit	Description
7	0 = Transfer Settings Octet
6	0/1 = Maintenance Mode 1/2
5	1 = Double Octet Mode
4	0 = Interlocked Transfer
3	0 = Slave is not capable of Data Streaming transfers
2	1 = Slave is capable of Interlocked transfers
1	1 = Slave is capable of transferring in Double Octet Mode
0	0 = Slave is not capable of transferring in Single Octet Mode

The transfer settings reported are those reflecting the capabilities and settings for the slave during Command/Responses Information Transfers.

5.2.11 Request Slave Interrupts Octet

The slave shall respond with a Slave Interrupts Octet when it receives a Request Slave Interrupts Octet. The organization of a Request Slave Interrupts Octet shall be as follows:

Bit	Description
7	1
6-4	Slave address
3	1
2-0	0

5.2.12 Slave Interrupts Octet

The slave shall respond with a Slave Interrupts Octet when it receives a Request Slave Interrupts Octet. The organization of the Slave Interrupts Octet shall be as follows:

Bit	Description
7	Reserved, set to zero.
6	<u>Busy</u> : Busy is an indication that the slave is unable to respond by the master's request; i.e., it is currently executing a Bus Control (previously issued from this port or the alternate port), or is reserved by the alternate port.
5	<u>Ready</u> : Ready is an indication that the slave is operational and able to accept any supported Command or Data Bus Control code that is in context.
4	Reserved, set to zero.
3	<u>Priority Selected</u> : This bit shall be set when a successful Priority Select has occurred during selection of the alternate port. This bit shall be reset at the end of the Request Slave Interrupts sequence during which it was reported.
2	<u>Status Pending Interrupt</u> : This interrupt shall be asserted when there is a status exception to be reported in the Status Response.
1	<u>RPS Interrupt</u> : This interrupt shall be asserted during the time on each disk revolution that the RPS Pulse is valid (the data heads are in the requested area defined by the RPS Target Sector Address and optional parameters, if any).
0	<u>Command Completion Interrupt</u> : This interrupt shall be asserted when a command, previously transferred with the Time-Dependent Operation bit set in the Slave Status octet is completed successfully. The Command Completion Interrupt is not asserted on a Load Position command that includes a valid RPS Target Sector Address parameter.

5.3 ATTENTION IN signal

The ATTENTION IN signal shall be asserted by an unselected slave when the RPS, Command Completion or Status Pending Interrupts are asserted, or if the slave is enabled to assert ATTENTION IN upon "No Longer Busy" (a Busy to Not Busy condition occurs). See 5.2.5.1 for a description of interrupts.

The Load Slave Function command provides for enabling and disabling the individual interrupts from asserting ATTENTION IN, on a port basis.

All ATTENTION IN assertions shall be enabled upon power-on Reset or Selective Reset (Reset Slave) except for "No Longer Busy".