
Identification cards — Test methods —
Part 6:
Proximity cards

Cartes d'identification — Méthodes d'essai —
Partie 6: Cartes de proximité



Reference number
ISO/IEC 10373-6:2011(E)

AVA Documents
Document Sharing Hub
© ISO/IEC 2011

PDF disclaimer

This PDF file may contain embedded typefaces. In accordance with Adobe's licensing policy, this file may be printed or viewed but shall not be edited unless the typefaces which are embedded are licensed to and installed on the computer performing the editing. In downloading this file, parties accept therein the responsibility of not infringing Adobe's licensing policy. The ISO Central Secretariat accepts no liability in this area.

Adobe is a trademark of Adobe Systems Incorporated.

Details of the software products used to create this PDF file can be found in the General Info relative to the file; the PDF-creation parameters were optimized for printing. Every care has been taken to ensure that the file is suitable for use by ISO member bodies. In the unlikely event that a problem relating to it is found, please inform the Central Secretariat at the address given below.



COPYRIGHT PROTECTED DOCUMENT

© ISO 2011

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either ISO at the address below or ISO's member body in the country of the requester.

ISO copyright office
Case postale 56 • CH-1211 Geneva 20
Tel. + 41 22 749 01 11
Fax + 41 22 749 09 47
E-mail copyright@iso.org
Web www.iso.org

Published in Switzerland

Contents

Foreword	vi
1 Scope	1
2 Normative references	1
3 Terms, definitions, symbols and abbreviated terms	2
3.1 Terms and definitions	2
3.2 Symbols and abbreviated terms	3
4 Default items applicable to the test methods	5
4.1 Test environment	5
4.2 Pre-conditioning	5
4.3 Default tolerance	6
4.4 Spurious Inductance	6
4.5 Total measurement uncertainty	6
5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters	6
5.1 Minimum requirements for measurement instruments	6
5.1.1 Oscilloscope	6
5.2 Calibration coil	6
5.2.1 Size of the calibration coil card	6
5.2.2 Thickness and material of the calibration coil card	7
5.2.3 Coil characteristics	7
5.3 Test PCD assembly	7
5.3.1 Test PCD antenna	8
5.3.2 Sense coils	8
5.3.3 Assembly of Test PCD	8
5.4 Reference PICC	9
5.4.1 Dimensions of the Reference PICC	9
5.4.2 Reference PICC construction	10
5.4.3 Reference PICC resonance frequency tuning	11
6 Test of ISO/IEC 14443-1 parameters	12
6.1 PCD tests	12
6.1.1 Alternating magnetic field	12
6.2 PICC tests	12
6.2.1 Alternating magnetic field	12
6.2.2 Static electricity test	13
7 Test of ISO/IEC 14443-2 parameters	14
7.1 PCD tests	14
7.1.1 PCD field strength	14
7.1.2 PCD field strength supporting operation with "Class 1" PICCs	15
7.1.3 Power transfer PCD to PICC	16
7.1.4 Modulation index and waveform	16
7.1.5 Load modulation reception	17
7.2 PICC tests	18
7.2.1 PICC transmission	18
7.2.2 PICC reception	19
7.2.3 PICC resonance frequency (informative)	21
7.2.4 "Class 1" PICC maximum loading effect	21
8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters	22
8.1 PCD tests	22
8.2 PICC tests	22

Annex A (normative) Test PCD Antenna.....	23
A.1 Test PCD Antenna layout including impedance matching network.....	23
A.2 Impedance matching network	27
A.2.1 Impedance matching network for a bit rate of $f_c/128$.....	27
A.2.2 Impedance matching network for bit rates of $f_c/64$, $f_c/32$ and $f_c/16$.....	28
Annex B (informative) Test PCD Antenna tuning.....	29
Annex C (normative) Sense coil	31
C.1 Sense coil layout.....	31
C.2 Sense coil assembly.....	32
Annex D (normative) Reference PICC antenna layout	33
Annex E (normative) Modulation index and waveform analysis tool	34
E.1 Overview	34
E.2 Sampling.....	34
E.3 Filtering.....	35
E.4 Envelope generation	36
E.5 Envelope smoothing	36
E.6 Modulation index determination	36
E.7 Timing determination	36
E.8 Overshoot and undershoot determination.....	37
E.9 Program of the modulation index and waveform analysis tool (informative)	37
E.9.1 structures.h	38
E.9.2 fftm.h.....	39
E.9.3 fftm.c.....	40
E.9.4 hilbert.h.....	44
E.9.5 hilbert.c.....	45
E.9.6 functs.c	52
Annex F (informative) Program for the evaluation of the spectrum	80
Annex G (normative) Additional PICC test methods	85
G.1 PICC-test-apparatus and accessories	85
G.1.1 Emulating the I/O protocol.....	85
G.1.2 Generating the I/O character timing in reception mode	85
G.1.3 Measuring and monitoring the RF I/O protocol	85
G.1.4 Protocol Analysis.....	85
G.1.5 RFU fields	85
G.2 Relationship of test methods versus base standard requirement	86
G.3 Test method for initialization of the PICC Type A	87
G.3.1 Introduction	87
G.3.2 Scenario G.1: Polling.....	87
G.3.3 Testing of the PICC Type A state transitions.....	88
G.3.4 Scenario G.13: Handling of Type A anticollision.....	109
G.3.5 Handling of RATS	110
G.3.6 Handling of PPS request.....	110
G.3.7 Scenario G.20: Handling of FSD.....	111
G.4 Test method for initialization of the PICC Type B	112
G.4.1 Introduction	112
G.4.2 Scenario G.21: Polling.....	112
G.4.3 Scenario G.22: PICC Reception.....	113
G.4.4 Testing of the PICC Type B state transitions.....	114
G.4.5 Scenario G.28: Handling of Type B anticollision.....	124
G.4.6 Handling of ATTRIB	126
G.4.7 Scenario G.31: Handling of Maximum Frame Size	127
G.5 Test methods for logical operation of the PICC Type A or Type B	127
G.5.1 Introduction	127
G.5.2 PICC reaction to ISO/IEC 14443-4 Scenarios	128
G.5.3 Handling of PICC error detection	138
G.5.4 PICC reaction on CID.....	140
G.5.5 PICC reaction on NAD	142

G.6	Reported results	143
Annex H	(normative) Additional PCD test methods	147
H.1	PCD-test-apparatus and accessories	147
H.1.1	Test method	147
H.1.2	PCD-test-apparatus structure	147
H.1.3	PCD-test-apparatus interface	148
H.1.4	Emulating the I/O protocol	148
H.1.5	Generating the I/O character timing in transmission mode	148
H.1.6	Measuring and monitoring the RF I/O protocol	149
H.1.7	Protocol Analysis	149
H.1.8	Protocol activation procedure	149
H.1.9	Scenario	149
H.1.10	UT, LT and PCD behavior	150
H.1.11	Relationship of test methods versus base standard requirement	151
H.2	Type A specific test methods	151
H.2.1	Frame delay time PICC to PCD	151
H.2.2	Request Guard Time	152
H.2.3	Handling of bit collision during ATQA	153
H.2.4	Handling of anticollision loop	153
H.2.5	Handling of RATS and ATS	157
H.2.6	Handling of PPS response	160
H.2.7	Frame size selection mechanism	161
H.2.8	Handling of Start-up Frame Guard Time	163
H.2.9	Handling of the CID during activation by the PCD	164
H.3	Type B specific test methods	165
H.3.1	I/O transmission timing	165
H.3.2	Frame size selection mechanism	166
H.3.3	Handling of the CID during activation by the PCD	167
H.4	Test method for logical operations of the PCD	169
H.4.1	Handling of the polling loop	169
H.4.2	Reaction of the PCD to request for waiting time extension	170
H.4.3	Error detection and recovery	173
H.4.4	Handling of NAD during chaining	182
H.5	Continuous monitoring of packets sent by the PCD	183
H.5.1	RFU fields	183
H.5.2	RFU values	183
H.5.3	R-block	183
H.5.4	S-block	183
H.5.5	PCB	183
H.5.6	Type A initialization frames	183
H.5.7	Apparatus	183
H.5.8	Procedure	183
H.5.9	Test report	184
H.6	Reported results	184
Annex I	(normative) High bit rate selection test methods for PCD	188
I.1	Apparatus	188
I.2	Procedure	188
I.2.1	Procedure for Type A	188
I.2.2	Procedure for Type B	193
	Bibliography	199

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of the joint technical committee is to prepare International Standards. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

ISO/IEC 10373-6 was prepared by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 17, *Cards and personal identification*.

This second edition cancels and replaces the first edition (ISO/IEC 10373-6:2001), which has been technically revised. It also includes the Amendments ISO/IEC 10373-6:2001/Amd.1:2007, ISO/IEC 10373-6:2001/Amd.2:2003, ISO/IEC 10373-6:2001/Amd.3:2006, ISO/IEC 10373-6:2001/Amd.4:2006 and ISO/IEC 10373-6:2001/Amd.5:2007.

ISO/IEC 10373 consists of the following parts, under the general title *Identification cards — Test methods*:

- *Part 1: General characteristics*
- *Part 2: Cards with magnetic stripes*
- *Part 3: Integrated circuit cards with contacts and related interface devices*
- *Part 5: Optical memory cards*
- *Part 6: Proximity cards*
- *Part 7: Vicinity cards*
- *Part 8: USB-ICC*
- *Part 9: Optical memory cards — Holographic recording method*

Identification cards — Test methods —

Part 6: Proximity cards

1 Scope

ISO/IEC 10373 defines test methods for characteristics of identification cards according to the definition given in ISO/IEC 7810. Each test method is cross-referenced to one or more base standards, which can be ISO/IEC 7810 or one or more of the supplementary standards that define the information storage technologies employed in identification card applications.

NOTE 1 Criteria for acceptability do not form part of ISO/IEC 10373, but will be found in the International Standards mentioned above.

NOTE 2 Test methods defined in this part of ISO/IEC 10373 are intended to be performed separately. A given proximity card or object, or proximity coupling device, is not required to pass through all the tests sequentially.

This part of ISO/IEC 10373 defines test methods which are specific to proximity cards and objects, and proximity coupling devices, defined in ISO/IEC 14443-1:2008, ISO/IEC 14443-2:2010, ISO/IEC 14443-3:— and ISO/IEC 14443-4:2008. ISO/IEC 10373-1 defines test methods which are common to one or more integrated circuit card technologies and other parts deal with other technology-specific tests.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7810:2003, *Identification cards — Physical characteristics*

ISO/IEC 14443-1:2008, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 1: Physical characteristics*

ISO/IEC 14443-2:2010, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 2: Radio frequency power and signal interface*

ISO/IEC 14443-3:—¹⁾, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 3: Initialization and anticollision*

ISO/IEC 14443-4:2008, *Identification cards — Contactless integrated circuit cards — Proximity cards — Part 4: Transmission protocol*

IEC 61000-4-2:2008, *Electromagnetic compatibility (EMC) — Part 4-2: Testing and measurement techniques — Electrostatic discharge immunity test*

1) To be published.

3 Terms, definitions, symbols and abbreviated terms

For the purposes of this document, the terms, definitions, abbreviations and symbols given in ISO/IEC 14443-1:2008, ISO/IEC 14443-2:2010, ISO/IEC 14443-3:—, ISO/IEC 14443-4:2008 and the following apply.

NOTE Elements in bold square brackets [] are optional definitions.

3.1 Terms and definitions

3.1.1

base standard

standard which the test method is used to verify conformance to

3.1.2

CascadeLevels

number of cascade levels of the PICC

3.1.3

"Class 1" PICC

PICC whose antenna is located as defined in ISO/IEC 14443-1:2008 and which passes the "Class 1" PICC maximum loading effect test defined in 7.2.4

3.1.4

Command Set

set describing the PICC commands during initialization and anticollision

NOTE See ISO/IEC 14443-3:—, 6.4 for PICC Type A and ISO/IEC 14443-3:—, 7.5 for PICC Type B.

3.1.5

Mute

no response within a specified timeout, e.g. expiration of FWT

3.1.6

PICC States

different PICC states during initialization and anticollision

NOTE See ISO/IEC 14443-3:—, 6.3 for PICC Type A and ISO/IEC 14443-3:—, 7.4 for PICC Type B.

3.1.7

Scenario

defined typical protocol and application specific communication to be used with the test methods defined in this part of ISO/IEC 10373

3.1.8

Test Initial State

TIS

element from PICC States that is the PICC state before performing a specific PICC command from Command Set

3.1.9

test method

method for testing characteristics of identification cards for the purpose of confirming their compliance with International Standards

3.1.10**Test Target State****TTS**

element from PICC States that is the PICC state after performing a specific PICC command from Command Set

3.2 Symbols and abbreviated terms

(xxxxx)b	Data bit representations
'XY'	Hexadecimal notation, equal to XY in base 16
ATA(cid)	Answer to ATTRIB, i.e. (mbli+cid CRC_B), with mbli an arbitrary hex value (see ISO/IEC 14443-3:—, 7.11)
ATTRIB(cid, fsdi)	Default ATTRIB command with PUPI from ATQB, CID = cid and Maximum Frame Size Code value = fsdi i.e. ('1D' PUPI cid fsdi '01 00' CRC_B)
DUT	Device under test
ESD	Electrostatic Discharge
$I(c)_n(\text{inf } [,CID = cid] [,NAD = nad] [,~CRC])$	ISO/IEC 14443-4 I-block with chaining bit $c \in \{1,0\}$, block number $n \in \{1,0\}$ and information field inf. By default no CID and no NAD will be transmitted. If $CID = cid \in \{0 \dots 15\}$ is specified, it will be transmitted as second parameter. If $NAD = nad \in \{0 \dots 'FF'\}$ is specified it will be transmitted as third parameter (or second parameter if no CID is transmitted). If the literal '~CRC' is not specified, a valid CRC corresponding to the type of the PICC will be transmitted by default (i.e. CRC_A or CRC_B)
IUT	Implementation Under Test (ISO/IEC 9646); within the scope of this part of ISO/IEC 10373, IUT represents the PCD under the test
LT	Lower Tester (ISO/IEC 9646), the PICC-emulation part of the PCD-test-apparatus
m	Modulation index
Mute	No response within a specified timeout
N/A	Not applicable
PPS(cid, dri, dsi)	Default PPS request with CID = cid, DRI = dri and DSI = dsi, i.e. ('D' + cid '11' dsi × 4 + dri CRC_A)
$R(\text{ACK } [,CID = cid] [,~CRC])_n$	ISO/IEC 14443-4 R(ACK) Block with block number n. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
$R(\text{NAK } [,CID = cid] [,~CRC])_n$	ISO/IEC 14443-4 R(NAK) Block with block number n. The definition of the optional CID and ~CRC symbols is as described in the $I(c)_n$ block above
RATS(cid, fsdi)	Default RATS command with CID = cid and FSDI value = fsdi i.e. ('E0' fsdi × 16 + cid CRC_A)
READY(I)	READY state in cascade level I, $I \in \{1, 2, 3\}$; e.g. READY(2) is a PICC cascade level 2

READY*(I)	READY* state in cascade level I, $I \in \{1, 2, 3\}$; e.g. READY*(2) is a PICC cascade level 2
REQB(N)	REQB command with N as defined in ISO/IEC 14443-3:—, 7.7.4
S(WTX)(WTXM [,CID = cid][,~CRC])	ISO/IEC 14443-4 S(WTX) block with parameter WTXM. The definition of the optional CID and ~CRC symbols is as described in the I(c) _n block above
S(DESELECT [,CID = cid [,~CRC])	ISO/IEC 14443-4 S(DESELECT) block. The definition of the optional CID and ~CRC symbols is as described in the I(c) _n block above
SAK(cascade)	the SELECT(I) answer with the cascade bit (bit 3) set to (1)b
SAK(complete)	the SELECT(I) answer with the cascade bit (bit 3) set to (0)b
SEL(c)	Select code of level c (i.e. SEL(1) = '93', SEL(2) = '95', SEL(3) = '97')
SELECT(I)	SELECT command of cascade level I, i.e. SELECT(1) = ('93 70' UIDTX ₁ BCC CRC_A) SELECT(2) = ('95 70' UIDTX ₂ BCC CRC_A) SELECT(3) = ('97 70' UIDTX ₃ BCC CRC_A)
SLOTMARKER(n)	Slot-MARKER command with slot number n, i.e. (16 × (n – 1) + 5 CRC_B)
TB-PDU	Transmission Block Protocol Data Unit, which consists of either I-block, R-block or S-block
TEST_COMMAND1(1)	Default test command consisting of one unchained I-block NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n), n > 1	Default test command consisting of n chained I-blocks (PCD chaining) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND1(n) _k	INF field of k'th I-block chain of TEST_COMMAND1(n) NOTE This command depends on the negotiated maximum frame size value of the PICC.
TEST_COMMAND2(n), n > 1	Default test command which expects a response consisting of n chained I-blocks NOTE This command depends on the negotiated maximum frame size value of the PCD.
TEST_COMMAND3	Default test command consisting of one I-block which needs more than FWT time for execution
TEST_RESPONSE1(n)	INF field of the response to TEST_COMMAND1(n) NOTE This response is assumed to be always unchained.
TEST_RESPONSE2(n)	Response to TEST_COMMAND2(n)

	NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE2(n) _k	INF field of k'th I-block chain of TEST_RESPONSE2(n)
	NOTE This response depends on the negotiated maximum frame size value of the PCD.
TEST_RESPONSE3	Response I-block to TEST_COMMAND3
	NOTE This response is always assumed to be unchained.
TM- PDU	Test Management Protocol Data Unit (ISO/IEC 9646-1, PDU)
UIDTX _i	Transmitted UID 32-bit data at cascade level i (see Table 1)
UT	Upper Tester (ISO/IEC 9646), the master part of the PCD-test-apparatus
UT_APDU	Upper Tester Application Protocol Data Unit: a packet of data to be sent by the PCD to the LT through the RF interface
WUPB(N)	WUPB command with N as defined in ISO/IEC 14443-3:—, 7.7.4
~X	Bit sequence consisting of the inverted bits of bit sequence X or any other bit sequence different from X
X[[a..b]]	Bit subsequence of bit sequence X consisting of the bits between position a and b included. If a > b then the sequence is empty
X[[n]]	Bit at position n of bit sequence X. First bit is at position 1
X[n]	Byte at position n of bit sequence X. First byte is at position 1 (i.e. X[n] = X[[(n - 1) × 8 + 1..n × 8]])

Table 1 — Mapping from UID to UIDTX

Cascade level	Single UID PICC	Double UID PICC	Triple UID PICC
UIDTX ₁	UID0 UID1 UID2 UID3	'88' UID0 UID1 UID2	'88' UID0 UID1 UID2
UIDTX ₂	---	UID3 UID4 UID5 UID6	'88' UID3 UID4 UID5
UIDTX ₃	---	---	UID6 UID7 UID8 UID9

4 Default items applicable to the test methods

4.1 Test environment

Unless otherwise specified, testing shall take place in an environment of temperature 23 °C ± 3 °C (73 °F ± 5 °F) and of relative humidity 40 % to 60 %.

4.2 Pre-conditioning

No environmental pre-conditioning of PICCs or PCDs is required by the test methods in this document.

4.3 Default tolerance

Unless otherwise specified, a default tolerance of $\pm 5\%$ shall be applied to the quantity values given to specify the characteristics of the test equipment (e.g. linear dimensions) and the test method procedures (e.g. test equipment adjustments).

4.4 Spurious Inductance

Resistors and capacitors should have negligible inductance.

4.5 Total measurement uncertainty

The total measurement uncertainty for each quantity determined by these test methods shall be stated in the test report.

Basic information is given in ISO/IEC Guide 98-3:2008.

5 Apparatus and circuits for test of ISO/IEC 14443-1 and ISO/IEC 14443-2 parameters

This clause defines the test apparatus and test circuits for verifying the operation of a PICC or a PCD according to ISO/IEC 14443-1:2008 and ISO/IEC 14443-2:2010. The test apparatus includes:

- Measurement instruments (see 5.1);
- Calibration coil (see 5.2);
- Test PCD assembly (see 5.3);
- Reference PICC (see 5.4).

These are described in the following clauses.

5.1 Minimum requirements for measurement instruments

5.1.1 Oscilloscope

The digital sampling oscilloscope shall be capable of sampling at a rate of at least 500 million samples per second with a resolution of at least 8 bits at optimum scaling and shall have an overall minimum bandwidth of 250 MHz. The oscilloscope should have the capability to output the sampled data as a text file to facilitate mathematical and other operations such as windowing on the sampled data using external software programs (see Annexes E and F).

NOTE The overall bandwidth is the combination of oscilloscope and probing system bandwidth.

5.2 Calibration coil

This clause defines the size, thickness and characteristics of the calibration coil.

5.2.1 Size of the calibration coil card

The calibration coil card shall consist of an area which has the height and width of an ID-1 type defined in ISO/IEC 7810:2003 containing a single turn coil concentric with the card outline (see Figure 1).

ISO/IEC 7810 ID-1 outline

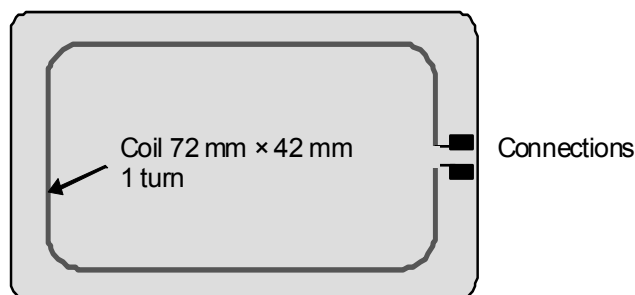


Figure 1 — Calibration coil

5.2.2 Thickness and material of the calibration coil card

The thickness of the calibration coil card shall be less than that of an ID-1 card. It shall be constructed of a suitable insulating material.

5.2.3 Coil characteristics

The coil on the calibration coil card shall have one turn. The outer size of the coil shall be 72 mm × 42 mm with corner radius 5 mm. Relative dimensional tolerance shall be $\pm 2\%$.

NOTE 1 The area over which the field is integrated is approximately 3000 mm².

The coil shall be made as a printed coil on printed circuit board (PCB) plated with 35 µm copper. Track width shall be 500 µm with a relative tolerance of $\pm 20\%$. The size of the connection pads shall be 1,5 mm × 1,5 mm.

NOTE 2 At 13,56 MHz the approximate inductance is 250 nH and the approximate resistance is 0,4 Ω.

A high impedance oscilloscope probe with an input admittance equivalent to a parallel capacitance $C_p < 14$ pF and a parallel resistance $R_p > 9$ kΩ at 13,56 MHz shall be used to measure the (open circuit) voltage induced in the coil. The resonance frequency of the calibration coil and connecting leads shall be above 60 MHz.

NOTE 3 A parasitic capacitance of the probe assembly of less than 35 pF normally ensures for the whole set a resonant frequency greater than 60 MHz.

The open circuit calibration factor for this coil is 0,32 V (rms) per A/m (rms) [Equivalent to 900 mV (peak-to-peak) per A/m (rms)].

NOTE 4 The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.3 Test PCD assembly

The test PCD assembly shall consist of a 150 mm diameter test PCD antenna and two parallel sense coils: sense coil a and sense coil b. The test set-up is shown in Figure 2. The sense coils shall be connected such that the signal from one coil is in opposite phase to the other. The 10 Ω potentiometer P1 serves to fine adjust the balance point when the sense coils are not loaded by a PICC or any magnetically coupled circuit. The capacitive load of the probe including its parasitic capacitance shall be less than 14 pF.

NOTE 1 The capacitance of the connections and of the oscilloscope probe should be kept to a minimum for reproducibility.

NOTE 2 In order to avoid any unintended misalignment in case of an unsymmetrical set-up the tuning range of the potentiometer P1 is only 10 Ω . If the set-up cannot be compensated by the 10 Ω potentiometer P1 the overall symmetry of the set-up should be checked.

NOTE 3 The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

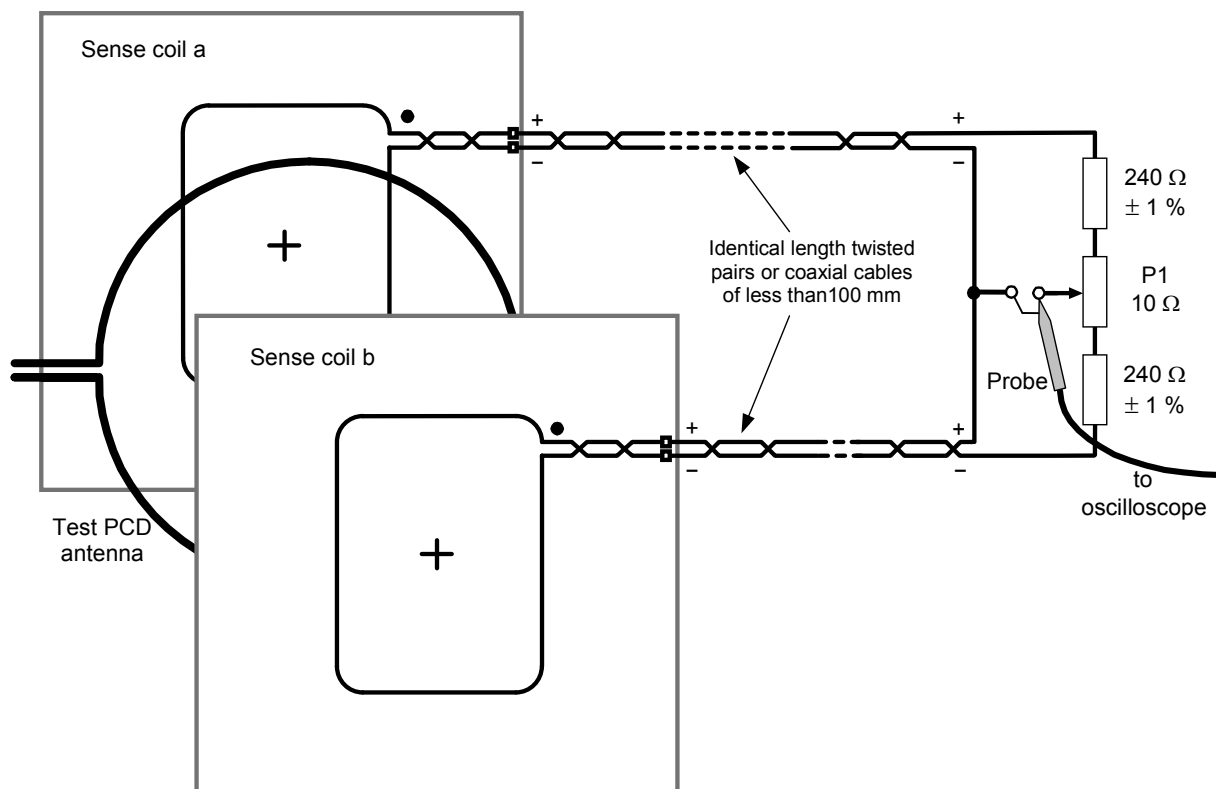


Figure 2 — Test set-up (principle)

5.3.1 Test PCD antenna

The test PCD antenna shall have a diameter of 150 mm and its construction shall conform to the drawings in Annex A.

The matching of the test PCD antenna should be accomplished by using an impedance analyzer or a network analyzer or a LCR meter. If either an impedance analyzer or a network analyzer or a LCR meter is not available, then the matching may be accomplished with the procedure given in Annex B.

5.3.2 Sense coils

The size of the sense coils shall be 100 mm $\times$ 70 mm with corner radius 10 mm. The sense coil construction shall conform to the drawings in Annex C.

5.3.3 Assembly of Test PCD

The sense coils and test PCD antenna shall be assembled parallel and with the sense and antenna coils coaxial and such that the distance between the active conductors is 37,5 mm as shown in Figure 3. The dimensional tolerance shall be better than $\pm 0,5$ mm. The distance between the coil in the DUT and the calibration coil shall be equal with respect to the coil of the test PCD antenna.

NOTE These distances are chosen to represent the typical operating distance of the PICC.

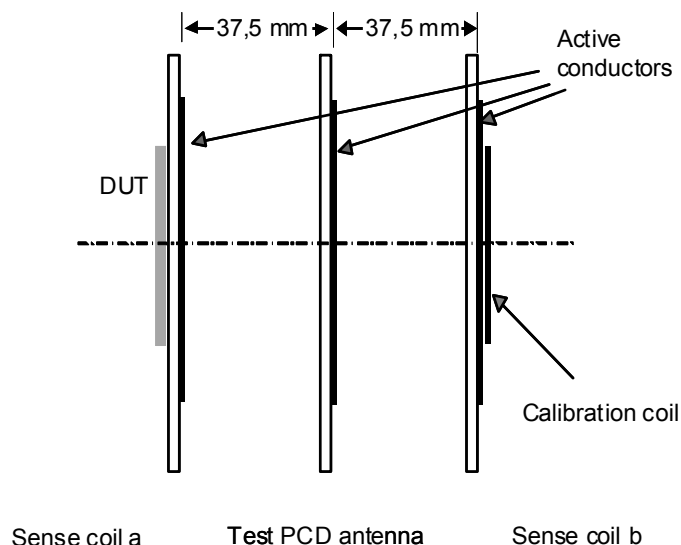


Figure 3 — Test PCD assembly

5.4 Reference PICC

A Reference PICC is defined to test the ability of a PCD to:

- generate a field strength of at least $H_{\min}$ and not exceeding $H_{\max}$;
- transfer power to a PICC;
- transmit a modulated signal to a PICC;
- receive a load modulation signal from the PICC;

in its operating volume.

5.4.1 Dimensions of the Reference PICC

The Reference PICC shall consist of an area containing the coils which has the height and width defined in ISO/IEC 7810:2003 for ID-1 type. An area external to this, containing the circuitry which emulates the required PICC functions, shall be appended in such a way as to allow insertion into the test set-ups and so as to cause no interference to the tests. The dimensions shall be as in Figure 4.

Outline ISO/IEC 7810
ID-1 type

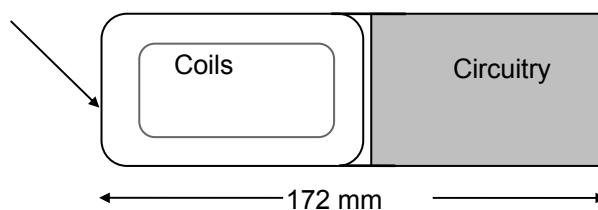


Figure 4 — Reference PICC dimensions

5.4.2 Reference PICC construction

The Reference PICC construction is defined in Annex D.

The Reference PICC shall have a circuit diagram as defined in Figure 5 and component values as defined in Table 2.

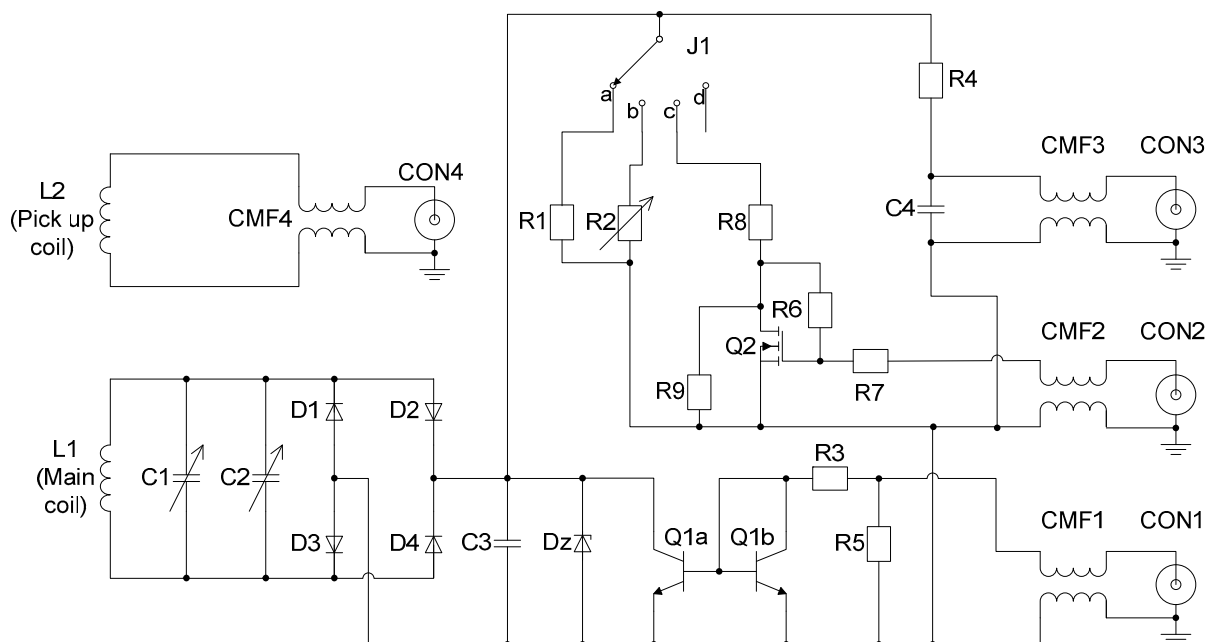


Figure 5 — Reference PICC circuit diagram

NOTE Position 'd' of jumper J1 is RFU.

Table 2 — Reference PICC components list

Component	Value	Component	Value
L1	See Annex D	C1	7 pF – 50 pF ^b
L2	See Annex D	C2	3 pF – 10 pF ^b
R1	1,8 kΩ	C3	27 pF
R2	0 kΩ – 2 kΩ ^a	C4	1 nF
R3	220 Ω	D1, D2, D3, D4	BAR43S or equivalent ^c
R4	51 kΩ	Dz	BZX84, 15 V or equivalent ^c
R5	51 Ω	Q1a, Q1b	BCV61A or equivalent
R6	500 kΩ	Q2	BSS83 or equivalent
R7	110 kΩ	CMF1, CMF2, CMF3, CMF4	ACM3225 -102-2P or equivalent
R8	51 Ω	CON1, CON2, CON3, CON4	RF connector
R9	1,5 kΩ		

^a A multi-turn potentiometer (turns ≥ 10) should be used.

^b Q - factor shall be higher than 100 at 13,56 MHz.

^c Care should be taken on parameters C_j (Junction capacitance), C_p (Package capacitance), L_s (Series inductance) and R_s (Series resistance) of equivalent diodes. Note that these values may not be available in the datasheet.

At CON1 the load modulation signal shall be applied. The load modulation can be determined in test PCD assembly. When not used, the load modulation signal generator shall be disconnected or set to 0 V.

With the voltage at CON2 the Reference PICC load can be adjusted until the required DC voltage shows at CON3.

The Reference PICC DC voltage shall be measured at CON3 using a high impedance voltmeter and the connection wires should be twisted or coaxial.

The PCD waveform parameters are picked up at CON4 using a high impedance oscilloscope probe. The high impedance oscilloscope probe ground connection should be as short as possible, less than 20 mm or coaxial connection.

5.4.3 Reference PICC resonance frequency tuning

The Reference PICC resonance frequency shall be calibrated with the following procedure:

- a) Set jumper J1 to position 'a'.
- b) Connect the calibration coil directly to a signal generator and the Reference PICC connector CON3 to a high impedance voltmeter. Connect all the other connectors to the same equipment as used for the tests.
- c) Locate the Reference PICC at a distance $d = 10$ mm above the calibration coil with the axes of the two coils (calibration coil and Reference PICC main coil) being congruent (see Figure 6).
- d) Drive the calibration coil with a sine wave set to the desired resonance frequency.
- e) Adjust the Reference PICC capacitors C1 and C2 to get maximum DC voltage at CON3.
- f) Adjust the signal generator drive level to read a DC voltage of 6 V at CON3.
- g) Repeat steps e) and f) until the maximum voltage after step e) is 6 V.
- h) Calibrate the Test PCD assembly to produce the $H_{\min}$ operating condition on the calibration coil.
- i) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 6 V measured at connector CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.
- j) Repeat steps b) to g) with the obtained value of R2.

NOTE Instead of a signal generator a vector network analyzer may be used if sufficient power is provided to produce 6 V at CON3 while reaching the maximum resistive part of the measured complex impedance of the calibration coil.

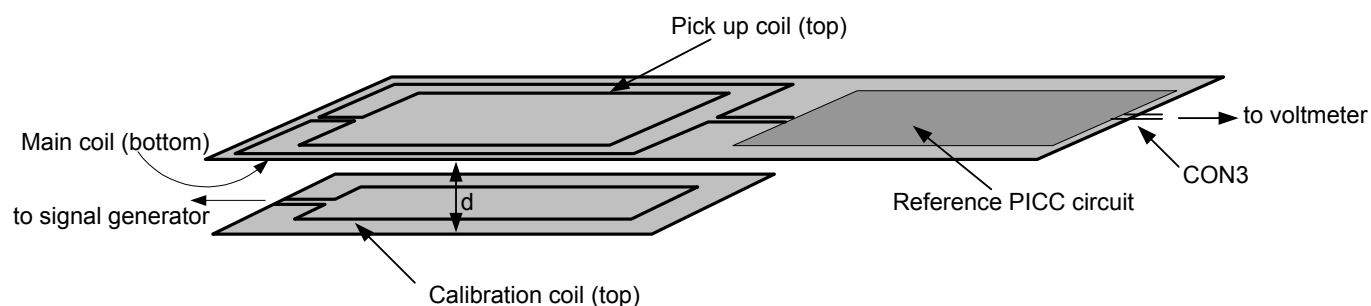


Figure 6 — Reference PICC frequency tuning set-up (principle)

6 Test of ISO/IEC 14443-1 parameters

6.1 PCD tests

6.1.1 Alternating magnetic field

6.1.1.1 Purpose

This test determines that the PCD generates a field not higher than the average value specified in ISO/IEC 14443-1:2008, in any possible PICC position.

6.1.1.2 Test procedure

- a) Tune the Reference PICC to 19 MHz as described in 5.4.3 steps a) to g).
- b) Calibrate the Test PCD assembly to produce the average field value specified in ISO/IEC 14443-1:2008, 4.4 on the calibration coil.
- c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at connector CON3. The operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING - R2 value should be between 55 and 65 Ω .

- d) Position the Reference PICC in any possible PICC position. The DC voltage at CON3 shall not exceed 3 V.
- e) If exceeded, use the same conversion factor to measure the maximum and average DC voltage and convert in field strength to check the maximum and the average field values specified in ISO/IEC 14443-1:2008, 4.4 in 30 s period.

6.1.1.3 Test report

The test report shall give the DC voltage measured at CON3.

6.2 PICC tests

6.2.1 Alternating magnetic field

The purpose of this test is to check the behavior of the PICC in relation to alternating magnetic field exposure at 13,56 MHz.

6.2.1.1 Apparatus

The test PCD assembly shall be used to produce the alternating magnetic field.

6.2.1.2 Test procedure

The procedure is as follows.

- a) Adjust the RF power delivered by the signal generator to the test PCD antenna to a field strength of 10 A/m (rms) as measured by the calibration coil.
- b) Place the PICC under test in the DUT position and readjust immediately the RF drive into the test PCD antenna to the required field strength if necessary.

- c) After 5 min, remove the PICC from the DUT position for at least 5 s.
- d) Adjust the RF power delivered by the signal generator to the test PCD antenna to a field strength of 12 A/m (rms) as measured by the calibration coil.
- e) Place the PICC under test in the DUT position and readjust immediately the RF drive into the test PCD antenna to the required field strength if necessary.
- f) Apply for 5 min an ASK 100 % modulation to this field with the following duty cycle:
 - 5 s at 0 A/m (rms);
 - 25 s at 12 A/m (rms).
- g) Check that the PICC operates as intended.

6.2.1.3 Test report

The test report shall state whether or not the PICC operates as intended.

6.2.2 Static electricity test

The purpose of this test is to check the behavior of the card IC in relation to electrostatic discharge (ESD) exposure in the test sample. The PICC under test is exposed to a simulated electrostatic discharge (ESD, human body model) and its basic operation checked following the exposure (see Figure 7).

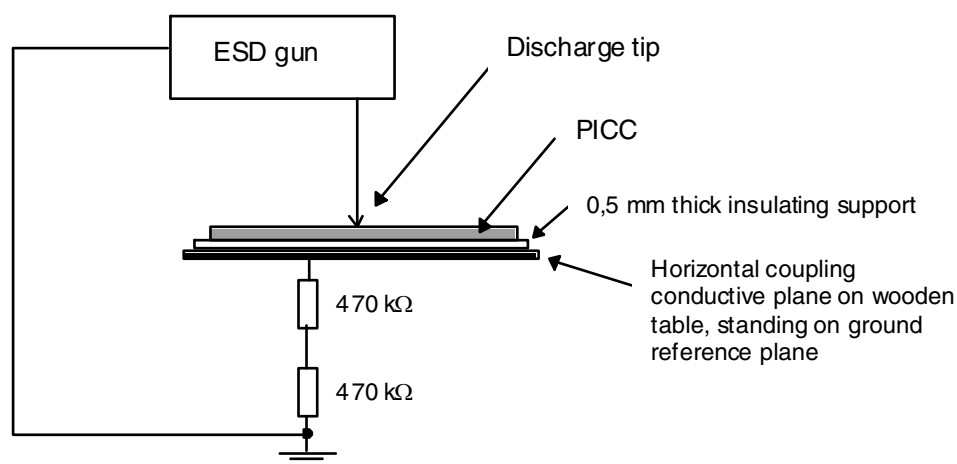


Figure 7 — ESD test circuit

6.2.2.1 Apparatus

Refer to IEC 61000-4-2:2008.

- a) Main specifications of the ESD generator:
 - energy storage capacitance: 150 pF $\pm$ 10 %;
 - discharge resistance: 330 Ω $\pm$ 10 %;
 - charging resistance: between 50 M Ω and 100 M Ω ;
 - rise time: 0,7 ns to 1 ns.

b) Selected specifications from the optional items:

- type of equipment: table top equipment;
- discharge method: direct application of air discharge to the equipment under test;
- discharge electrodes of the ESD generator: Round tip probe of 8 mm diameter.

6.2.2.2 Test procedure

Connect the ground pin of the apparatus to the conductive plate upon which the PICC is placed.

Apply the discharge successively in normal polarity to each of the 20 test zones shown in Figure 8. Then repeat the same procedure with reversed polarity. Allow a cool-down period between successive pulses of at least 10 s.

WARNING - If the PICC includes contacts, the contacts should face up and the zone which includes contacts should not be exposed to this discharge.

Check that the PICC operates as intended at the end of the test.

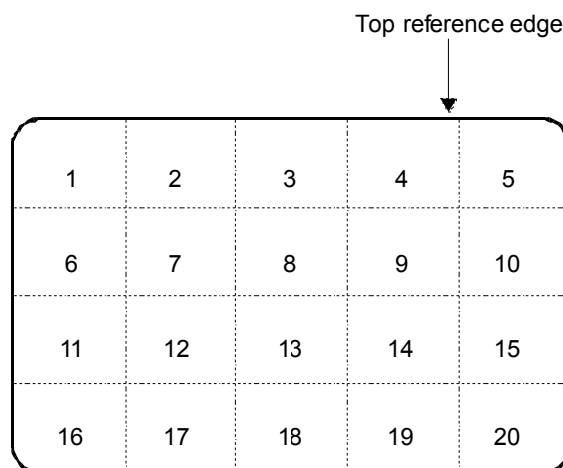


Figure 8 — Test zones on PICC for ESD test

6.2.2.3 Test report

The test report shall state whether or not the PICC operates as intended.

7 Test of ISO/IEC 14443-2 parameters

7.1 PCD tests

All the tests described below will be done in the operating volume as defined by the PCD manufacturer.

7.1.1 PCD field strength

7.1.1.1 Purpose

This test measures the field strength produced by a PCD in its operating volume.

NOTE The test takes account of PICC loading of the PCD.

7.1.1.2 Test procedures

Procedure for $H_{\max}$ test:

- a) Tune the Reference PICC to 19 MHz as described in 5.4.3 steps a) to g).
- b) Calibrate the Test PCD assembly to produce the $H_{\max}$ operating condition on the calibration coil.
- c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of 3 V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING - R2 value should be between 75 and 85 Ω . Check this range at least once before using the alternative method.

- d) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall not exceed 3 V.

Procedure for $H_{\min}$ test:

- a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3.
- b) Calibrate the Test PCD assembly to produce the $H_{\min}$ operating condition on the calibration coil.
- c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 3 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the voltage on CON2 is adjusted to obtain a DC voltage of 3 V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING - R2 value should be between 400 and 550 Ω . Check this range at least once before using the alternative method.

- d) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall exceed 3 V.

7.1.1.3 Test report

The test report shall give the DC voltage measured at CON3 for R2 or variable load resistor adjusted to $H_{\min}$ and $H_{\max}$ field strength under the conditions applied.

7.1.2 PCD field strength supporting operation with "Class 1" PICCs

7.1.2.1 Purpose

The following additional PCD test is necessary for interoperability between PCDs and "Class 1" PICCs. This test is similar to PCD field strength test specified in 7.1.1 but uses a Reference PICC adjusted to apply a higher loading effect.

NOTE The loading effect of "Class 1" PICCs is lower than the loading effect of the Reference PICC used in this test (see "Class 1" PICC maximum loading effect test in 7.2.4). This guarantees that $H_{\min}$ is supplied in the "Class 1" PCD operating volume if additionally the "Class 1" PICCs' antenna size and location are similar to the Reference PICC (Annex D) antenna size and location. For PICCs with different antenna size and/or location other classes may be created with, for each class, a corresponding Reference PICC.

7.1.2.2 Test procedure

The PCD field strength test defined in 7.1.1, procedure for $H_{\min}$ test, shall be repeated with the Reference PICC calibrated to obtain 6 V at CON3 instead of 3 V.

NOTE The Reference PICC calibration used in this test is the same as the calibration defined in 7.1.1.

7.1.2.3 Test report

The test report shall give the DC voltage measured at CON3 for R2 or variable load resistor adjusted to $H_{\min}$ field strength under the conditions applied.

NOTE The volume in which the DC voltage exceeds 6 V defines the "Class 1" operating volume.

7.1.3 Power transfer PCD to PICC

7.1.3.1 Purpose

This test is used to determine that the PCD is able to supply a certain power to a PICC placed anywhere within the defined operating volume.

7.1.3.2 Test procedure

- a) Tune the Reference PICC to 19 MHz as described in 5.4.3 steps a) to g) and leave jumper J1 to position 'a'.
- b) Position the Reference PICC within the defined operating volume of the PCD under test. The DC voltage at CON3 shall exceed 3 V.

7.1.3.3 Test report

The test report shall give the DC voltage at CON3 measured within the defined operating volume under the defined conditions.

7.1.4 Modulation index and waveform

7.1.4.1 Purpose

This test is used to determine the index of modulation of the PCD field as well as the rise and fall times and the overshoot values as defined in ISO/IEC 14443-2:2010.

7.1.4.2 Test procedure

- a) Position the calibration coil at an arbitrary position in the defined operating volume and display the induced coil voltage on a suitable oscilloscope. Determine the modulation index and waveform characteristics using the analysis tool defined in Annex E.
- b) Tune the Reference PICC to 16,5 MHz as described in 5.4.3 steps a) to g) and switch the jumper J1 to position 'c'.
- c) Place the Reference PICC at a particular position in the PCD operating volume.
- d) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of 3 V or optionally 6 V when supporting "Class 1" at that position.

NOTE 1 If a DC voltage of 6 V cannot be reached at the selected position, the maximum achievable voltage should be used for the test.

- e) If the unmodulated voltage on CON4, measured with a suitable oscilloscope (requirements see 5.1.1) is below 1 V (peak-to-peak), use an alternative pick up coil to determine the waveform characteristic.

NOTE 2 This alternative pick up coil should have a "figure of 8" shape with 15 mm radius positioned farthest away from the Reference PICC to minimize coupling and as close as possible to the PCD antenna to maximize induced voltage.

- f) Determine the modulation index and waveform characteristic from the voltage at CON4 or at the alternative pick up coil using the analysis tool defined in Annex E.
- g) Repeat steps c) to f) for various positions within the operating volume.

NOTE 3 The selected position of the calibration coil within the operating volume is not expected to affect the results.

NOTE 4 The Reference PICC load does not represent the worst case loading effect of a PICC. Higher loading effects may be achieved with resonance frequencies closer to carrier frequency (e.g. 15 MHz or 13,56 MHz).

7.1.4.3 Test report

The test report shall give the measured modulation index of the PCD field, the rise and fall times and overshoot values, within the defined operating volume in unloaded and loaded conditions.

7.1.5 Load modulation reception

7.1.5.1 Purpose

This test is used to verify that a PCD correctly detects the load modulation of a PICC which conforms to ISO/IEC 14443-2:2010.

7.1.5.2 Test procedure

The Reference PICC and its calibration procedure allow the sensitivity of a PCD to load modulation to be assessed. The Reference PICC does not emulate the loading effect of all types of PICC.

- a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3 and switch the jumper J1 to position 'c'.
- b) Place the Reference PICC at a particular position in the PCD operating volume.
- c) Apply and adjust a DC voltage at CON2 to obtain a DC voltage at connector CON3 of 3 V or optionally 6 V when supporting "Class 1" at that position.
- d) Increase the modulation signal amplitude at CON1 to produce responses until the PCD detects at least 10 of them consecutively.
- e) Place the Reference PICC in the DUT position on the Test PCD assembly.
- f) Adjust the Test PCD assembly to produce a field strength H which gives the same voltage at CON3 and note the corresponding field strength by reading the calibration coil voltage.
- g) Measure the Reference PICC load modulation amplitude V_{LMA} as described in 7.2.1 and compare it with the standard limit associated with the noted field strength. This measured V_{LMA} level defines the PCD sensitivity criterion in order to compare with the standard limit to perform these test measurements.
- h) Repeat steps b) to g) for various positions within the operating volume.
- i) Repeat steps a) to h) with Reference PICC resonance frequency 15 MHz.

Any position in which the PCD sensitivity is above the standard limit shall be considered out of the operating volume.

NOTE 1 The test coverage may be expanded by using additional resonance frequencies below 13,56 MHz such as 12 MHz and 10 MHz.

NOTE 2 The PCD sensitivity should be below the standard limit to ensure good reception of the PICC load modulation.

NOTE 3 This test does not check that the PCD reception is independent of the phase of the PICC load modulation. Consequently, it cannot guarantee the correct reception of any PICC compliant with ISO/IEC 14443-2:2010.

7.1.5.3 Test report

The test report shall give the PCD load modulation sensitivity for the tested positions.

7.2 PICC tests

7.2.1 PICC transmission

7.2.1.1 Purpose

The purpose of this test is to determine the load modulation amplitude V_{LMA} of the PICC within the operating field range $[H_{min}, H_{max}]$ as specified in ISO/IEC 14443-2:2010. Also the functionality of the PICC for Type A and Type B within their corresponding modulation ranges as defined in ISO/IEC 14443-2:2010 shall be determined.

NOTE No load modulation test is required for bit rates of $fc/64$, $fc/32$ and $fc/16$.

7.2.1.2 Test procedure

Step 1: The load modulation test circuit of Figure 2 and the Test PCD assembly of Figure 3 are used.

Adjust the RF power delivered by the signal generator to the test PCD antenna to the required field strength as measured by the calibration coil. Connect the output of the load modulation test circuit of Figure 2 to a digital sampling oscilloscope. The 10 Ω potentiometer P1 shall be trimmed to minimize the residual carrier. This signal shall be at least 40 dB lower than the signal obtained by shorting one sense coil.

WARNING - The PICC load modulation amplitude test should be done by increasing the field strength from 0 A/m (rms), thus checking correct PICC operation starting from H_{min} .

Step 2: The PICC under test shall be placed in the DUT position, concentric with sense coil a. The RF drive into the test PCD antenna shall be re-adjusted to the required field strength.

A REQA or a REQB command sequence as defined in ISO/IEC 14443-3:— shall be sent by the Test PCD to obtain a signal or load modulation response from the PICC.

Display a segment of at least six cycles of the waveform of the subcarrier load modulation on the digital sampling oscilloscope and store the sampled data in a file for analysis by a computer software program (see Annex F).

NOTE 1 Care should be taken to apply a proper synchronization method for low amplitude load modulation.

Fourier transform with a Bartlett window exactly six subcarrier cycles of the sampled modulation waveform using suitable computer software (as the one given in Annex F). Use a discrete Fourier transformation with a scaling such that a pure sinusoidal signal results in its peak magnitude. In order to minimize transient effects, avoid analyzing a subcarrier cycle immediately following a non-modulating period or a phase shift of the subcarrier. The discrete Fourier transformation shall be done at the sidebands frequencies generated by the PICC under test, i.e. $fc + fs$ and $fc - fs$.

The resulting peak amplitudes of the upper and lower sidebands at $fc + fs$ and $fc - fs$ shall be above the value defined in ISO/IEC 14443-2:2010, 8.2.2.

NOTE 2 For Type B PICC load modulation test, the oscilloscope FFT (Fast Fourier Transform) option may also be used on a large number of subcarrier cycles with neither transient effect nor phase shift (i.e. on a stable part of synchronization time TR1 as defined in ISO/IEC 14443-2:2010, 9.2.5 or on a stable part of SOF as defined in ISO/IEC 14443-3:—, 7.1.4).

7.2.1.3 Test report

The test report shall give the measured peak amplitudes of the upper and lower sidebands at $f_c + f_s$ and $f_c - f_s$ and the applied fields and modulations.

7.2.2 PICC reception

7.2.2.1 Purpose

The purpose of this test is to verify the ability of the PICC to receive the PCD commands.

7.2.2.2 PICC Type A

7.2.2.2.1 Test conditions for a bit rate of $fc/128$

Three test conditions are defined with timings at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2010, Figure 4:

- Condition 1: maximum $t_1 - t_2$ and maximum t_3 , no overshoot;
- Condition 2: minimum achievable (with Test PCD assembly) $t_1 - t_2$ and maximum associated t_3 , maximum overshoot;
- Condition 3: minimum achievable (with Test PCD assembly) t_3 and maximum associated $t_1 - t_2$, maximum overshoot.

NOTE The carrier amplitude at the end of t_2 should be less than 4 %.

These 3 tests conditions shall be tested at least using $H_{\min}$ and $H_{\max}$ whereas parameter t_1 is the maximum specified value when condition 1 and condition 3 are used and is the minimum specified value when condition 2 is used.

7.2.2.2.2 Test conditions for bit rates of $fc/64$, $fc/32$ and $fc/16$

Three test conditions are defined with timings at the border of the Type A PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2010, Figures 7, 8 and 9:

- Condition 1: maximum $t_1 - t_5$ and maximum t_6 , no overshoot;
- Condition 2: minimum achievable (with Test PCD assembly) $t_1 - t_5$ and maximum associated t_6 , maximum overshoot;
- Condition 3: minimum achievable (with Test PCD assembly) t_6 and maximum associated $t_1 - t_5$, maximum overshoot.

These 3 tests conditions shall be tested at least using $H_{\min}$ and $H_{\max}$ whereas:

- parameter a is the maximum specified value when condition 1 is used and is the minimum achievable value for the Test PCD assembly when condition 2 and condition 3 are used;
- parameter t_1 is the maximum specified value when condition 1 and condition 3 are used and is the minimum specified value when condition 2 is used.

7.2.2.2.3 Test procedure

Under the conditions defined in 7.2.2.2.1 the PICC shall answer to a REQA with ATQA.

A PICC supporting the optional $fc/64$ bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of $fc/64$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/64$.

A PICC supporting the optional $fc/32$ bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of $fc/32$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/32$.

A PICC supporting the optional $fc/16$ bit rate shall operate under the conditions defined in 7.2.2.2.2 after selection of a bit rate of $fc/16$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/16$.

7.2.2.3 PICC Type B

7.2.2.3.1 Test conditions

Three test conditions are defined with timings at the border of the Type B PICC modulation waveform timing parameters zone defined in ISO/IEC 14443-2:2010, Figures 14, 15, 16 and 17:

- Condition 1: maximum t_f and maximum t_r , no undershoot and overshoot;
- Condition 2: minimum achievable (with Test PCD assembly) t_f and maximum associated t_r , maximum undershoot and overshoot;
- Condition 3: minimum achievable (with Test PCD assembly) t_r and maximum associated t_f , maximum undershoot and overshoot.

These 3 tests conditions shall be tested at least using:

- $H_{\min}$ and $H_{\max}$;
- minimum and maximum modulation index m for the associated field strength applied (see ISO/IEC 14443-2:2010, Figure 13).

7.2.2.3.2 Test procedure

Under the conditions defined in 7.2.2.3.1 the PICC operating at a bit rate of $fc/128$ shall answer to a REQB with ATQB.

A PICC supporting the optional $fc/64$ bit rate shall operate under the conditions defined in 7.2.2.3.1 after selection of a bit rate of $fc/64$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/64$.

A PICC supporting the optional $fc/32$ bit rate shall operate under the conditions defined in 7.2.2.3.1 after selection of a bit rate of $fc/32$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/32$.

A PICC supporting the optional $fc/16$ bit rate shall operate under the conditions defined in 7.2.2.3.1 after selection of a bit rate of $fc/16$. This PICC shall respond correctly to an I-block transmitted at a bit rate of $fc/16$.

7.2.2.4 Test report

The test report shall confirm the intended operation at the mandatory $fc/128$ bit rate. For PICCs supporting one or more of the optional high bit rates the test report shall confirm the intended operation at the supported bit rates. Used test conditions shall be mentioned in the test report.

7.2.3 PICC resonance frequency (informative)

7.2.3.1 Purpose

The test may be used to measure the resonance frequency of a PICC.

When two or more PICCs are placed in the same PCD energizing field, the resonance frequency of each PICC decreases.

Care should be taken in designing each PICC resonance frequency.

WARNING - The resonance frequency may depend on the field strength used during the measurement.

7.2.3.2 Procedure

The resonance frequency of a PICC is measured by using an impedance analyzer or a network analyzer or a LCR-meter connected to a calibration coil. The PICC should be placed on the calibration coil at a distance of 10 mm, with the axes of the two coils being congruent. The resonance frequency is that frequency at which the resistive part of the measured complex impedance is at maximum.

7.2.3.3 Test report

When applied the test report shall give the PICC resonance frequency and the measurement conditions.

7.2.4 "Class 1" PICC maximum loading effect

7.2.4.1 Purpose

The following additional PICC test is necessary for interoperability between PCDs and "Class 1" PICCs defined in ISO/IEC 14443-1:2008.

NOTE This test improves interoperability only if the "Class 1" PICCs antenna size and location are similar to the Reference PICC (Annex D) antenna size and location. For PICCs with different antenna size and/or location other classes may be created with, for each class, a corresponding reference PICC.

7.2.4.2 Test procedure

The PICC loading effect at $H_{\min}$ shall be measured using the test PCD assembly. It shall not exceed the loading effect of the Reference PICC tuned to 13,56 MHz and calibrated to obtain 6 V at CON3 at $H_{\min}$. The procedure of this substitution method is as follows.

- a) Tune the Reference PICC to 13,56 MHz as described in 5.4.3.
- b) Calibrate the Test PCD assembly to produce the $H_{\min}$ operating condition on the calibration coil.
- c) Place the Reference PICC into the DUT position on the Test PCD assembly. Switch the jumper J1 to position 'b' and adjust R2 to obtain a DC voltage of 6 V measured at connector CON3. Alternatively, jumper J1 may be set to position 'c' and the applied voltage on CON2 is adjusted to obtain a DC voltage of 6 V at connector CON3. In both cases, the operating field condition shall be verified by monitoring the voltage on the calibration coil and adjusted if necessary.

WARNING - R2 value should be between 900 and 1000 Ω . Check this range at least once before using the alternative method.

- d) Remove the Reference PICC.
- e) Place the PICC under test into the DUT position on the Test PCD assembly.

f) Measure the field strength H_C monitored by the calibration coil.

The field strength H_C shall be greater than $H_{\min}$.

7.2.4.3 Test report

The test report shall give the value H_C .

8 Test of ISO/IEC 14443-3 and ISO/IEC 14443-4 parameters

8.1 PCD tests

See Annex H and Annex I.

8.2 PICC tests

See Annex G.

Annex A (normative)

Test PCD Antenna

A.1 Test PCD Antenna layout including impedance matching network

Figures A.1, A.2, A.3 and A.4 illustrate Test PCD antenna layout. Drawings are not to scale.

The antenna coil track width is 1,8 mm (except for through-plated holes).

Starting from the impedance matching network there are crossovers every 45 °.

Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 µm copper.

NOTE 1 The layout of the impedance matching network is informative.

NOTE 2 Such printed circuit boards and R_{ext} resistors are available from various commercial sources.

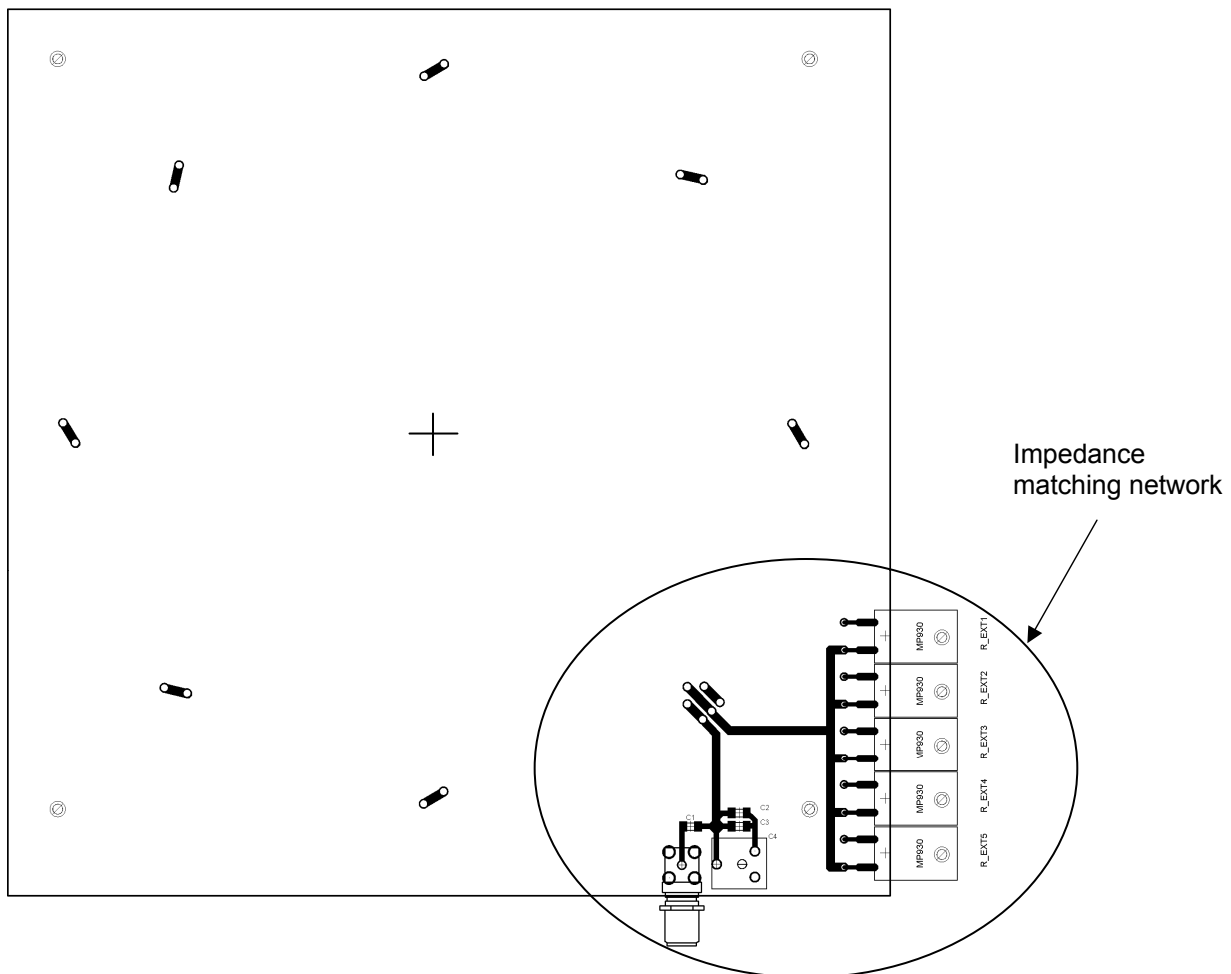


Figure A.1 — Test PCD antenna layout including impedance matching network for a bit rate of $fc/128$ (View from front)

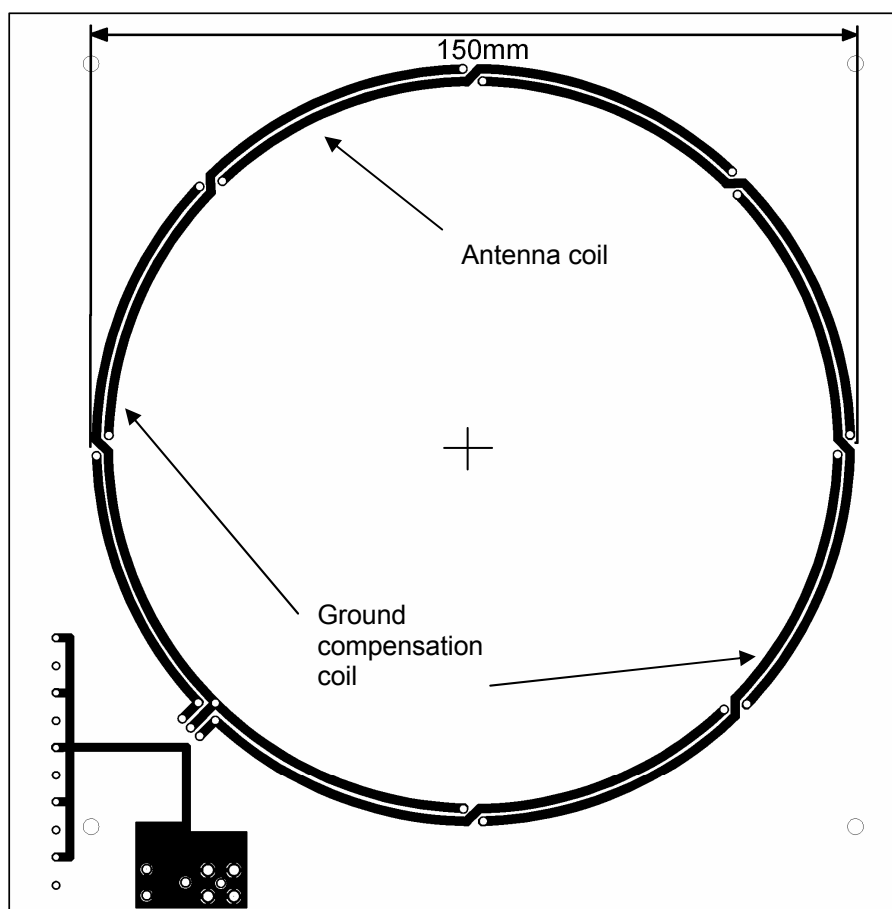


Figure A.2 — Test PCD antenna layout including impedance matching network for a bit rate of $f_c/128$
(View from back)

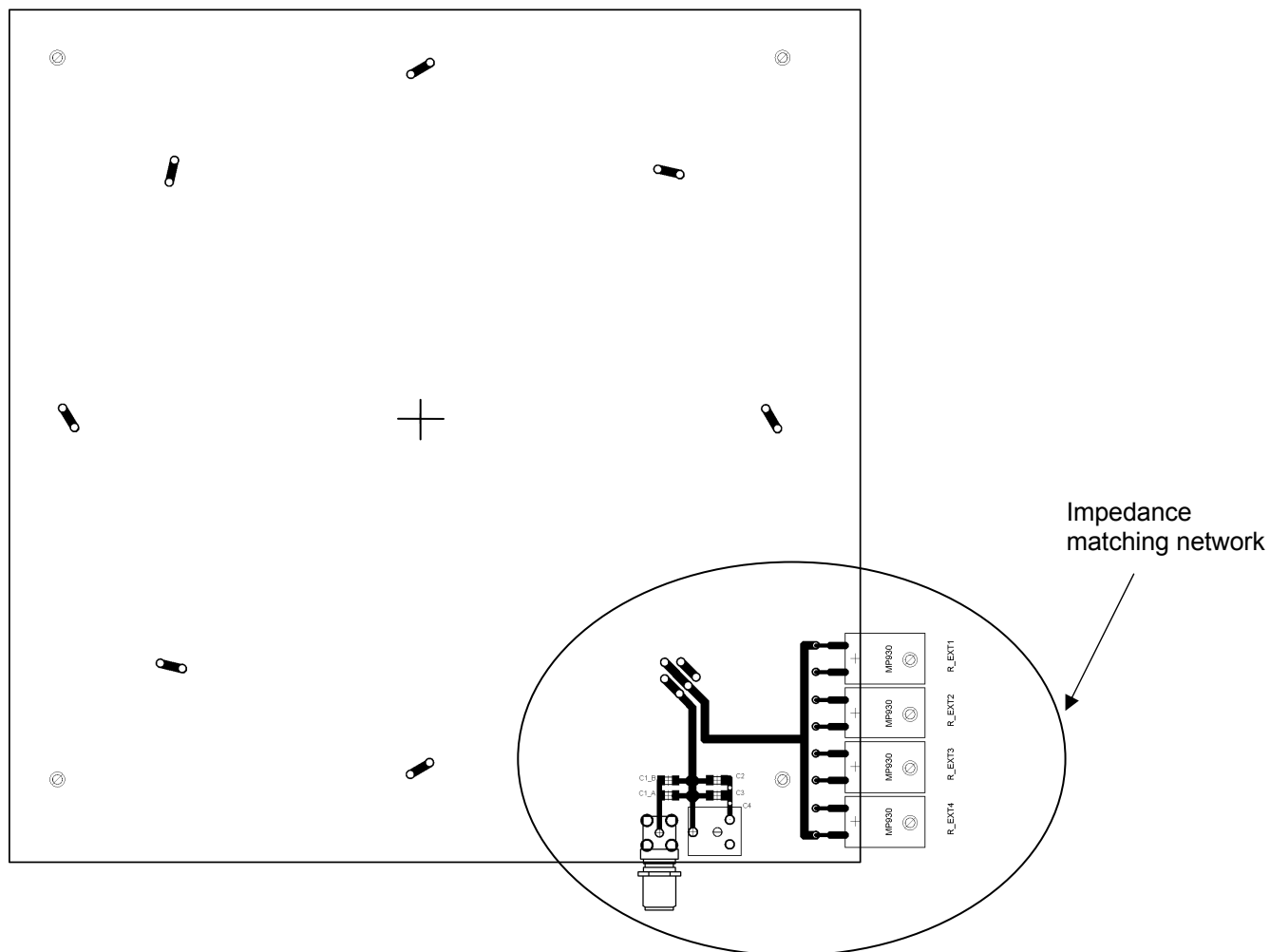


Figure A.3 — Test PCD antenna layout including impedance matching network for bit rates of $fc/64$, $fc/32$ and $fc/16$ (View from front)

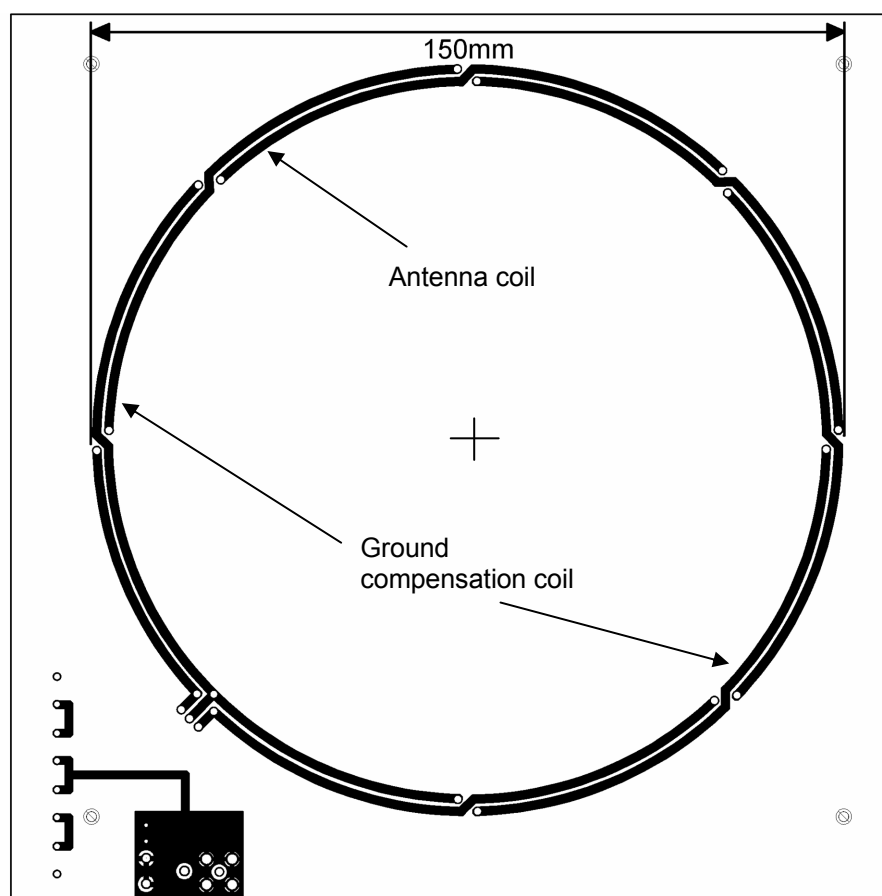


Figure A.4 — Test PCD antenna layout including impedance matching network for bit rates of $fc/64$, $fc/32$ and $fc/16$ (View from back)

A.2 Impedance matching network

The antenna impedance (R_{ant} , L_{ant}) is adapted to the signal generator output impedance ($Z = 50 \Omega$) by a matching circuit (see A.2.1 and A.2.2). The capacitors C1, C1a, C1b, C2 and C3 have fixed values. The input impedance phase can be adjusted with the variable capacitor C4.

The test PCD assembly as defined in 5.3 and in this Annex is intended to be used for time limited measurements, to avoid any overheating of the individual components. If the test is run continuously, heat dissipation shall be improved. Care shall be taken to keep maximum voltages and maximum heat dissipation within the specified limits of the individual components.

Two impedance matching networks are described: the impedance matching network for a bit rate of $fc/128$ and the impedance matching network for bit rates of $fc/64$, $fc/32$ and $fc/16$. Table A.1 contains their use cases.

Table A.1 — Impedance matching network use cases

Impedance matching network	Magnetic field capability	Bit rate capability
For a bit rate of $fc/128$	Up to 12 A/m (rms)	Only $fc/128$
For bit rates of $fc/64$, $fc/32$ and $fc/16$	Up to 7,5 A/m (rms)	From $fc/128$ to $fc/16$

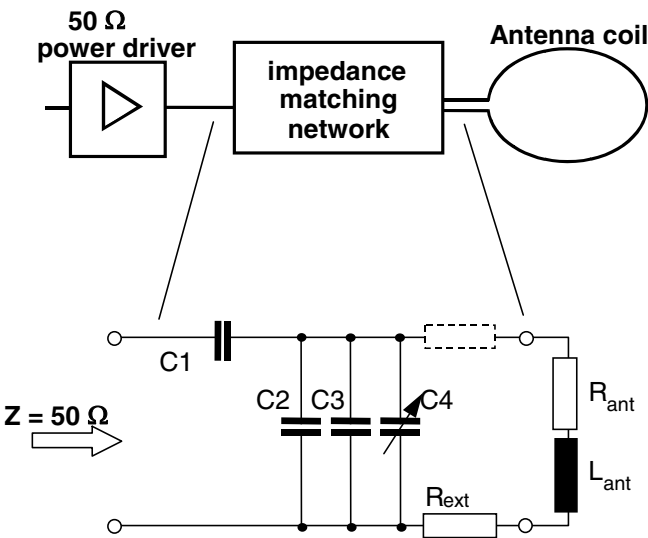
NOTE 1 The tolerance of the matched antenna impedance is $\pm 5 \Omega$ and $\pm 10^\circ$.

NOTE 2 R_{ext} is placed on the ground side of the antenna coil.

NOTE 3 The power and voltage ranges include a safety margin.

NOTE 4 The linear low distortion variable output 50Ω power driver should be capable of emitting Type A and Type B modulations for transmission of REQA and REQB as defined in 7.2.2. The output power should be adjustable to deliver H fields in the range of 1,5 A/m (rms) – 12 A/m (rms). Care should be taken with the duration of fields above the upper operating range of 7,5 A/m (rms).

A.2.1 Impedance matching network for a bit rate of $fc/128$



Component Table:

	Value	Unit	Remarks
C1	47	pF	Voltage range 200 V
C2	180	pF	Voltage range 200 V
C3	22	pF	Voltage range 200 V
C4	2-27	pF	Voltage range 200 V
R_{ext}	0,94	Ω	Power range 10 W

Figure A.5 — Impedance matching network for a bit rate of $fc/128$

- NOTE 1 R_{ext} may be built by connecting five resistors of $4,7\ \Omega\ 2\ W$ in parallel.
- NOTE 2 R_{ext} may still be placed at the position marked with a dashed outline, as shown in Figure A.5.
- NOTE 3 R_{ext} may be $4\ W$ if the maximum field is up to $7,5\ A/m$ (rms).
- NOTE 4 The parasitic capacitance of the antenna is not shown in Figure A.5.

A.2.2 Impedance matching network for bit rates of $fc/64$, $fc/32$ and $fc/16$

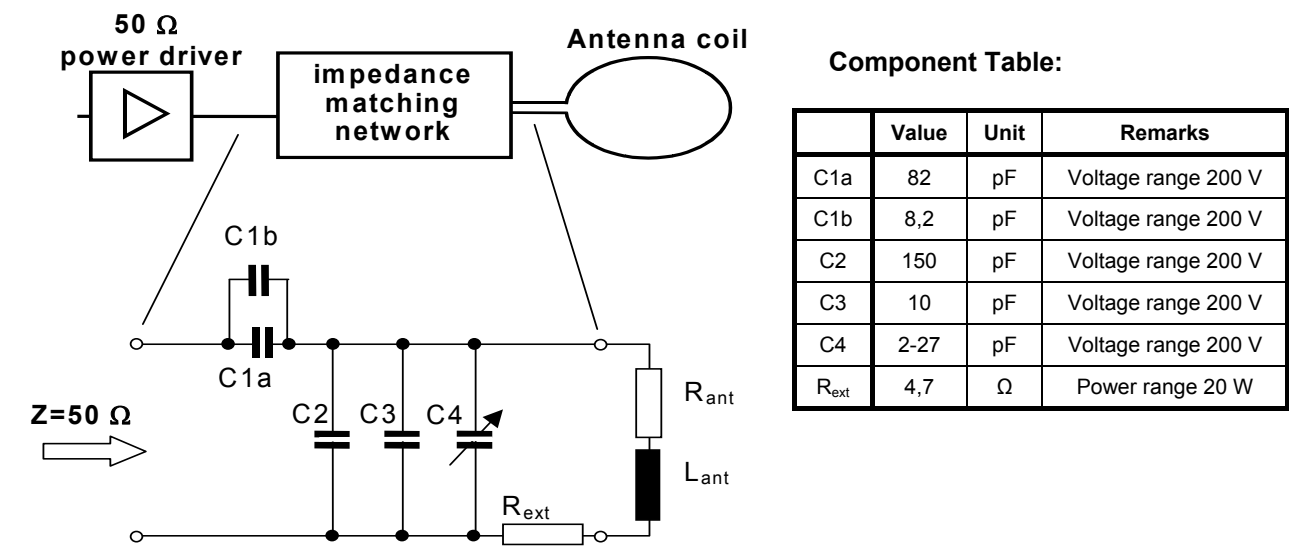


Figure A.6 — Impedance matching network for bit rates of $fc/64$, $fc/32$ and $fc/16$

- NOTE 1 R_{ext} may be built by a parallel circuit of each two resistors of $4,7\ \Omega\ 5\ W$ in series.
- NOTE 2 R_{ext} should be placed on the GND side of the antenna as drawn.
- NOTE 3 The parasitic capacitance of the antenna is not shown in Figure A.6.

Annex B (informative)

Test PCD Antenna tuning

Figures B.1 and B.2 show the two steps of a simple phase tuning procedure to match the impedance of the antenna to that of the driving generator. After the two steps of the tuning procedure the signal generator shall be directly connected to the antenna output for the tests.

Step 1:

A high precision resistor of $50\ \Omega \pm 1\%$ (e.g. $50\ \Omega$ BNC resistor) is inserted in the signal line between the signal generator output and an antenna connector. The two probes of the oscilloscope are connected to both sides of the serial reference resistor. The oscilloscope displays a Lissajous figure when it is set in Y to X presentation. The signal generator is set to:

- Wave form: Sinusoidal;
- Frequency: 13,56 MHz;
- Amplitude: 2 V (rms) - 5 V (rms).

The output is terminated with a second high precision resistor of $50\ \Omega \pm 1\%$ (e.g. $50\ \Omega$ BNC terminating resistor). The probe, which is in parallel to the output connector has a small parasitic capacitance C_{probe} . A calibration capacitance C_{cal} in parallel to the reference resistor compensates this probe capacitor if $C_{\text{cal}} = C_{\text{probe}}$. The probe capacitor is compensated when the Lissajous figure is completely closed.

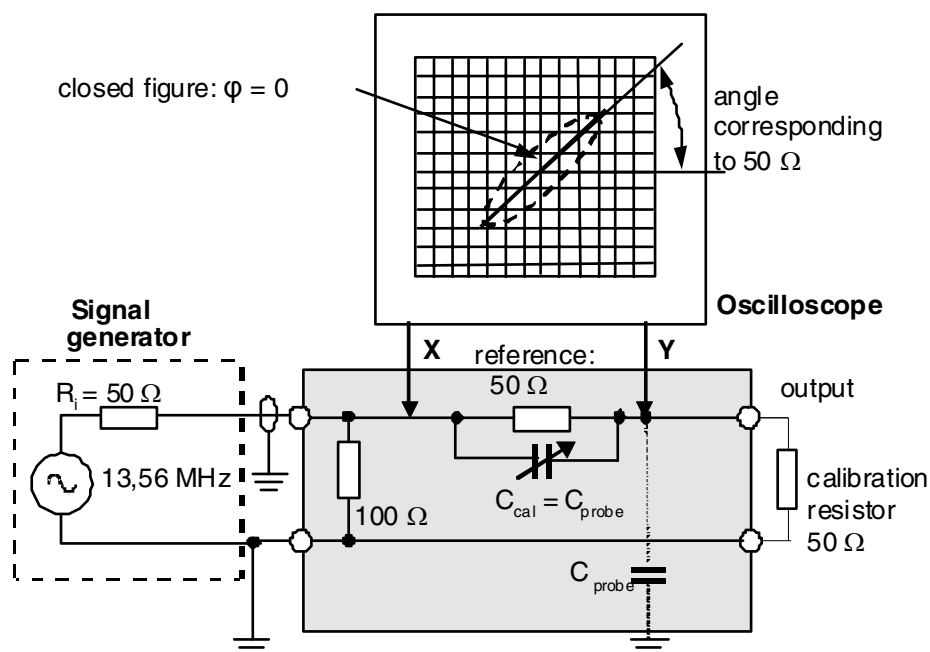


Figure B.1 — Calibration set-up (Step 1)

NOTE The ground cable has to be run close to the probe to avoid induced voltages caused by the magnetic field.

Step 2:

Using the same values as set for step 1, in the second step the matching circuitry is connected to the antenna output. The capacitor C4 on the antenna board is used to tune the phase to zero.

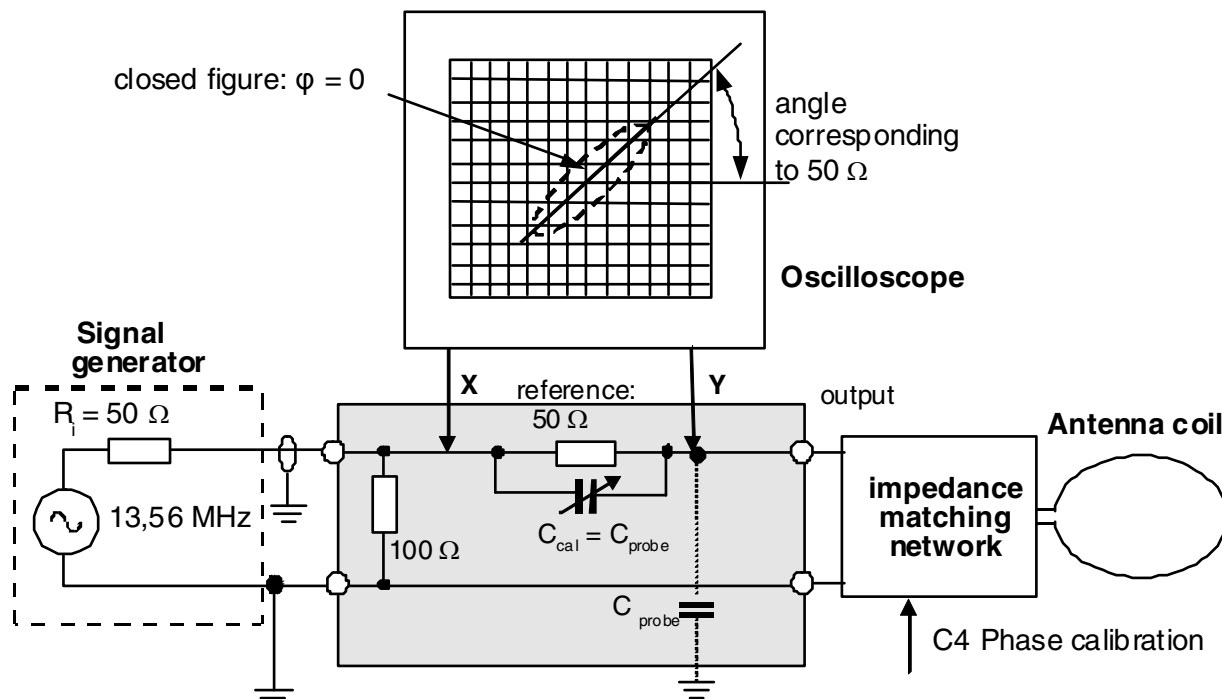


Figure B.2 — Calibration set-up (Step 2)

Annex C (normative)

Sense coil

C.1 Sense coil layout

Figure C.1 illustrates sense coil layout.

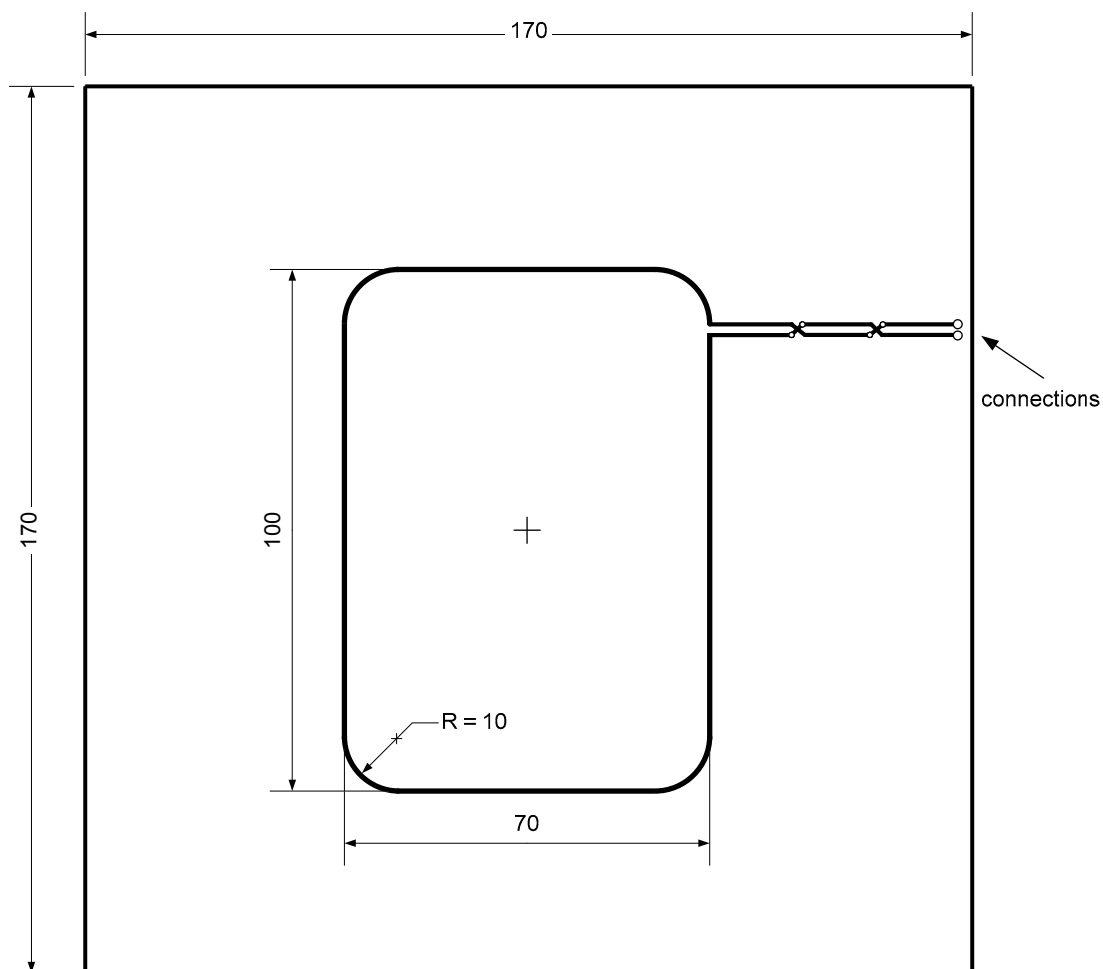


Figure C.1 — Layout for sense coils a and b

Dimensions in millimeters (drawings are not to scale).

The sense coil track width is 0,5 mm with relative tolerance $\pm 20\%$ (except for through-plated holes). Size of the coils refers to the outer dimensions.

Printed circuit board (PCB): FR4 material, thickness 1,6 mm, double sided with 35 μm copper.

NOTE Such printed circuit boards are available from various commercial sources.

C.2 Sense coil assembly

Figure C.2 illustrates sense coil assembly.

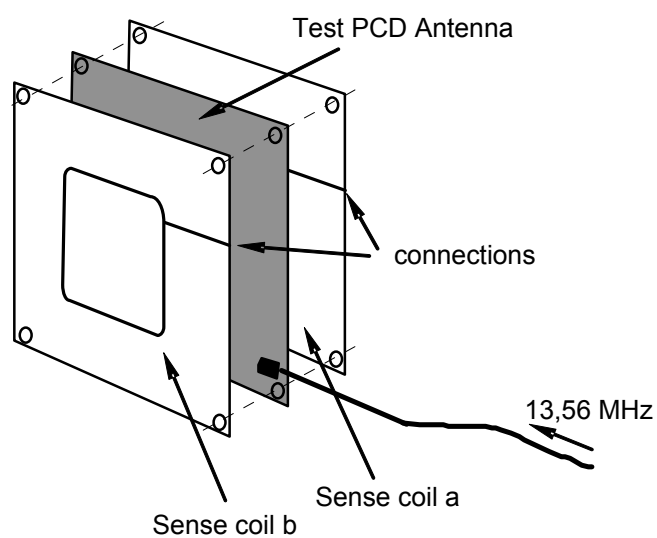


Figure C.2 — Sense coil assembly

Annex D (normative)

Reference PICC antenna layout

Figure D.1 illustrates Reference PICC antenna layout.

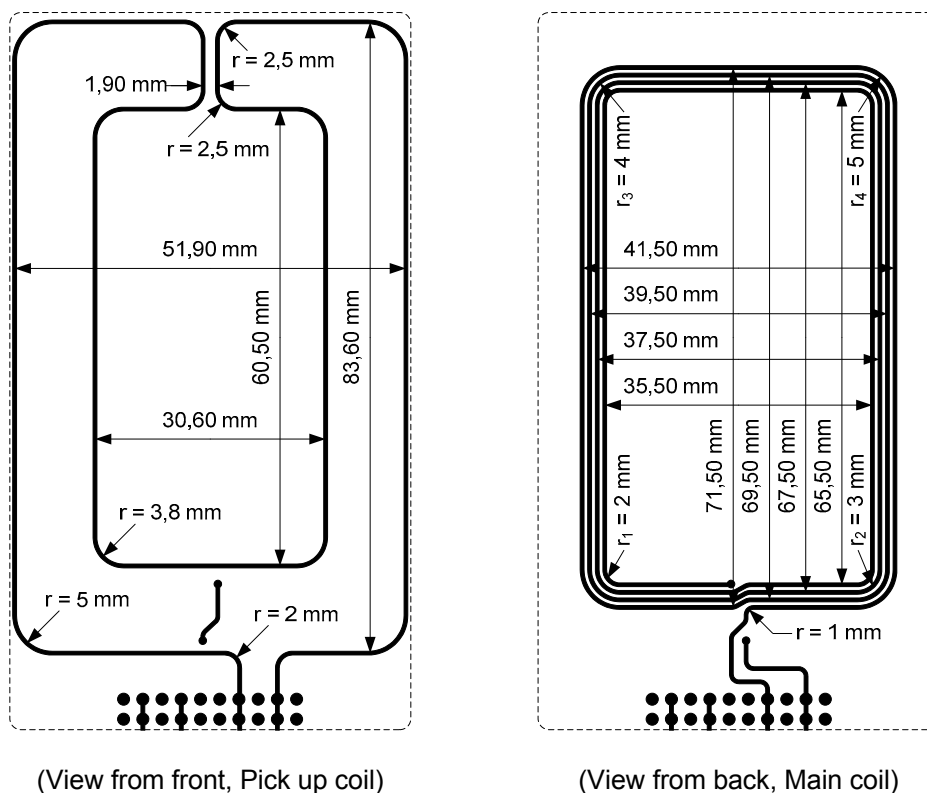


Figure D.1 — Antenna layout

Dimensions to track center (drawings are not to scale).

The Pick up coil and the Main coil shall be concentric.

The two coils track width and spacing shall be 0,5 mm with a relative tolerance of $\pm 20\%$.

Printed circuit board (PCB): FR4 material, thickness 0,76 mm with a relative tolerance of $\pm 10\%$, double sided with 35 μm copper.

NOTE 1 At 13,56 MHz the inductance of the Main coil L1 is 2,3 $\mu\text{H} \pm 10\%$ and the resistance is 1,8 $\Omega \pm 10\%$.

NOTE 2 At 13,56 MHz the inductance of the Pick up coil L2 is 375 nH $\pm 10\%$ and the approximate resistance is 0,65 $\Omega \pm 10\%$.

NOTE 3 Such printed circuit boards are available from various commercial sources.

Annex E (normative)

Modulation index and waveform analysis tool

E.1 Overview

The working principle of the modulation index and waveform analysis tool is illustrated in Figure E.1.

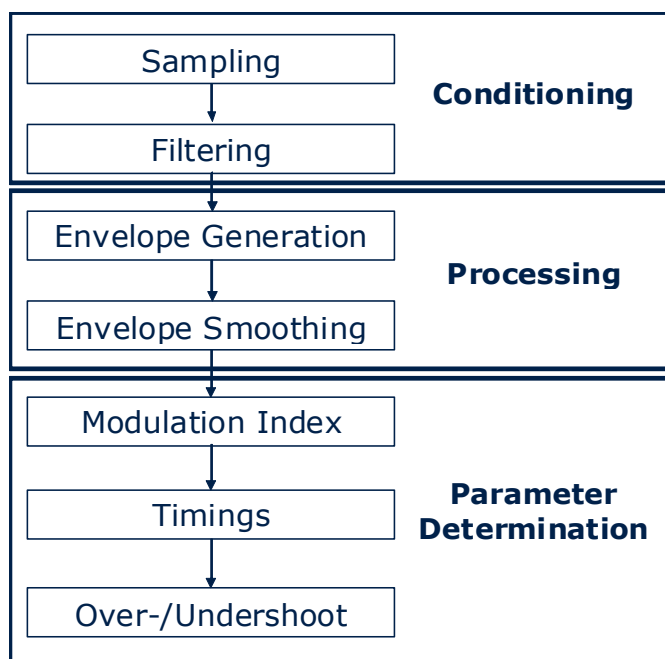


Figure E.1 — Modulation index and waveform analysis tool block diagram

Each block is described in following clauses.

E.2 Sampling

The oscilloscope used for signal capturing shall fulfill the requirements defined in 5.1.1. The time and voltage data of one modulation pulse (see Figure E.2) shall be transferred to a suitable computer.

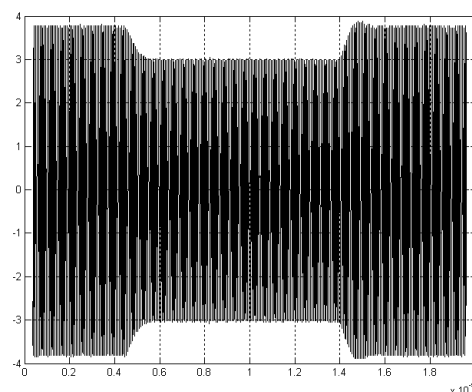


Figure E.2 — Modulation pulse

E.3 Filtering

A 4th order, Butterworth type band pass filter with center frequency of 13,56 MHz and 10 MHz 3-dB bandwidth shall be used for filtering the DC and higher harmonic components. The filter characteristic is illustrated in Figure E.3.

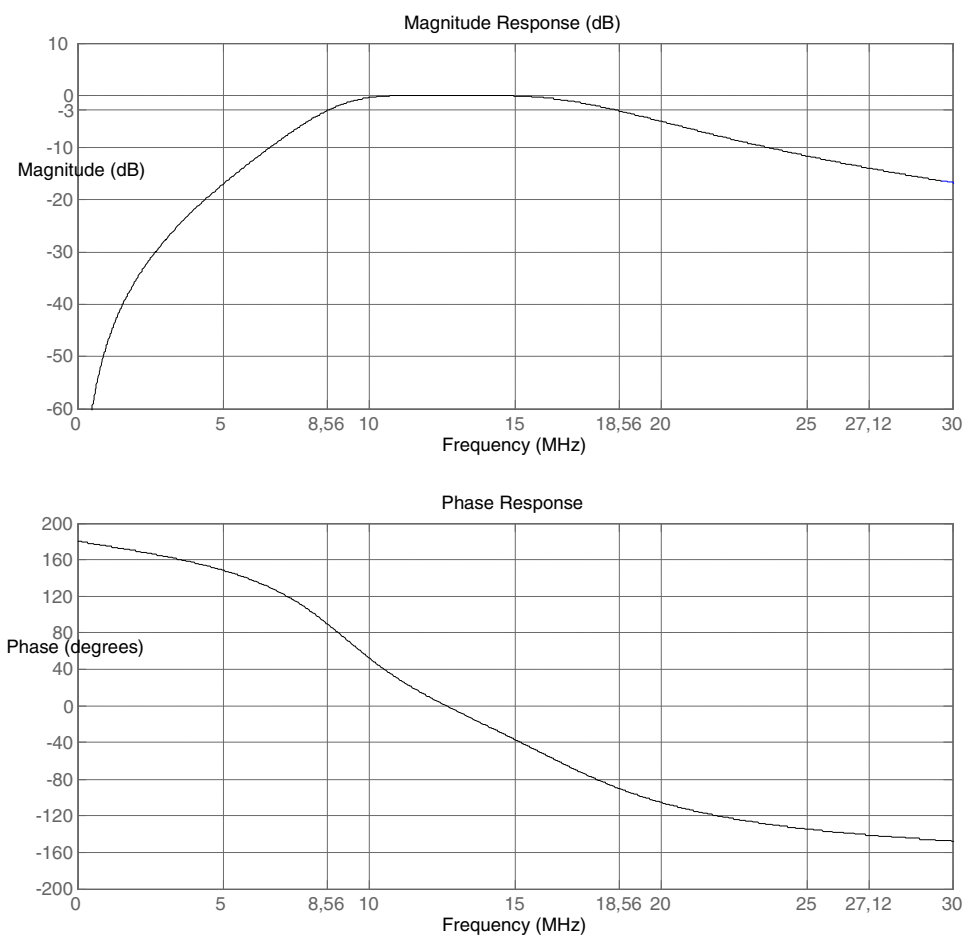


Figure E.3 — Filter characteristics

E.4 Envelope generation

The filtered signal shall be Hilbert transformed and the magnitude of this complex transform represents the signal envelope.

E.5 Envelope smoothing

The signal envelope shall be smoothed with a moving average filter and the filter period shall be one carrier period. The smoothed envelope signal is illustrated Figure E.4.

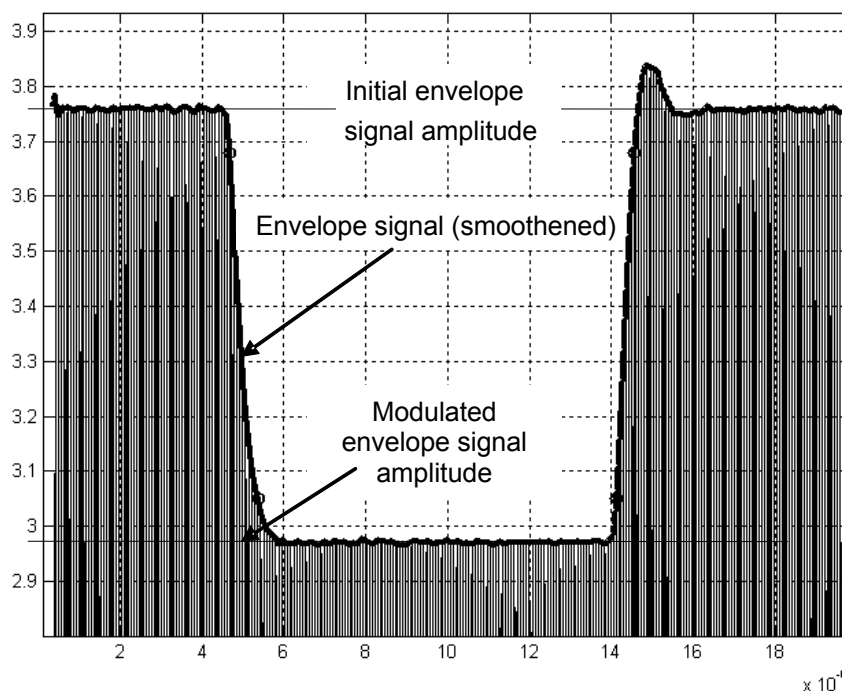


Figure E.4 — Envelope smoothing

E.6 Modulation index determination

The initial and modulated envelope signal amplitudes shall be determined by calculating the histogram of the smoothed envelope signal. The most frequent values correspond to the initial and modulated envelope signal amplitude. For Type A modulation signals only the initial envelope signal amplitude shall be determined using the histogram approach.

E.7 Timing determination

The rise and fall times should be determined according to the definitions in ISO/IEC 14443-2:2010.

E.8 Overshoot and undershoot determination

The already smoothened envelope signal shall be further smoothened by a moving average filter over 3 carrier periods before determining the overshoot and undershoot values according to the definitions in ISO/IEC 14443-2:2010.

E.9 Program of the modulation index and waveform analysis tool (informative)

The following program written in C language gives an example for the implementation of the modulation index and waveform analysis tool.

The C implementation consists of 6 different files which should be placed in the same folder.

E.9.1 structures.h

```

/*****
/*structures.h
/*This code contains the structures to save important results
/*****
#ifndef STRUCTURES_H
#define STRUCTURES_H

typedef struct esl
{
    double volt;
    double time;
    struct esl *sig;
}ESL;

typedef struct times
{
    double tf; // Type B
    double tr; // Type B
    double b; // Type B
    double trstartind; // Type B
    double trendind; // Type B
    double tfstartind; // Type B
    double tfendind; // Type B

    double t1; // Type A (all bit rates)
    double t1startind; // Type A (all bit rates)
    double t1start; // Type A (all bit rates)
    double t1endind; // Type A (all bit rates)

    double t2; // Type A
    double t2startind; // Type A
    double t2start; // Type A
    double t3; // Type A
    double t3end; // Type A
    double t3endind; // Type A
    double t4; // Type A
    double t4endind; // Type A

    double t5; // Type A (higher bit rates)
    double t5startind; // Type A (higher bit rates)
    double t6; // Type A (higher bit rates)
    double t6end; // Type A (higher bit rates)
    double t6endind; // Type A (higher bit rates)
    double a; // Type A (higher bit rates)
    double tploone; //Type A (higher bit rates)
}TIMES;

typedef struct shootreader
{
    double shootind;
    double shootind_b;
    double hf_reader;
    double hr_reader;
    double above;
    double above_b;
}SHOOTREADER;

#endif

```

E.9.2 fftm.h

```

/*****
/*fftm.h
/*This is the header file for fftm.c
/*****

#ifndef FFTM_H
#define FFTM_H

#define RE(z) ((z).r)
#define IM(z) ((z).i)

typedef float real;
typedef double doublereal;
typedef struct { real r, i; } complex;
typedef struct { doublereal r, i; } doublecomplex;

int zffts (int debug, doublecomplex *X, int M);
int ziffts (int debug, doublecomplex *X, int M);
void zfftrmc(doublecomplex *X, int M, int P, float D);
void rmpo (int *rv, int *rvp );

#endif

```

E.9.3 fftm.c

```

/*****
/*fftm.c
/*This code contains the necessary function for Fourier and inverse Fourier
/* transformation
/*****

#include <stdio.h>
#include <math.h>
#include <malloc.h>
#include "fftm.h"

#ifndef M_PI
#define M_PI 3.1415926535897932384626433832795
#endif

float *WR;
float *WI;

doublelereal *DWR;
doublelereal *DWI;

void rmpo( int *rv, int *rvp )
{
    int value_h;
    int n;

    n = 1;
    *rvp = -1;
    value_h = 1;

    while ( value_h > 0 )
    {
        value_h = *rv - n;
        (*rvp)++;
        n += n;
    }
}

void zfftrmc( doublecomplex *X, int M, int P, float D )
{
    int MV2,MM1,J,I,K,L,LE,LE1,IP,IQ,IND,IND1,R;
    int I1,J1;
    float A,B;
    float WCOS,WSIN;
    float VR,VI;
    float ARG;

    static int IPOTC;
    static float DALT;

    DWR = (doublelereal *)calloc(M,sizeof(doublelereal));
    DWI = (doublelereal *)calloc(M,sizeof(doublelereal));

    /* if (IPOTC == P & D == DALT) goto warmstart; */

    IPOTC = P;
    DALT = (float)D;
    LE = 1;

```

```

IND = 0;

for (L=1; L<=P; L++)
{
    LE1 = LE;
    LE = LE*2;
    DWR[IND] = 1.0;
    DWI[IND] = 0.0;
    ARG = (float)M_PI/(float)LE1;
    WCOS = (float)cos(ARG);
    WSIN = (float)(D*sin(ARG));

    for (R=1; R<=LE1; R++)
    {
        IND1 = IND+1;
        A = (float)DWR[IND];
        B = (float)DWI[IND];
        DWR[IND1] = A*WCOS - B*WSIN;
        DWI[IND1] = B*WCOS + A*WSIN;
        ++IND;
    }
}

/* warmstart: */

MV2=M/2;
MM1=M-1;
J=1;

for (I=1; I<=MM1; I++)
{
    if (I >= J)
        goto P1;

    J1 = J-1;
    I1 = I-1;

    VR = (float)RE(X[J1]);
    VI = (float)IM(X[J1]);

    RE(X[J1]) = RE(X[I1]);
    IM(X[J1]) = IM(X[I1]);

    RE(X[I1]) = VR;
    IM(X[I1]) = VI;

P1: K = MV2;
P2: if (K >= J) goto P3;
    J = J-K;
    K = K/2;
    goto P2;
P3: J = J+K;
}
IND = 0;
LE = 1;

for (L=1; L<=P; L++)
{
    LE1 = LE;
    LE = LE*2;

```

```

    for (R=0; R<LE1; R++)
    {
        WCOS = (float)DWR[IND];
        WSIN = (float)DWI[IND];
        IND = IND+1;
        for (IQ=R; IQ<M; IQ+=LE)
        {
            IP = IQ+LE1;

            A = (float)RE(X[IP]);
            B = (float)IM(X[IP]);

            VR = A*WCOS - B*WSIN;
            VI = B*WCOS + A*WSIN;

            RE(X[IP]) = RE(X[IQ]) - VR;
            IM(X[IP]) = IM(X[IQ]) - VI;

            RE(X[IQ]) = RE(X[IQ]) + VR;
            IM(X[IQ]) = IM(X[IQ]) + VI;
        }
    }

    free(DWR);
    free(DWI);
}

/*=====*/
/*__1-D FFT with respect to a spatial coordinate_____*/
/*=====*/
int zffts( int debug, doublecomplex *X, int M )
{
    int P;
    float D;

    D = -1.0;

    rmpo( &M, &P);

    if ( debug )
    {
        printf("P = %d\n",P);
        printf("FFT ...\\n");
    }

    zfftrmc( X, M, P, D); /* fftrm.c */

    return 0;
}

/*=====*/
/*__1-D Inverse FFT with respect to a spatial coordinate_____*/
/*=====*/
int ziffts( int debug, doublecomplex *X, int M )
{
    int i;
    int P;
    float D;

```

```

D = 1.0;

rmpo( &M, &P);

if ( debug )
{
    printf("P = %d\n",P);
    printf("IFFT ... \n");
}

zfftrmc( X, M, P, D); /* fftrm.c */

/*__Multiply with 1/M__*/

for (i=0; i<M; i++)
{
    RE(X[i]) /= (double)M;
    IM(X[i]) /= (double)M;
}

return 0;
}/*End of fftrm.c*/

```

E.9.4 hilbert.h

```

/*****
*/hilbert.h
/*This code contains the necessary functions for extracting envelope
/*****

#ifndef HILBERT_H_
#define HILBERT_H_

/*This function reads the sampled data recorded in the file*/
int ReadData(void);

/*This function performs the Fourier transform*/
void Fft(void);

/*This function performs the necessary phase shift*/
void PhaseShifting(void);

/*This function performs the inverse Fourier transform*/
void Ifft(void);

/*Envelope reconstruction is done by this function*/
int EnvelopeReconstruction(void);

/*Hilbert main function*/
void hilbert(char *fnamep);

#endif /* HILBERT_H_ */

```