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Edition 1.0 2010-10

INTERNATIONAL STANDARD

Information technology –
Small computer system interface (SCSI)
Part 121: Passive interconnect performance (PIP)



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INFORMATION TECHNOLOGY – SMALL COMPUTER SYSTEM INTERFACE (SCSI)–

Part 121: Passive interconnect performance (PIP)

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This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

IMPORTANT – The "colour inside" logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its content. Users should therefore print this publication using a colour printer.

Introduction

The Parallel Interface Performance standard defines requirements for measuring the electrical performance of bulk cable and interconnect assemblies for use in SPI-x applications and specification of performance limits.

The Parallel Interface Performance standard is divided into the following clauses:

Clause 1 is the scope;
Clause 2 enumerates the normative references;
Clause 3 describes the definitions, symbols, conventions and abbreviations;
Clause 4 provides a general overview of the concepts;
Clause 5 contains a summary of bulk cable requirements;
Clause 6 contains sample preparation, fixtures and setups for bulk cable;
Clause 7 contains bulk cable test procedures;
Clause 8 contains a summary of interconnect assembly requirements;
Clause 9 contains sample preparation, fixtures and setups for interconnect assemblies;
Clause 10 contains interconnect test requirements;

Annex A, Single ended bulk cable requirements, forms an integral part of this standard.

The following informative annexes are provided:

- Annex B, Periodic structure effects;
- Annex C, Requirements for SCSI signal driver board (SSDB);
- Annex D, Mirage effects in multi-drop subassembly TDR impedance measurement.

1 Scope

In the past only the performance requirements for uniform bulk cable (called "media" in earlier standards) have been specified in SCSI standards. Since bulk cable provides only part of the electrical path in a SCSI bus segment, the performance requirements of the interconnect comprising the path is incomplete if only bulk cable is considered. This document expands the coverage to the complete assembled interconnect including connectors, uniform bulk cable, and non-uniform bulk cable. A syntax and framework is described for all types of passive interconnect. The methodology for performing the electrical measurements required to determine compliance with the performance requirements for bulk cable of several types, various assembled interconnects and printed circuit board designs is included.

Details of the measurement methodology are specified to minimize the difference in measured results from different electrical testing laboratories. Details include calibration, fixturing and sample preparation, equipment, measurement procedure and data output format.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 14776-112, *Information technology – Small computer system interface (SCSI) – Part 112: Parallel interface-2 (SPI-2)*

ISO/IEC 14776-113, *Information technology – Small computer system interface (SCSI) – Part 113: Parallel interface-3 (SPI-3)*

ISO/IEC 14776-115, *Information technology – Small computer system interface (SCSI) – Part 115: Parallel interface-5 (SPI-5) [T10/1525D]*

INCITS 362-2002, *Information technology – Small computer system interface (SCSI) – Parallel Interface-4 (SPI-4)*

3 Terms, definitions and abbreviations

3.1 Terms and definitions

3.1.1 accuracy:

quality of freedom from mistake or error;
the degree of correctness with which a measured value agrees with the true value

NOTE Not to be confused with precision, see 3.1.74.

3.1.2 admittance:

an n -terminal network, the complex current flowing to the i -th terminal divided by the complex voltage applied between the j -th terminal with respect to the reference point when all other terminals have arbitrary terminations; the inverse of impedance

3.1.3 american wire gauge:

formerly the Brown & Sharpe Gage, the standard gauge for copper, aluminum and other conductors except steel

3.1.4 assembly:

subordinate element of a system that is comprised of two or more components

3.1.5 asserted:

having a signal value associated with a logic 1

3.1.6 attenuation:

- a) general term used to denote a decrease in signal magnitude from one point to another; attenuation may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio
- b) reciprocal of gain

3.1.7 backplane:

printed circuit board that contains the interconnect traces and connectors, into which boards or plug-in units are inserted

3.1.8 balanced:

a) state of impedance on a two-wire circuit when the impedance-to-ground of one wire is equal from the impedance-to-ground of the other wire

b) a circuit, in which two branches are electrically alike and symmetrical with respect to a common reference point, usually ground

3.1.9 buffer:

in the sense of the IBIS standard, an isolating circuit used to prevent a driven circuit from influencing a driving circuit; a transceiver, see 3.1.98.

3.1.10 bulk cable:

cable that is not pure connector terminated

3.1.11 bus:

signal line or a set of lines used by an interface system to connect a number of devices and transfer data

3.1.12 Cable assembly:

cable that is connector terminated;

NOTE Generally, a cable that has been terminated by a manufacturer and is ready for installation.

3.1.13 Calibration:

criteria to validate the measurement

3.1.14 capacitive coupling:

type of coupling in which the mechanism is capacitance between the interference source and the signal system; that is, the interference is induced in the signal system by an electric field produced by the interfering source

3.1.15 circuit:

interconnection of electrical components

3.1.16 circuit element:

basic constituent part of a circuit, exclusive of interconnections; a component

3.1.17 common-mode:

instantaneous algebraic average of two signals applied to a balanced circuit, both signals refer to a common reference

3.1.18 common-mode noise:

noise voltage that appears equally and in phase from each signal conductor to ground

3.1.19 component: I

items from which a system, assembly or sub-assembly is assembled;
for example, resistors, capacitors, inductors, semiconductors, etc.; a circuit element

3.1.20 complementary metal oxide semiconductor:

semiconductor technology in which circuits are composed of paired NMOS and PMOS devices

3.1.21 complex dielectric constant:

the complex permittivity of a physical medium in relation to the permittivity of free space

3.1.22 complex permittivity:

for isotropic media, the ratio of the complex amplitude of the electric displacement density to the complex amplitude of the electric field strength

3.1.23 computer-aided engineering:

application of computers to the engineering process

NOTE The term applies to any computer system or program that manipulates data for the purpose or which assists engineering, design, procurement, maintenance, etc.

3.1.24 concatenated:

two or more interconnect assemblies (similar or dissimilar) connected together as part of a single SCSI bus segment

NOTE Examples include round shielded cable connected to a backplane with no expander on the backplane and flat multidrop interconnect assembly connected to a round point-to-point interconnect assembly.

3.1.25 conductivity:

(σ) macroscopic material property that relates the conduction current density (J) to the electric field (E) in the medium

3.1.26 connector terminated:

section of cable with connectors attached

3.1.27 contact:

electrically conductive portion of a connector associated with a single conductor in a cable

3.1.28 de-asserted:

having a current value equal to a logic 0

3.1.29 device:

entity that contains the SCSI driver and receiver

3.1.30 dielectric constant: 1

- a) the physical property which determines the electrostatic energy stored per unit volume for unit potential gradient; this value is usually given relative to vacuum
- b) the real part of the complex dielectric constant

3.1.31 dielectric loss:

contribution to the attenuation constant of a propagating mode on a transmission line that represents losses associated with the dielectric properties of the insulation materials involved

3.1.32 differential-mode:

instantaneous algebraic difference of two signals applied to a balanced circuit, both signals refer to a common reference

3.1.33 differential-mode noise:

noise voltage that appears differentially between two signal wires and acts on the signal sensing circuit in the same manner as the desired signal

3.1.34 differential SCSI:

SCSI signal configuration that uses balanced transmission lines

3.1.35 discontinuity:

- a) abrupt non uniformity in a uniform transmission line that causes reflected waves
- b) abrupt change in the cross section of the planar transmission line

NOTE Abrupt refers usually to a change in dimensions or material over a length that is short compared to a wavelength. Short is generally recognized as 0,1 wavelength or smaller.

3.1.36 driver:

- a) electronic circuit that supplies input to another electronic circuit
- b) electrical circuit whose purpose is to signal a binary state for transmitting information

NOTE Driver is also referred to as a generator in international standards.

3.1.37 electromagnetic compatibility:

a system's ability to perform its specified functions in the presence of electrical noise generated either internally or externally by other systems

3.1.38 electromagnetic interference:

electromagnetic energy from sources internal or external to electrical or electronic equipment that adversely affect equipment by creating undesirable responses

3.1.39 electrostatic discharge:

sudden transfer of charge between bodies of differing electrostatic potential

3.1.40 element:

component, subcomponent, assembly, subassembly or part of a physical architecture or system

3.1.41 expander:

device that connects SCSI device segments together to form a single SCSI domain (see SDV)

3.1.42 false:

one of two binary states the other of which is true; false is usually represented by 0

3.1.43 gain:

- a) general term used to denote a increase in signal magnitude from one point to another; gain may be expressed as a scalar ratio of the input magnitude to the output magnitude or in decibels as 20 times the log of that ratio
- b) reciprocal of attenuation

3.1.44 group delay:

derivative of radian phase with respect to radian frequency $\partial\phi/\partial\omega$

Group delay is equal to the phase delay for an ideal non dispersive device or medium, but may differ greatly in an actual device or medium where there is ripple in the phase versus frequency characteristic. In network analyzers, $\partial\omega$ is replaced by $\Delta\omega$, and shall be sufficiently large to permit adequate measurement resolution. If $\Delta\omega$ is too large, the limit in the defining equation will not be reached, and the measured group delay is dependent upon $\Delta\omega$. Therefore the value of $\Delta\omega$ used in a measurement shall be specified.

3.1.45 group delay time:

the rate of change, with angular frequency, of the total phase shift through a network

Group delay time is the time interval required for the crest of a group of interfering waves to travel through a 2-port network, where the component wave trains have slightly different individual frequencies.

3.1.46 group velocity:

velocity of propagation of a signal envelope, provided that the envelope moves without a significant change of shape

The magnitude of the group velocity is equal to the reciprocal of the rate of change of the phase constant with angular frequency.

3.1.47 hardware description language:

computer language with special constructs and verification protocols, used to develop, analyze, validate and document a hardware design or computer architecture

3.1.48 inductive coupling:

type of coupling in which the mechanism is inductance between the interference source and the signal system; that is, the interference is induced in the signal system by a magnetic field produced by the interfering source

3.1.49 insulation displacement contact:

type of contact where the connection to the cable is made by mechanically piercing the cable insulation as opposed to a connection in which the cable insulation is removed to provide access to the conductor

3.1.50 interconnect component:

interconnect components include cables, connectors, printed circuit boards and transition regions; all interconnect components are passive

3.1.51 isotropic:

pertaining to a material whose electric or magnetic properties, or both, are directionally independent

3.1.52 logical unit:

externally addressable entity within a target and that processes SCSI commands

3.1.53 least significant:

within a group of items that, taken as a whole, represents a numerical value, the item within the group with the smallest numerical weighting

3.1.54 loss tangent:

ratio of the imaginary part of the complex dielectric constant of a material to its real part

3.1.55 measurement:

process of obtaining data

3.1.56 microstrip:

class of planar transmission lines consisting of one or more thin conducting strips of finite width parallel to a single extended conducting ground plane.

The strips are fixed to an insulating substrate attached to the ground plane. The semi-infinite space above the strips is filled with a medium of relative permittivity and permeability equal to or less than the substrate.

3.1.57 mode:

synonymous with transmission mode, see 3.1.102

3.1.58 model:

a) approximation, representation or idealization of selected aspects of the structure, behavior, operation or other characteristics of a real-world process, concept or system; models may have other models as components

b) to serve as a model in definition a)

c) to develop or use a model as in definition a)

3.1.59 most significant:

within a group of items that, taken as a whole, represents a numerical value, the item within the group with the greatest numerical weighting

3.1.60 multilane:

model representation of a multi-conductor component that includes the capacitive and inductive coupling among the conductors

3.1.61 netlist:

listing of the nets of a circuit, providing, usually in text format, a description of the connections among the components of the circuit

3.1.62 network:

any set of devices or subsystems connected by links joining, directly or indirectly, a set of terminal nodes

3.1.63 network function:

any impedance, admittance function or any other function of p that can be expressed in terms of or derived from the determinant of a network and its cofactors; this also includes voltage ratios, current ratios and numerous other quantities

3.1.64 network matrix:

anyone of several matrices that relate the equivalent voltage, current, incident waves and reflected waves of an n -port network

3.1.65 network parameters:

elements of a network matrix

3.1.66 one:

true logic state

3.1.67 phase angle:

measure of the progression of a periodic wave in time or space from a chosen instant or position

3.1.68 phase delay:

relation of total radian phase shift to the specified radian frequency; phase delay is nominally constant over the frequency band of operation for nondestructive delay components

3.1.69 phase shift:

a) the absolute magnitude of the difference between two phase angles

b) the displacement in time of one periodic-waveform relative to other waveforms

3.1.70 phase velocity:

velocity of an equiphase surface normal to the direction of propagation of a traveling wave at a single frequency and for a given mode

3.1.71 planar transmission line:

a transmission line composed of one or more parallel plates, slabs or sheets of conduction or insulating material, including free space, and in which one or more layers are composed of material of differing electromagnetic properties, arranged in strips of finite cross section and aligned with the axis of propagation to form the guiding structures

3.1.72 pole:

value of s that makes a transfer function in the complex variable infinity, or its corresponding point in the s plane

3.1.73 port:

place of access to a network where the network variables may be observed or measured

NOTE In this document the places of access include connectors on interconnect assemblies, prepared bulk cable ends and pads on unpopulated backplanes.

3.1.74 precision:

- a) degree of exactness or discrimination with which a quantity is stated; for example 3 decimal places versus 5 decimal places
- b) the repeatability of measurement data expressed in terms of standard deviation

3.1.75 primary bus:

collection of signals that provides the system with the basic mechanism for exchanging data

3.1.76 radio frequency:

frequency in the range of 10 kHz to 100 000 MHz.

3.1.77 radio frequency interference:

degradation of a wanted signal by an electromagnetic disturbance having components in the RF range

3.1.78 receiver:

- a) an electronic circuit that recognizes input from another electronic circuit
- b) an electrical circuit whose purpose is to recognize the binary state of transmitted information

3.1.79 resistivity:

the reciprocal of volume conductivity measured in siemens per centimeter

3.1.80 s parameter:

one of the coefficients of the scattering matrix

3.1.81 scattering matrix:

square array used to relate incident and reflected waves for an n -port network

3.1.82 SCSI bus segment:

all the conductors and connectors required to attain signal line continuity between every driver, receiver, and terminator for each signal

3.1.83 SCSI component:

a component part of a complete SCSI system

NOTE SCSI components include but are not limited to: cables, cable assemblies, devices, terminators, boards, backplanes, controllers and chips.

3.1.84 SCSI device:

device that contains one or more SCSI ports that are connected to a service delivery subsystem and supports a SCSI application protocol, see SAM-2

3.1.85 SCSI port:

single attachment to a SCSI bus segment from a SCSI device

3.1.86 signal assertion:

act of driving a signal to the true state

3.1.87 signal negation:

act of performing a signal release or of driving a signal to the false state

3.1.88 single line:

a model representation of a multi-conductor component that does not include the capacitive and inductive coupling among the conductors

3.1.89 single-ended SCSI:

SCSI signal configuration that uses unbalanced transmission lines

3.1.90 skin depth:

of a conducting material, at a given frequency, the depth at which the surface current density is reduced to $1/e$ of its value at the surface

3.1.91 skin effect:

tendency of alternating current to concentrate in the areas of lowest impedance

3.1.92 small computer system interface:

data-transfer interface used to connect multiple peripheral devices such as disk drives, tapes or printers to computer systems while taking up only one slot in the computer

NOTE Previously this was known as Shugart Associates Systems Interface.

3.1.93 simulation program with integrated circuit emphasis:

application-oriented programming language used widely to design electrical circuits

3.1.94 stripline:

class of planar transmission line characterized by one or more conducting strips of finite width parallel to and approximately midway between two extended conducting ground planes; the space between the planes is filled with a homogeneous insulation medium

3.1.95 stub:

section of transmission line joined to the main transmission line and containing a non dissipative termination

3.1.96 system:

in a hierarchical approach, a collection of interacting, interrelated or interdependent elements forming a collective functioning entity

3.1.97 test:

measurement to which a pass-fail criteria is applied

3.1.98 transceiver:

device that both transmits and receives data

3.1.99 transition region:

the region of the cable or PCB, between the connector attachment point and the point in the bulk cable or PCB that is physically undisturbed by the connector attachment methodology

3.1.100 transmission line:

structure designed to guide the propagation of electromagnetic energy in a well-defined direction

3.1.101 transmission medium:

material on which information signals may be carried; for example, twisted-wire pairs, planar transmission lines, coaxial cable, etc.

3.1.102 transmission mode:

form of propagation along a transmission line characterized by the presence of one of the elemental types of transverse electric, transverse magnetic or transverse electromagnetic waves; more than one mode may be concurrent along a transmission line

3.1.103 transmittance:

response function for which the variables are measured at different ports

3.1.104 true:

one of two binary states, usually represented by 1, the other of which is false

3.1.105 two-port parameters:

network parameters for a two-port device

3.1.106 unbalanced:

- a) state of impedance on a two-wire circuit where the impedance-to-ground of one wire is different from the impedance-to-ground of the other wire
- b) unbalanced frequently signifies a circuit where one side is grounded

3.1.107 uniform transmission line:

a transmission line that has substantially identical electrical properties throughout its length

3.1.108 validation:

the process of evaluating a system or component to ensure compliance with the functional, performance and interface requirements

3.1.109 vendor-specific:

term used to describe parameters that may vary between vendors supplying similar components

3.1.110 verification:

confirmation by examination (testing) with evidence that specified requirements have been met

3.1.111 via:

electrical connection between the layers of a printed circuit board

3.1.112 zero:

- a) a false logic state
- b) any value of p , real or complex, for which the network function is zero
- c) value of s that makes a transfer function in the complex variable zero, or its corresponding point in the s plane

3.2 Acronyms

AWG	american wire gauge
CMOS	complementary metal-oxide semiconductor
DCP	driver calibration pattern
DUT	device under test
EMC	electromagnetic compatibility
EMI	electromagnetic interference
ESD	electrostatic discharge
HBA	host bus adapter
HDD	hard disk drive
HVD	high voltage differential
IDC	insulation displacement contact
ISI	inter-symbol interference
LSB	least significant bit
LVD	low voltage differential
MSB	most significant bit
NEXT	near end crosstalk
PCB	printed circuit board
RF	radio frequency
RFI	radio frequency interference
RLGC	resistance, inductance, admittance, capacitance
SCSI	small computer system interface
SDV	
SE	single-ended

SPI	SCSI parallel interface
SPI-x	all versions of SPI
SPICE	simulation program with integrated circuit emphasis
SSDB	SCSI signal driver board
STD	signal transition duration
TDR	time domain reflectometer
TDT	time domain through
TDW	time domain waveform
TDWP	time domain waveform pattern
URL	uniform resource locator

3.3 Symbols and abbreviations

$\pm$	plus or minus
$\approx$	approximately
x	multiply
+	add
-	subtract
< or LT	less than
$\leq$ or LE	less than or equal
= or EQ	equal
> or GT	greater than
$\geq$ or GE	greater than or equal
$\neq$ or NE	not equal
A	ampere
c	velocity of light in a vacuum
C	coulomb or capacitance
dB	decibel
E	electric field
F	farad
G	conductance
g	gram
H	henry
Hz	hertz
j	square root of minus one
J	joule
J	current density
L	inductance
m	meter
N	newton
Np	neper
R	resistance
s	second
s	s parameter
T	tesla
t	time
V	volt
W	watt
Wb	weber
∂	partial differential
ϕ	radial phase
ρ	either conductance or admittance
Ω	ohm
ω	radians per second
T	10^{12}
G	10^9

M	10^6
k	10^3
c	10^{-2}
m	10^{-3}
μ	10^{-6}
n	10^{-9}
p	10^{-12}
f	10^{-15}

3.4 Keywords

3.4.1 expected:

Describes the behavior of the hardware in the design models assumed by this document. Other hardware design models may also be implemented.

3.4.2 mandatory:

Indicates an item that is required to be implemented as defined in this document.

3.4.3 may:

Indicates flexibility of choice with no implied preference.

3.4.4 optional:

Features that are not required to be implemented by this document. However, if any optional feature defined in this document is implemented, it shall be implemented as defined in this document.

3.4.5 shall:

Indicates a mandatory requirement.

3.4.6 should:

Indicates flexibility of choice with a preferred alternative; equivalent to the phrase "it is recommended".

3.5 Conventions

Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in 3.1 or in the text where they first appear. Names of signals are in all uppercase (e.g., DT DATA IN), lower case is used for words having the normal English meaning.

All parametric data are specified in terms of fundamental MKSA units - meters, kilograms, coulombs, seconds - and their derivatives - ohms, henrys, mhos, farads, volts, amperes, etc.

Numbers that are not immediately followed by lower-case b or h are decimal values.

Numbers immediately followed by lower-case b (xxb) are binary values.

Numbers immediately followed by lower-case h (xxh) are hexadecimal values.

Numbers immediately followed by a lower-case n (xxn) are a specific signal in a connector.

Numbers immediately followed by an upper case N' (xxN' - pronounced "xxN primed") are a specific connector number.

Decimals are indicated with a comma (e.g., two and one half is represented as 2,5).

Decimal numbers having a value exceeding 999 are represented with a space (e.g., 24 255).

An alphanumeric list (e.g., a, b, c or A, B, C) of items indicate the items in the list are unordered.

A numeric list (e.g., 1, 2, 3) of items indicate the items in the list are ordered (i.e., item 1 shall occur or complete before item 2).

In the event of conflicting information the precedence for requirements defined in this standard is:

- 1) text,
- 2) tables, then
- 3) figures.

3.6 Specification of measurement equipment

Requirements for measurement equipment is called out by reference to a specific manufacturer and model in some cases because specification of all the equipment performance requirements is impractical in this document. Any equipment so specified is replaceable by equipment from other manufacturers if the performance of the equipment is substantially equivalent.

4 Overview

4.1 General

This clause defines the relationship between the constituent parts of a passive SCSI interconnect and the measurements required to verify the performance of the interconnect.

4.2 Open versus closed systems related to this standard

Open systems are those where all the components with interoperability points may be supplied by different suppliers and the resulting configuration is expected to meet the requirements at all interoperability points.

Closed systems are those that are comprised of components that nominally are similar to those used in open systems but where the exact parts used are always assembled in the same combination and in the same configuration and usually are the same part number from the same supplier.

Open systems require specification at all interoperability points (typically connectors) for any component. Closed systems only require that the signal received at the device meet the specification. Closed systems are much simpler to specify since the only requirement is the received signal.

This standard is focused on the open system assumption with the further restriction that open concatenated systems are not included in this standard. Open concatenated systems are those that allow connection of dissimilar passive interconnects (e.g. flat to round cable, cable to backplane, etc.) and specify the performance requirements at other than port-to-port interoperability points. Closed concatenated systems are comprehended within this standard if the closed system is capable of being accessed with the test fixtures and calibration procedures defined for the open system requirements. An example of a closed concatenated system is the cable assembly to passive backplane construction. In this configuration there are no requirements specified at the cable/backplane interface by SCSI standards unless an active SCSI expander port is present at that interface in which case the backplane/cable assembly connector is a SCSI device connector (the device being the expander). With the expander present, the system becomes an open system and both the cable assembly and the passive part of the backplane are separately covered by this document. See also 4.6.

4.3 Structural considerations

4.3.1 SCSI interconnects

The collection of wires, connectors and circuits that form the electrical path between SCSI device connectors are SCSI interconnects. If the path between the SCSI device connectors does not contain any expanders or other active circuits the interconnect is passive. This standard addresses only passive SCSI interconnects.

This clause defines the structural variations of the interconnect and the physical measurement points to be used. In general, passive SCSI interconnects are complex multi-port circuits whose performance is considered from every initiator connector in the interconnect assembly to every target connector in the interconnect assembly. Requirements are also specified for connectors that support only SCSI bus segment termination.

Performance requirements for interconnect assemblies are limited to configurations that do not contain any bus segment path connectors except those within a stub length of the end of the SCSI bus segment (at the terminator). The following constitute the basic building blocks of passive interconnect:

- a) conductors (wire and backplane)
- b) connectors
- c) transition regions (connector termination / comb out / lacing regions / vias)

Interconnect that contains enabled integral terminators are addressed in this standard even though the terminators themselves are active components and, strictly speaking, make the interconnect non-passive. If enabled integral terminators exist, the enabled integral terminators eliminate the requirement for using a standard load with an enabled terminator in that position. See 4.9.2. For interconnect that contains disabled terminators the disabled terminator shall be considered as part of the interconnect assembly under test.

All measurements are specified through a mated connector. This means that the test fixture specification is critical since part of the tested interconnect remains with the test environment and part is removable with the interconnect assembly under test.

4.3.2 SCSI passive interconnect topology

SCSI interconnects have an N'-port construction where every connector is a possible SCSI device port and all ports are directly connected to each other in a multidrop topology. Since SCSI is a parallel bus every connector also contains a multiplicity of signal level ports (one for every differential signal).

A SCSI passive interconnect is characterized by the number of connectors and the number of signals. n ranges from 1 to 27. N' is determined by the structure of the passive interconnect and ranges from 2 to 18 (16 devices + 2 terminators). A SCSI passive interconnect may contain up to $18 \times 27 = 486$ signal level ports.

4.3.3 Interconnect sub-assemblies, transition regions and bulk cable

A passive interconnect with the connectors removed is termed an interconnect sub-assembly.

Transition regions are parts of an interconnect assembly between the uniform part of the bulk cable and the connector attachment. The term "multidrop" is used to describe constructions that have transition regions in addition to those needed to attach the end connectors. Examples of interconnect sub assemblies are: twist and flat, round cable prepared for termination to connectors and printed circuit boards without connectors.

Bulk cable is the collection of conductors and associated insulation used between the connectors or non-permanent transition regions (e.g. comb out) in a passive SCSI interconnect. Non-permanent transition regions are not part of bulk cable. Bulk cable includes permanent transition regions (e.g., flat regions used in twist and flat type bulk cable) designed for purposes of enabling connector attachment. The term bulk cable refers to physically flexible conductors and is not used to describe printed circuit boards. Printed circuit boards without connectors are included under separate headings in the clauses associated with multidrop bulk cable due to the permanent transition regions on PCBs.

Bulk cable with permanent transition regions may also be a subassembly for some interconnect assembly designs.

This document only considers the performance requirements for complete interconnect assemblies and interconnect subassemblies that have permanent transition regions.

The term "media" is not used to refer to bulk cable or any other construction addressed in this document. Similarly, the concept of "non-uniform media" does not accurately describe the situation with multidrop constructions and is also not used herein. The term "cable sub-assembly" is used to describe bulk cable that has been modified to accommodate the next higher level of assembly, typically connectors.

4.3.4 Interconnect assemblies

An interconnect with connectors installed is termed an interconnect assembly. Each SCSI connector shall be identified by all the functions listed in 4.9.1 that the connector is expected to support in service. This requirement may be more restrictive than allowed by the SCSI architecture model (SAM). SAM allows all SCSI ports to have either the initiator role or the target role or both roles. However, in practice most SCSI ports implement only one role.

4.3.5 Relationship between SE and DF in this document

SE (single ended) and DF (differential) requirements contained in this document, are described in table 1.

Table 1 - SE and DF map

	Bulk cable	Interconnect assembly
SE	Annex A	NA
DF	Clause 5, Clause 6 and Clause 7	Clause 8, Clause 9 and Clause 10

4.4 Relationship between requirements on bulk cable and requirements on interconnect assemblies

Performance requirements on interconnect assemblies are dictated by the signal requirements specified in SPI-x at the connectors. Bulk cable testing alone does not guarantee that interconnect assemblies made using the bulk cable meet the SPI-x requirements.

Separate performance specifications for bulk cable that are independent from the interconnect assembly are defined in this document for purposes of enabling multi sourcing for bulk cable and for allowing statements of compliance for bulk cable.

Interconnect assemblies are not required to use bulk cable that conforms to the requirements for bulk cable as long as the performance of the interconnect assembly meets its requirements.

However, the signal quality loss, the propagation time and propagation time skew, the impedance, and the cross talk are significantly determined by mechanisms intrinsic to the bulk cable.

4.5 Physical measurement points

For bulk cable the performance specifications shall be measured at the point of attachment of the stripped conductors to the test fixture. For the interconnect assemblies the performance specifications shall be measured through the mated connectors.

4.6 Concatenated configurations

Bus segments comprised of multiple interconnect assemblies connected together with one or more bus path connectors shall be termed concatenated configurations. Examples of concatenated configurations include: round cable to round cable (similar) connected together through a connector, round cable to flat cable (dissimilar) connected together with a connector, shielded cable connected to backplane with no expander on the backplane near the connector (dissimilar) and other combinations of construction. The performance of concatenated SCSI bus segments is not guaranteed by each of the constituent interconnect assemblies meeting the requirements in a non-concatenated configuration.

Interoperability points, as described in 4.7, shall not be specified at bus path connectors in concatenated configurations. If the point of connection between the sections of dissimilar physical construction is permanent, then the interconnect assembly for the entire SCSI bus segment may be treated as a single interconnect assembly whose performance requirements are addressed by this document.

4.7 Interoperability points

Interoperability points are physical points in the system where performance requirements exist at separable connectors and where it is required that the components on either side of the connector may be supplied from different compliant vendors. Interoperability points only apply to interconnect assemblies.

Following is a sample list where interoperability might be expected in a SCSI segment. A “Y” following the position designation means that this is considered an interoperability point in this standard. Similarly, a “N” following the position designation means that the point is not considered an interoperability point in this standard.

- a) Disk drive connector mounted directly on the disk drive (Y)
- b) HBA connector external connector with no internal cable on the same segment (Y)
- c) HBA internal SCSI connector to internal cables with no external cable on the same segment (Y)
- d) Motherboard SCSI connector where the mother board contains the HBA (in an ASIC) on board (Y)
- e) Backplane connector that directly accepts a disk drive or other SCSI device (Y)
- f) Backplane connector that directly connects an external cable assembly to an expander on the backplane (Y)
- g) External cable assembly connector that connects to an external connector of an HBA with no internal cable on the same segment (Y)
- h) External cable assembly connector that connects to an external connector of a disk drive array containing an expander immediately behind the external connector (Y)
- i) Internal cable connector that directly connects to a disk drive or other SCSI device (Y)
- j) Connectors that have a separable terminator attached (Y)
- k) HBA internal SCSI connector to the mother board (N)
- l) External connector to a box that has external cable assembly attached and an internal cable assembly attached to the same connector (including the case where a short cable assembly is used between the HBA and the bulkhead in a PC-like packaging (N)
- m) Internal cable assembly connector for a short cable assembly used between the disk drive and the backplane (N)
- n) HBA external bulkhead connector and internal connector when both internal and external cables are attached (N)
- o) External cable assembly connector and backplane connector when the external cable assembly is attached directly to a backplane (N)

4.8 Constructions considered

This document addresses the performance of the following types of constructions. Other constructions may also be measured using similar procedures.

Point-to-point bulk cable:

- flat planar (ribbon)
- unshielded round
- shielded round *

Multi-drop bulk cable or printed circuit boards (unpopulated)

- twisted and flat planar (ribbon) *
- unshielded round
- printed circuit boards *

Point-to-point interconnect assemblies:

- two connector shielded *
- two connector unshielded

Multi-drop interconnect assemblies:

- multi-connector cable (e.g. external daisy chain)
- backplanes: (multi-connector) *

*most common constructions

4.9 Identification, constraints and loading requirements

4.9.1 Connector function identification

All connectors in the interconnect assembly shall be identified as one or more of the following 14 functions:

- a) open
- b) transmitter for initiator device with enabled terminator
- c) receiver for initiator device with enabled terminator
- d) transmitter for initiator device with no enabled terminator
- e) receiver for initiator device with no enabled terminator
- f) transmitter for target device with enabled terminator
- g) receiver for target device with enabled terminator
- h) transmitter for target device with no enabled terminator
- i) receiver for target device with no enabled terminator
- j) enabled terminator only
- k) feed through enabled terminator with transmitter for initiator device with no enabled terminator attached on the other side of the terminator
- l) feed through enabled terminator with receiver for initiator device with no enabled terminator attached on the other side of the terminator
- m) feed through enabled terminator with transmitter for target device with no enabled terminator attached on the other side of the terminator
- n) feed through enabled terminator with receiver for target device with no enabled terminator attached on the other side of the terminator

4.9.2 Constraints

The following configurations are used for specifying the level 1 tests in this standard:

- a) point to point shielded
- b) unshielded multidrop bulk cable up to 3 m, up to 16 drops
- c) multidrop backplanes up to 16 drops

This document does not consider configurations where another interconnect assembly is attached to a connector in the interconnect assembly under test. Concatenated configurations are not considered - for example: round cable to flat; shielded cable to backplane with no expander; shielded round to shielded round etc. are all concatenated configurations.

Each function for each connector requires a specific load to be in place during the interconnect assembly testing process, see 4.9.1.

The position of the enabled terminators shall be defined for every measurement of interconnect assembly performance. The standard load appropriate for the connectors with the enabled terminators attached shall be attached. Loading conditions for the remaining connectors in the interconnect assembly under test shall meet both of the following requirements.

- a) All SCSI device ports not attached to devices with enabled terminators have a standard load appropriate for the function of the connector in place during the measurement.
- b) Any one target port not attached to devices with enabled terminators shall have the standard load removed to simulate hot plugging conditions.

4.9.3 Standard loads

4.9.3.1 Targets and initiators with no enabled terminator

Standard loads for targets and initiators with no enabled terminator shall have the following properties:

- a) be identified by the connector type, SCA-2, VHDCI, or HD68,
- b) be optimized for SPI-5,
- c) the capacitance at the connector interface shall be held to a tolerance of $\pm 1,0$ pF at the connector,
- d) the nominal signal to ground capacitances of the various portions of the standard load shall be
 - 2 pF for the connector,
 - 2 pF for the trace,
 - 1 pF for the via/pad and
 - 6 pF the chip input capacitance,
- e) the nominal signal to signal capacitance shall be 6,0 pF,
- f) the distance from connector interface to chip capacitance shall be $37,5 \text{ mm} \pm 2,0 \text{ mm}$ and
- g) the PCB impedance shall be $122 \Omega \pm 10 \Omega$ and shall match the SPI-5 specification.

4.9.3.2 Targets and initiators with enabled terminator

Standard loads for initiators and targets with an enabled terminator shall have the following properties:

- a) be identified by the connector type, SCA-2, VHDCI, or HD68,
- b) be optimized for SPI-5,
- c) the capacitance at the connector interface shall be held to a tolerance of $\pm 1,0$ pF at the connector,
- d) the nominal signal to ground capacitances of the various portions of the standard load shall be:
 - 2 pF for the connector,
 - 2 pF for the trace,
 - 1 pF for the via/pad,
 - 6 pF for the chip input capacitance and
 - 3 pF for the terminator,
- e) the nominal signal to signal capacitance shall be 9,0 pF,
- f) the distance from connector interface to chip capacitance shall be $47,5 \text{ mm} \pm 2,0 \text{ mm}$,
- g) the distance from the connector interface to the terminator shall be $27,5 \pm 2,0 \text{ mm}$ and
- h) the PCB impedance shall be $122 \Omega \pm 10 \Omega$ and shall match the SPI-5 specifications.

4.10 Nature of requirements

4.10.1 Measurements and tests

A measurement is the process of acquiring data that indicates a property of the bulk cable or interconnect assembly of interest. A test is a measurement to which a pass-fail criteria is applied.

4.10.2 Performance levels and applications

Several parameters are required to verify electrical performance. Measurement of passive interconnect performance is divided into two levels:

- a) level 1: those used to verify compliance to the requirements set forth in SPI-x or in this document, and
- b) level 2: those needed to aid in the diagnosis of the causes of degraded performance, to setup the conditions for executing a level 1 measurement, or as additional characterization of the interconnect but are not required for specification compliance.

Since level 1 measurements are intended to determine compliance to requirements, and performance level all level 1 measurements are tests as defined above. No level 2 measurements are tests.