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INTERNATIONAL STANDARD



**Information technology – Small computer system interface (SCSI) –
Part 153: Serial attached SCSI - 2.1 (SAS-2.1)**





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Part 153: Serial attached SCSI - 2.1 (SAS-2.1)**

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INFORMATION TECHNOLOGY – SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 153: SERIAL ATTACHED SCSI - 2.1 (SAS-2.1)

FOREWORD

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This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2, as far as is practicable.

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INTRODUCTION

General

The SCSI family of standards provides for many different transport protocols that define the rules for exchanging information between different SCSI devices. This standard specifies the functional requirements for the Serial Attached SCSI (SAS) physical interconnect, which is compatible with the Serial ATA physical interconnect. The SAS Protocol Layer (SPL) standard documents the SAS protocol layer corresponding to the Serial Attached SCSI - 2.1 (SAS-2.1) and beyond, defining the rules for exchanging information between SCSI devices using a serial interconnect. Other SCSI transport protocol standards define the rules for exchanging information between SCSI devices using other interconnects.

SCSI standards family

Figure 1 shows the relationship of this standard to the other standards and related projects in the SCSI family of standards.

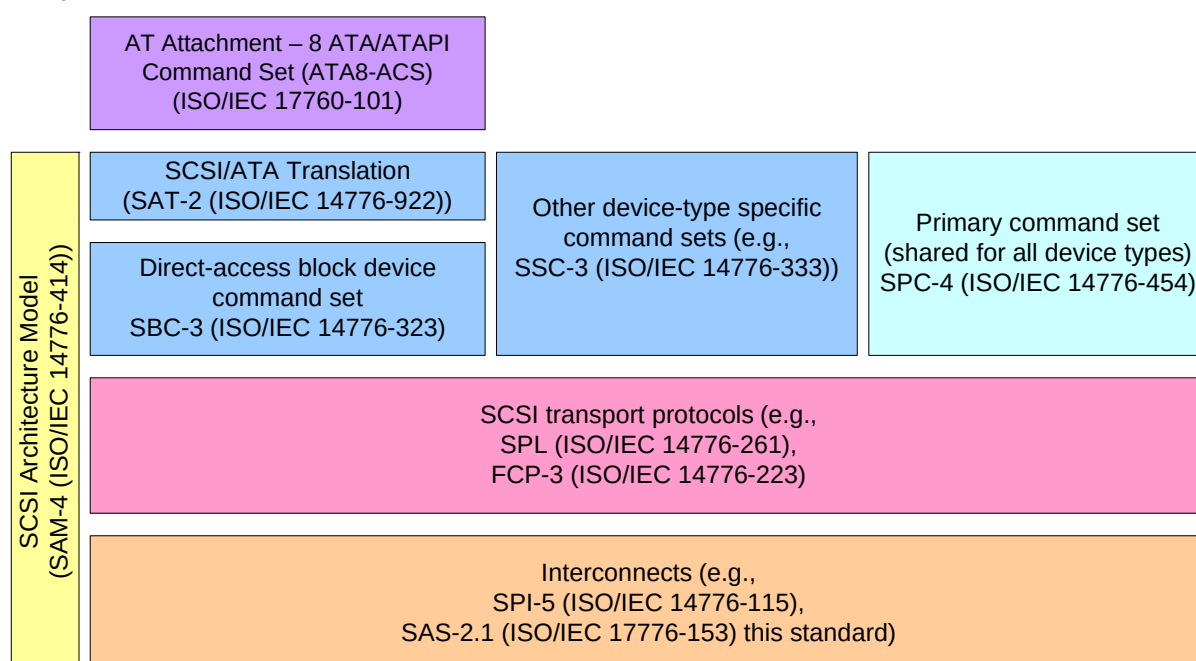


Figure 1 — SCSI document relationships

Figure 2 shows the relationship of this standard to other standards and related projects in the ATA family of standards.

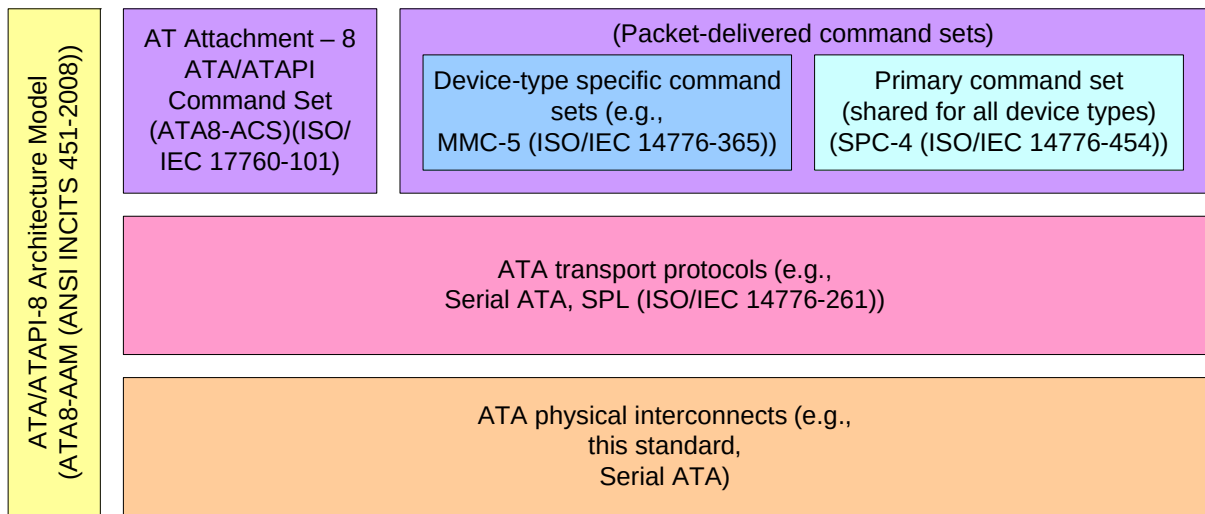


Figure 2 — ATA document relationships

Figure 1 and figure 2 show the general relationship of the documents to one another, and do not imply a relationship such as a hierarchy, protocol stack or system architecture.

These standards specify the interfaces, functions and operations necessary to ensure interoperability between conforming implementations. This standard is a functional description. Conforming implementations may employ any design technique that does not violate interoperability.

INFORMATION TECHNOLOGY – SMALL COMPUTER SYSTEM INTERFACE (SCSI) –

Part 153: SERIAL ATTACHED SCSI - 2.1 (SAS-2.1)

1 Scope

This part of ISO/IEC 14776 defines the physical layer of the Serial Attached SCSI (SAS) interconnect.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 14165-117, *Information technology – Fibre channel – Part 117: Methodologies for jitter and signal quality (MJSQ)*^{1 2}

ISO/IEC 14776-261, *Information technology – Small Computer System Interface (SCSI) – Part 261: SAS Protocol Layer (SPL)*³

ISO/IEC 14776-414, *Information technology – Small Computer System Interface (SCSI) – Part 414: SCSI Architecture Model - 4 (SAM-4)*

ANSI INCITS 451-2008, *Information technology – AT Attachment-8 ATA/ATAPI Architecture Model (ATA8-AAM)*

For information on the current status of the listed documents, or regarding availability, contact the indicated organization.

Serial ATA Revision 3.0 (SATA). 2 June 2009

NOTE 1 For more information on Serial ATA international Organization, see www.sata-io.org.

SFF-8086, *Compact Multilane Series: Common Elements*

SFF-8087, *Compact Multilane Series: Unshielded*

SFF-8088, *Compact Multilane Series: Shielded*

SFF-8147, *54mm x 71mm Form Factor w/micro SAS Connector*

SFF-8223, *2.5" Drive Form Factor with Serial Connector*

SFF-8323, *3.5" Drive Form Factor with Serial Connector*

SFF-8410, *HSS Copper Testing and Performance Requirements*

SFF-8416, *Measurement and Performance Requirements for HPEI Bulk Cable*

SFF-8436, *QSFP+ Copper and Optical Modules*

SFF-8449, *Mini Multilane Series Management Interface*

SFF-8460, *HSS Backplane Design Guidelines*

SFF-8482, *Unshielded Dual Port Serial Attachment Connector*

1. ANSI INCITS TR-35-2004

2. When MJSQ is referenced from this standard, the FC Port terminology used within MJSQ should be substituted with SAS phy terminology.

3. T10/2124-D

SFF-8484, *Multi-Lane Unshielded Serial Attachment Connectors*

SFF-8485, *Serial GPIO (SGPIO) Bus*

SFF-8486, *Serial Attachment Micro Connector*

SFF-8523, *5.25" Drive Form Factor with Serial Connector*

SFF-8643, *Mini Multilane Series: Unshielded HD Integrated Connector*

SFF-8644, *Mini Multilane Series: Shielded HD Integrated Connector*

NOTE 2 For more information on the current status of SFF documents, contact the SFF Committee at 408-867-6630 (phone), or 408-867-2115 (fax). To obtain copies of these documents, contact the SFF Committee at 14426 Black Walnut Court, Saratoga, CA 95070 at 408-867-6630 (phone) or 408-741-1600 (fax) or see <http://www.sffcommittee.org>.

ASTM Standard B 258-02, 2002, *Standard specification for standard nominal diameters and cross-sectional areas of AWG sizes of solid round wires used as electrical conductors*, ASTM International, West Conshohocken, PA, USA.

NOTE 3 For more information on ASTM International standards, see www.astm.org.

PANTONE® Color Formula Guide

NOTE 4 Pantone® and PANTONE MATCHING SYSTEM® are registered trademarks of Pantone, Inc. For more information on Pantone colors, contact Pantone, Inc. (see <http://www.pantone.com>). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

Touchstone® File Format Specification. Revision 1.1. IBIS Open Forum.

NOTE 5 Touchstone® is a registered trademark of Agilent Corporation. For more information on the Touchstone specification, contact the IBIS Open Forum (see <http://www.eigroup.org>). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

MATLAB® 7 Programming Fundamentals. Release 2008b.

NOTE 6 MATLAB® is a registered trademark of The MathWorks, Inc. For more information on MATLAB, contact The Mathworks, Inc. (see <http://www.mathworks.com>). This information is given for the convenience of users of this standard and does not constitute an endorsement by [ISO or IEC] of the product named. Equivalent products may be used if they can be shown to lead to the same results.

3 Terms, definitions, symbols, abbreviations, keywords, and conventions

3.1 Terms and definitions

For the purposes of this document the following terms and definitions apply.

3.1.1

active cable assembly

cable assembly (see 3.1.9) that requires power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.2

AT Attachment

ATA

standard for the internal attachment of storage devices to hosts

Note 1 to entry: See ATA8-AAM.

3.1.3

baud rate

nominal signaling speed, expressed as the maximum number of times per second that the signal (see 3.1.87) may change the state of the physical link (see 3.1.66)

Note 1 to entry: Each state change produces a transition (i.e., signal edge).

Note 2 to entry: The baud rate is the reciprocal of the *UI* (i.e., $f_{\text{baud}} = 1 / UI$) (see 3.1.103).

3.1.4

bit error ratio

BER

number of logical bits output from a receiver circuit that differ from the correct transmitted logical bits, divided by the number of transmitted logical bits

Note 1 to entry: The BER is computed on the raw bit stream before 10b8b decoding.

Note 2 to entry: The BER is usually expressed as a coefficient and a power of 10 (e.g., 2 erroneous bits out of 100 000 bits transmitted is expressed as 2 out of 10^5 or 2×10^{-5}).

Note 3 to entry: See MJSQ.

3.1.5

bit time

nominal duration of a signal transmission bit (e.g., 666,6 ps at 1,5 Gbit/s, 333,3 ps at 3 Gbit/s, and 166,6 ps at 6 Gbit/s)

3.1.6

bounded uncorrelated jitter

BUJ

part of DJ (see 3.1.23) not aligned in time with the signal being measured; specifically, BUJ excludes ISI (see 3.1.47) and duty cycle distortion

Note 1 to entry: See MJSQ.

3.1.7

burst time

part of an OOB signal (see 3.1.60) where the OOB burst (see 3.1.56) is transmitted (see 5.9)

3.1.8

byte

sequence of eight contiguous bits considered as a unit

3.1.9

cable assembly

bulk cable with a separable connector at each end plus any retention, backshell, shielding features, or circuitry used for cable management or signal transmission

Note 1 to entry: See 5.4.3.

3.1.10

clock data recovery

CDR

function provided by the receiver circuit responsible for producing a regular clock signal (i.e., the recovered clock) from the received signal and for aligning the recovered clock to the symbols (i.e., bits) being transmitted with the signal

Note 1 to entry: The CDR uses the recovered clock to recover the bits.

Note 2 to entry: See MJSQ.

3.1.11

common SSC transmit clock

implementation that employs a single transmit clock for multiple transmitter devices and enables or disables SSC (see 5.7.6) on the transmit clock signal to all transmitter devices in common rather than allowing each transmitter device to independently control SSC

3.1.12

compliance point

interoperability point where interoperability specifications are met

Note 1 to entry: See 5.3.

3.1.13

compliant jitter tolerance pattern

CJTPAT

test pattern for jitter testing

Note 1 to entry: See 5.7.3.5 and Annex A.

3.1.14

connector

electro-mechanical components consisting of a receptacle and a plug that provide a separable interface between two transmission segments

Note 1 to entry: See 5.4.3.

3.1.15

cumulative distribution function

CDF

probability that jitter (see 3.1.48) is less than a given value

Note 1 to entry: See MJSQ.

3.1.16

D.C. idle

differential signal level that is nominally 0 V(P-P), used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60) when D.C. mode (see 3.1.17) is enabled

Note 1 to entry: See 5.7.4.

3.1.17

D.C. mode

mode in which D.C. idle (see 3.1.16) is used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60)

3.1.18

data dependent jitter

DDJ

jitter (see 3.1.48) that is added when the transmission pattern is changed from a clock-like to a non-clock-like pattern

Note 1 to entry: See MJSQ.

3.1.19

decibel

dB

ten times the common logarithm (i.e., $\log_{10}$) of the ratio of relative powers

Note 1 to entry: The ratio of powers P_1 and P_2 in dB is $10 \times \log_{10} (P_1 / P_2)$. If $P_1 = V_1^2 / R_1$, $P_2 = V_2^2 / R_2$, and $R_1 = R_2$, then this ratio is equivalent to 20 times the common logarithm of the relative voltage ratio (i.e., $\text{dB} = 20 \times \log_{10} (V_1 / V_2)$). A ratio of 1 results in a dB value of 0 (e.g., $20 \times \log_{10} (1) = 0 \text{ dB}$), a ratio greater than 1 results in a positive dB value (e.g., $20 \times \log_{10} (2) = 6 \text{ dB}$) and a ratio less than 1 results in a negative dB value (e.g., $20 \times \log_{10} (0.5) = -6 \text{ dB}$).

3.1.20

dB millivolts

dBmV

decibel ratio of an RMS voltage value relative to 1 mV

Note 1 to entry: 20 mV(r.m.s.) is equal to $20 \times \log_{10} (20 \text{ mV} / 1 \text{ mV}) = 26 \text{ dBmV}$; this does not depend on the impedance level.

3.1.21

dB milliwatts

dBm

decibel ratio of a power value relative to 1 mW

Note 1 to entry: 20 mW is equal to $10 \times \log_{10} (20 \text{ mW} / 1 \text{ mW}) = 13 \text{ dBm}$. If power is measured with a 50Ω impedance level, then 20 mW is equivalent to $(0.02 \text{ W} \times 50 \Omega)^{(1/2)} = 1 \text{ V}$ or 60 dBmV. If power is measured with a 25Ω impedance level (i.e., the reference impedance for common mode measurements), then 20 mW is equivalent to $(0.02 \text{ W} \times 25 \Omega)^{(1/2)} = 0.707 \text{ V}$ or 57 dBmV.

3.1.22

decision feedback equalizer

DFE

nonlinear equalizer that uses a feedback loop based on previously decoded symbols

3.1.23

deterministic jitter

DJ

jitter (see 3.1.48) with non-Gaussian distribution that is bounded in amplitude and has specific causes

Note 1 to entry: See MJSQ.

3.1.24

direct current

D.C.

non-A.C. component of a signal

Note 1 to entry: In this standard, all frequency components below 100 kHz.

3.1.25

disparity

difference between the number of ones and zeros in a character

Note 1 to entry: See SPL.

3.1.26

dispersion

signal pulse broadening and distortion from all causes

3.1.27

duty cycle distortion

DCD

one-half of the difference of the average width of a one and the average width of a zero in a signal waveform eye pattern measurement

Note 1 to entry: See MJSQ.

3.1.28

dword

sequence of four contiguous bytes or four contiguous characters considered as a unit

Note 1 to entry: See SPL.

3.1.29

electromagnetic interference

EMI

any electromagnetic disturbance that interrupts, obstructs, or otherwise degrades or limits the effective performance of electronics/electrical equipment

3.1.30

enclosure

box, rack, or set of boxes providing the powering, cooling, mechanical protection, EMI protection, and external electronic interfaces for one or more end device(s) (see 3.1.34) and/or expander device(s) (see SPL)

Note 1 to entry: The enclosure provides the outermost electromagnetic boundary and acts as an EMI barrier.

3.1.31

enclosure in port

set of expander phys with subtractive routing attributes using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.32

enclosure out port

set of expander phys with table routing attributes in an expander device that does not support table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.33

enclosure universal port

set of expander phys with table routing attributes in an expander device that supports table-to-table attachment using the same external connector (see 5.4.3.4)

Note 1 to entry: See SPL.

3.1.34

end device

SAS device or SATA device that is not contained within an expander device (see 3.1.36)

Note 1 to entry: See SPL.

3.1.35

etch

printed circuit board copper conductor path

3.1.36

expander device

device that is part of a service delivery subsystem (see SAM-4), facilitates communication between SAS devices (see 3.1.80) and SATA devices (see 3.1.83)

Note 1 to entry: See SPL.

3.1.37

expander phy

phy in an expander device that interfaces to a service delivery subsystem (see SAM-4)

3.1.38

expander port

expander device object that interfaces to a service delivery subsystem (see SAM-4) and to SAS ports in other devices

Note 1 to entry: See SPL.

3.1.39

external connector

bulkhead connector (see 3.1.14) that carries signals into and out of an enclosure (see 3.1.30) and exits the enclosure with only minor compromise to the shield effectiveness of the enclosure (e.g., a Mini SAS 4x receptacle or Mini SAS HD receptacle)

Note 1 to entry: See 5.4.3.4.

3.1.40

eye contour

locus of points in a signal level versus time eye diagram where the CDF of 10^{-12} in the actual signal population exists

Note 1 to entry: Comparison of the measured eye contour to the jitter eye mask determines whether a jitter eye mask violation has occurred.

Note 2 to entry: See 5.7.3 and MJSQ.

3.1.41

fall time

time interval for the falling signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 80 % and 20 % voltage levels.

Note 2 to entry: See also rise time (see 3.1.79).

3.1.42

fanout cable assembly

cable assembly with one connector on one end and multiple connectors on the other end

Note 1 to entry: See 5.4.4.1.3.

3.1.43

field

group of one or more contiguous bits

3.1.44**golden phase lock loop****golden PLL**

function that conforms to the jitter timing reference frequency response requirements in MJSQ that extracts the jitter timing reference from the data stream under test to be used as the timing reference for the instrument used for measuring the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.45**idle time**

part of an OOB signal (see 3.1.60) where OOB idle (see 3.1.16) is being transmitted

Note 1 to entry: See 5.9.

3.1.46**insertion loss**

ratio of incident power to delivered power

Note 1 to entry: The dB magnitude of S_{12} or S_{21} is the negative of insertion loss in dB.

Note 2 to entry: The insertion loss ratio is usually expressed in dB.

Note 3 to entry: See clause D.10.

3.1.47**intersymbol interference****ISI**

reduction in the distinction of a pulse caused by overlapping energy from neighboring pulses

Note 1 to entry: Neighboring pulses are pulses that are close enough to have significant energy overlapping the affected pulse and does not imply or exclude adjacent pulses (i.e., many bit times (see 3.1.5) may separate the pulses, especially in the case of reflections).

Note 2 to entry: ISI may result in DDJ and vertical eye closure.

Note 3 to entry: Several mechanisms produce ISI (e.g., dispersion, reflections, and circuits that lead to baseline wander).

Note 4 to entry: See MJSQ.

3.1.48**jitter**

collection of instantaneous deviations of signal edge times at a defined signal level of the signal from the reference times for those events

Note 1 to entry: Reference times such as times defined by the jitter timing reference.

Note 2 to entry: See MJSQ.

3.1.49**jitter timing reference**

signal used as the basis for calculating the jitter in the signal under test

Note 1 to entry: See MJSQ.

3.1.50**jitter tolerance**

ability of the receiver device to recover transmitted bits in an incoming data stream in the presence of specified jitter in the signal applied to the receiver device compliance point

Note 1 to entry: See MJSQ.

3.1.51

jitter tolerance pattern

JTPAT

test pattern for jitter testing

Note 1 to entry: See 5.7.3.5 and Annex A.

3.1.52

least mean square

LMS

algorithm for adaptively adjusting the tap coefficients of a DFE (see 3.1.22) based on the difference between the desired and actual signal

3.1.53

managed connector category

category of connectors that support a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.54

near-end crosstalk

NEXT

crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the disturbing channel

Note 1 to entry: The terminals of the disturbed channel, at which the near-end crosstalk is present, and the energized terminals of the disturbing channel are usually near each other.

3.1.55

negation time

part of an OOB signal during which OOB idle is transmitted after the last OOB burst

Note 1 to entry: See 5.9.

3.1.56

OOB burst

transmission of signal transitions or ALIGN3 primitives for a burst time (see 3.1.7)

Note 1 to entry: See 5.9.1.

3.1.57

OOB idle

transmission of D.C. idle (see 3.1.16) when D.C. mode (see 3.1.17) is enabled, or a defined sequence of dwords when optical mode (see 3.1.61) is enabled

3.1.58

OOB interval

time basis for burst times (see 3.1.7), idle times (see 3.1.45), negation times (see 3.1.55), and signal times (see 3.1.90) used to create OOB signals (see 3.1.60)

Note 1 to entry: See 5.9.1.

3.1.59

OOB sequence

sequence where two phys exchange OOB signals (see 3.1.60)

Note 1 to entry: See SPL.

3.1.60**OOB signal**

pattern of idle time (see 3.1.45), burst time (see 3.1.7), and negation time (see 3.1.55) used during the link reset sequence

Note 1 to entry: See 5.9.

3.1.61**optical mode**

mode in which a defined sequence of dwords is used during the idle time (see 3.1.45) and negation time (see 3.1.55) of an OOB signal (see 3.1.60)

Note 1 to entry: See 5.9.

3.1.62**part per million****ppm**

dimensionless unit used to express signal clock frequency deviation relative to the nominal reference frequency

Note 1 to entry: The value for ppm is obtained by multiplying the fractional variation of the measured signal clock frequency from the nominal signal clock frequency value by 1 million.

3.1.63**passive cable assembly**

cable assembly (see 3.1.9) that does not require external power for internal circuitry used in the transmission of the signal through the cable assembly

3.1.64**passive TxRx connection**

complete simplex signal path between the transmitter circuit (see 3.1.98) and receiver circuit (see 3.1.72) that does not include powered circuitry used in the transmission of the signal through the TxRx connection (see 3.1.101)

Note 1 to entry: See 5.5.1.

3.1.65**phy**

object in a device that is used to interface to other devices

Note 1 to entry: Other devices are, for example, an expander phy (see 3.1.37) or a SAS phy (see 3.1.81).

Note 2 to entry: See 4.1.

3.1.66**physical link**

two differential signal pairs, one pair in each direction, that connect two physical phys (see 3.1.68)

Note 1 to entry: See 4.1.

3.1.67**physical link rate**

link rate between two physical phys established as a result of speed negotiation between those phys

3.1.68**power on**

power being applied

3.1.69**probe point**

physical position in a test load where signal characteristics for compliance points are measured

Note 1 to entry: See 5.6.

3.1.70

random jitter

RJ

jitter (see 3.1.48) characterized by a Gaussian distribution and that is unbounded

Note 1 to entry: See MJSQ.

3.1.71

rate

data transfer rate of a physical or logical link

Note 1 to entry: Typical data transfer rates are 1.5 Gbit/s, 3 Gbit/s, or 6 Gbit/s.

3.1.72

receiver circuit

electronic circuit that converts an analog serial input signal to a logic signal

3.1.73

receiver device

Rx

device downstream from a receiver device compliance point (see 3.1.12) containing a portion of the physical link and a receiver circuit (see 3.1.72)

3.1.74

reference receiver device

set of parameters defining electrical performance characteristics that provide a set of minimum electrical performance requirements for a receiver device and that are also used in mathematical modeling to determine compliance of a TxRx connection or transmitter device

Note 1 to entry: See 5.7.5.7.3.

3.1.75

reference transmitter device

set of parameters defining electrical performance characteristics of a transmitter device that are used in mathematical modeling to determine compliance of a TxRx connection

Note 1 to entry: See 5.7.4.6.5.

3.1.76

reference transmitter test load

set of S-parameters defining the electrical characteristics of a TxRx connection used as the basis for transmitter device and receiver device performance evaluation through mathematical modeling

Note 1 to entry: See 5.6.5.

3.1.77

reflection coefficient

ρ

ratio of reflected voltage to incident voltage

3.1.78

return loss

ratio of incident power to reflected power

Note 1 to entry: The dB magnitude of S_{11} or S_{22} is the negative of return loss in dB.

Note 2 to entry: Return loss is usually expressed in decibel (dB).

Note 3 to entry: See clause D.10.

3.1.79

rise time

time interval for the rising signal edge to transit between specified percentages of the signal amplitude

Note 1 to entry: In this standard, the measurement points are the 20 % and 80 % voltage levels.

Note 2 to entry: See fall time (see 3.1.41).

3.1.80

SAS device

SAS initiator device and/or a SAS target device

Note 1 to entry: See SPL.

3.1.81

SAS phy

phy in a SAS device (see 3.1.80) that interfaces to a service delivery subsystem

Note 1 to entry: See SAM-4.

3.1.82

SAS target device

device containing SSP, STP, and/or SMP target ports in a SAS domain

Note 1 to entry: See SPL.

3.1.83

SATA device

ATA device (see ATA8-AAM) that contains a SATA device port in an ATA domain

Note 1 to entry: See SPL.

3.1.84

SATA phy

phy in a SATA device or SATA port selector that interfaces to a service delivery subsystem

Note 1 to entry: For ATA device (see SPL), for SATA port selector (see SPL), and for a service delivery subsystem (see SAM-4).

Note 2 to entry: Analogous to a SAS phy (see 3.1.81).

3.1.85

Serial ATA

protocol defined by SATA

Note 1 to entry: See SATA.

3.1.86

Serial Attached SCSI

set of protocols defined in SPL and the interconnect defined by this standard

Note 1 to entry: See SAS.

3.1.87

signal

detectable transmitted energy that is used to carry information

3.1.88

signal amplitude

property of the overall signal (see 3.1.87) that describes the peak or peak-to-peak values of the signal level (see 3.1.89)

3.1.89**signal level**

instantaneous intensity of a signal (see 3.1.87) measured in volts

3.1.90**signal time**

time of an OOB signal (see 3.1.60), consisting of six burst times (see 3.1.7), six idle times (see 3.1.45), and one negation time (see 3.1.55)

Note 1 to entry: See 5.9.

3.1.91**signal tolerance**

ability of the receiver device to recover transmitted bits in an incoming data stream with maximum jitter and minimum amplitude

Note 1 to entry: See MJSQ.

3.1.92**sinusoidal jitter****SJ**

single frequency jitter (see 3.1.48) applied during signal tolerance testing

3.1.93**spread spectrum clocking****SSC**

technique of modulating the operating frequency of a transmitted signal to reduce the measured peak amplitude of radiated emissions

Note 1 to entry: The operating frequency of a transmitted signal is the physical link rate.

Note 2 to entry: See SPL.

3.1.94**symbol**

smallest unit of data transmission on a physical link

Note 1 to entry: The smallest unit of data is a bit.

Note 2 to entry: A symbol represents a single transition if the maximum transition rate (i.e., a 0101b pattern) is occurring.

3.1.95**total jitter****TJ**

jitter (see 3.1.48) from all sources

Note 1 to entry: See MJSQ.

3.1.96**trained**

physical link rate negotiated with Train-SNW

Note 1 to entry: See SPL.

3.1.97**transceiver**

physical entity that contains both a transmitter device (see 3.1.100) and a receiver device (see 3.1.73)

3.1.98**transmitter circuit**

electronic circuit that converts a logic signal to an analog serial output signal

3.1.99**transmitter compliance transfer function****TCTF**

mathematical statement of the transfer function through which the transmitter shall be capable of producing acceptable signals as defined by a receive mask

Note 1 to entry: See 5.7.4.1.

3.1.100**transmitter device****Tx**

device upstream from a transmitter device compliance point (see 3.1.12) containing a portion of the physical link and a transmitter circuit (see 3.1.98)

3.1.101**TxRx connection**

complete simplex signal path between the transmitter circuit (see 3.1.98) and receiver circuit (see 3.1.72)

Note 1 to entry: See 5.5.1.

3.1.102**TxRx connection segment**

that portion of a TxRx connection (see 3.1.101) delimited by separable connectors or changes in the conductive material

Note 1 to entry: See 5.5.1.

3.1.103**unit interval****UI**

normalized, dimensionless, nominal duration of a symbol (see 3.1.94)

Note 1 to entry: Typical UIs are 666.6 ps at 1.5 Gbit/s, 333.3 ps at 3 Gbit/s, and 166.6 ps at 6 Gbit/s, for example.

Note 2 to entry: The UI is the reciprocal of the baud rate (i.e., $UI = 1 / f_{\text{baud}}$) (see 3.1.3).

3.1.104**unmanaged active connector category**

category of connectors that support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2), but do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.105**unmanaged passive connector category**

category of connectors that do not support power for Mini SAS 4x active external cable assemblies (see 5.4.4.2.2) and do not support cable assemblies with a cable management interface

Note 1 to entry: See 5.4.3.2.

3.1.106**untrained**

physical link rate not negotiated with Train-SNW

Note 1 to entry: See SPL.

3.1.107**usage variable**

SASWDP parameter set to a value that determines if the stressor file is to be added to the simulation

Note 1 to entry: See Annex B.

3.1.108

voltage modulation amplitude

VMA

difference in electrical voltage of a signal (see 3.1.87) between the stable one level and the stable zero level

3.1.109

waveform dispersion penalty

WDP

simulated measure of the deterministic penalty of the signal waveform from a particular transmitter device transmitting a particular pattern and a particular test load with a reference receiver device

Note 1 to entry: See 5.7.4.6.1 and Annex B.

3.2 Symbols and abbreviations

3.2.1 Abbreviations

See clause 2 for abbreviations of standards bodies (e.g., ISO). Abbreviations used in this standard:

Abbreviation	Meaning
A.C.	alternating current (a.c. within a sentence)
ATA	AT attachment (see 3.1.1)
ATAPI	AT attachment packet interface
ATA8-AAM	AT Attachment - 8 ATA/ATAPI Architecture Model standard (see clause 2)
AWG	American wire gauge (see ASTM Standard B 258-02) (see clause 2)
BER	bit error ratio (see 3.1.4)
BUJ	bounded uncorrelated jitter (see 3.1.6)
CDF	cumulative distribution function (see 3.1.15)
CDR	clock data recovery (see 3.1.10)
CIC	compliance interconnect channel (see SATA)
CJTPAT	compliant jitter tolerance pattern (see 3.1.13)
CR	inter-enclosure (i.e., cabinet) receiver device compliance point (see 5.3)
CT	inter-enclosure (i.e., cabinet) transmitter device compliance point (see 5.3)
D.C.	direct current (see 3.1.24)
DCD	duty cycle distortion (see 3.1.27)
DDJ	data dependent jitter (see 3.1.18)
DFE	decision feedback equalizer (see 3.1.22)
DJ	deterministic jitter (see 3.1.23)
EMI	electromagnetic interference (see 3.1.29)
ESD	electrostatic discharge
G1	generation 1 physical link rate (i.e., 1.5 Gbit/s)
G2	generation 2 physical link rate (i.e., 3 Gbit/s)
G3	generation 3 physical link rate (i.e., 6 Gbit/s)
Gen1i	SATA generation 1 physical link rate (i.e., 1.5 Gbit/s) (see SATA)
Gen2i	SATA generation 2 physical link rate (i.e., 3 Gbit/s) (see SATA)
Gen3i	SATA generation 3 physical link rate (i.e., 6 Gbit/s) (see SATA)

Abbreviation	Meaning
GPIO	general purpose input/output
HD	high-density
IR	intra-enclosure (i.e., internal) receiver device compliance point (see 5.3)
ISI	intersymbol interference (see 3.1.47)
IT	intra-enclosure (i.e., internal) transmitter device compliance point (see 5.3)
JMD	jitter measurement device
JTF	jitter transfer function (see 5.7.3.2)
JTPAT	jitter tolerance pattern (see 3.1.51)
LED	light-emitting diode
LMS	least mean square (see 3.1.52)
N/A	not applicable
NEXT	near-end crosstalk (see 3.1.54)
OOB	out-of-band
OOBI	out-of-band interval (see 3.1.58)
PCB	printed circuit board
PJ	periodic jitter
PLL	phase lock loop
P-P	peak-to-peak
RD	running disparity (see SPL)
RJ	random jitter (see 3.1.70)
RMS	root mean square
RTTL	reference transmitter test load (see 3.1.76)
Rx	receiver device (see 3.1.73)
SAM-4	SCSI Architecture Model - 4 standard (see clause 2)
SAS	Serial Attached SCSI (see 3.1.86)
SATA	Serial ATA (see 3.1.85) or the Serial ATA 3.0 specification (see clause 2)
SCSI	Small Computer System Interface
SGPIO	serial GPIO
SJ	sinusoidal jitter (see 3.1.92)
SMA	subminiature version A connector
SPC-4	SCSI Primary Commands - 4 standard
SPL	SAS Protocol Layer (see clause 2)
SSC	spread spectrum clocking
STP	Serial ATA Tunneled Protocol
TCTF	transmitter compliance transfer function (see 3.1.99)
TDNA	time domain network analyzer (i.e., TDR/TDT plus analysis software that performs a VNA-style output)
TDR	time domain reflectometer
TDT	time domain transmission
TJ	total jitter (see 3.1.95)
Tx	transmitter device (see 3.1.100)
VMA	voltage modulation amplitude (see 3.1.108)
VNA	vector network analyzer

Abbreviation	Meaning
WDP	waveform dispersion penalty (see 3.1.109)

3.2.2 Units

Units used in this standard:

Units	Meaning
dB	decibel (see 3.1.19)
dBm	decibel milliwatts (see 3.1.21)
dBmV	decibel millivolts (see 3.1.20)
Gbit/s	gigabits per second (i.e., 10^9 bits per second)
GHz	gigahertz (i.e., 10^9 cycles per second)(i.e., s^{-9})
Hz	hertz (i.e., cycles per second)(i.e., s^{-1})
kHz	kilohertz (i.e., 10^3 cycles per second)(i.e., s^{-3})
μ A	microampere (i.e., 10^{-6} amperes)
μ s	microsecond (i.e., 10^{-6} seconds)
m	meter
mA	milliampere (i.e., 10^{-3} amperes)
MB/s	megabytes per second (i.e., 10^6 bytes per second)
MHz	megahertz (i.e., 10^6 cycles per second)(i.e., s^{-6})
ms	millisecond (i.e., 10^{-3} seconds)
mV	millivolt (i.e., 10^{-3} volts)
mW	milliwatt (i.e., 10^{-3} watts)
nF	nanofarad (i.e., 10^{-9} farads)
ns	nanosecond (i.e., 10^{-9} seconds)
ppm	parts per million (i.e., 10^{-6})
ps	picosecond (i.e., 10^{-12} seconds)
r.m.s.	root mean square (i.e., quadratic mean)
s	second (unit of time)
sgn	signum function (i.e., sign function)
UI	unit interval (see 3.1.103)
V	volt
W	watt

3.2.3 Symbols

Symbols used in this standard:

Symbols	Meaning
Dxx.y	data character (see 3.1.18)
S_{ij}	S-parameter for port j to port i (see D.10)
S_{CCij}	S-parameter for common-mode to common-mode port j to port i (see D.10)
S_{CDij}	S-parameter for differential to common-mode port j to port i (see D.10)
S_{DCij}	S-parameter for common-mode to differential port j to port i (see D.10)
S_{DDij}	S-parameter for differential to differential port j to port i (see D.10)
Δ (Delta)	difference operator
ϕ (phi)	phase

Symbols	Meaning
π (pi)	3.141 59... , the ratio of the circumference of a circle to its diameter
ρ (rho)	reflection coefficient (see 3.1.77)
τ (tau)	time constant
®	registered trademark

3.2.4 Mathematical operators

Mathematical operators used in this standard:

Mathematical Operators	Meaning
e	2.718 28..., the base of the natural (i.e., hyperbolic) system of logarithms
sgn	signum function (i.e., sign function)
$\wedge$	exclusive logical OR
$<$	less than
$\leq$	less than or equal to
$>$	greater than
$\geq$	greater than or equal to
$\pm$	plus or minus
$\times$	multiplication
$/$	division
$ v $	the absolute value (i.e., magnitude) of v
$\sim$	approximately equal to

3.3 Keywords

3.3.1

invalid

a keyword used to describe an illegal or unsupported bit, byte, word, field or code value; receipt of an invalid bit, byte, word, field or code value shall be reported as an error

3.3.2

mandatory

a keyword indicating an item that is required to be implemented as defined in this standard

3.3.3

may

a keyword that indicates flexibility of choice with no implied preference (equivalent to “may or may not”)

3.3.4

may not

keywords that indicate flexibility of choice with no implied preference (equivalent to “may or may not”)

3.3.5

obsolete

a keyword indicating that an item was defined in prior standards but has been removed from this standard

3.3.6

optional

a keyword that describes features that are not required to be implemented by this standard; however, if any optional feature defined in this standard is implemented, then it shall be implemented as defined in this standard

3.3.7

reserved

a keyword referring to bits, bytes, words, fields and code values that are set aside for future standardization; a reserved bit, byte, word or field shall be set to zero, or in accordance with a future extension to this standard; recipients are not required to check reserved bits, bytes, words or fields for zero values. Receipt of reserved code values in defined fields shall be reported as an error

3.3.8

restricted

a keyword referring to bits, bytes, words, and fields that are set aside for other identified standardization purposes; a restricted bit, byte, word, or field shall be treated as a reserved bit, byte, word or field in the context where the restricted designation appears

3.3.9

shall

a keyword indicating a mandatory requirement; designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard

3.3.10

should

a keyword indicating flexibility of choice with a strongly preferred alternative (equivalent to “is strongly recommended”)

3.3.11

vendor specific

something (e.g., a bit, field, or code value) that is not defined by this standard and may be used differently in various implementations

3.4 Editorial conventions

Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

Names of signals are in all uppercase (e.g., GROUND).

Normal case is used for words having the normal English meaning.

A binary number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 and 1 immediately followed by a lower-case b (e.g., 0101b). Underscores or spaces may be included between characters in binary number representations to increase readability or delineate field boundaries (e.g., 0 0101 1010b or 0_0101_1010b).

A hexadecimal number is represented in this standard by any sequence of digits consisting of only the Western-Arabic numerals 0 through 9 and/or the upper-case English letters A through F immediately followed by a lower-case h (e.g., FA23h). Underscores or spaces may be included between characters in hexadecimal number representations to increase readability or delineate field boundaries (e.g., B FD8C FA23h or B_FD8C_FA23h).

A decimal number is represented in this standard by any sequence of digits consisting of only the Arabic numerals 0 through 9 not immediately followed by a lower-case b or lower-case h (e.g., 25).

This standard uses the following conventions for representing decimal numbers:

- a) the decimal separator (i.e., separating the integer and fractional portions of the number) is a period;
- b) the thousands separator (i.e., separating groups of three digits in a portion of the number) is a space; and
- c) the thousands separator is used in both the integer portion and the fraction portion of a number.

Table 1 shows some examples of decimal numbers using various numbering conventions.

Table 1 — Numbering conventions

French	English	This standard
0,6	0.6	0.6
3,141 592 65	3.14159265	3.141 592 65
1 000	1,000	1 000
1 323 462,95	1,323,462.95	1 323 462.95

A decimal number represented in this standard with an overline over one or more digits following the decimal point is a number where the overlined digits are infinitely repeating (e.g., 666. $\overline{6}$ means 666.666 666... or 666 $\frac{2}{3}$, and 12.142 $\overline{857}$ means 12.142 857 142 857... or 12 $\frac{1}{7}$).

Lists sequenced by letters (e.g., a) red, b) blue, c) green) show no ordering relationship between the listed items. Lists sequenced by numbers (e.g., 1) red, 2) blue, 3) green) show an ordering relationship between the listed items.

In the event of conflicting information the precedence for requirements defined in this standard is:

- 1) text;
- 2) tables; and
- 3) figures.

Notes do not constitute any requirements for implementers.

4 General

4.1 Physical links and phys

A physical link is a set of four wires used as two differential signal pairs. One differential signal transmits in one direction while the other differential signal transmits in the opposite direction. Data may be transmitted in both directions simultaneously.

A physical phy contains a transceiver which electrically interfaces to a physical link, which attaches to another physical phy.

Phys are contained in ports (see SPL). Phys interface to a service delivery subsystem (see SAM-4).

Figure 3 shows two phys attached with a physical link.

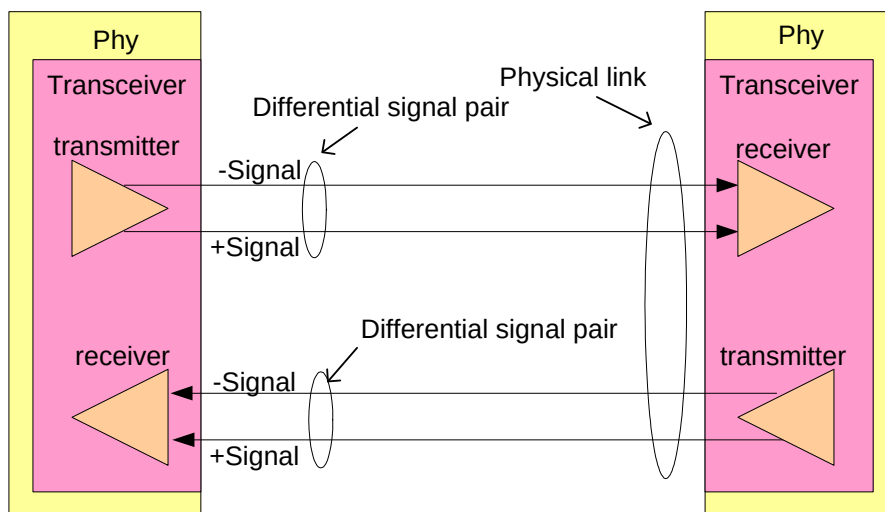


Figure 3 — Physical links and phys

An attached phy is the phy to which a phy is attached over a physical link.

The transceiver follows the electrical specifications defined in 5.7. Phys transmit and receive bits at physical link rates defined in 5.7. The bits are parts of 10-bit characters (see SPL), which are parts of dwords (see SPL). The physical link rates supported by a phy are specified or indicated by the following fields in the SMP DISCOVER response (see SPL), the SMP PHY CONTROL request (see SPL), and the Phy Control and Discover mode page (see SPL):

- a) the NEGOTIATED PHYSICAL LINK RATE field;
- b) the HARDWARE MINIMUM PHYSICAL LINK RATE field;
- c) the HARDWARE MAXIMUM PHYSICAL LINK RATE field;
- d) the PROGRAMMED MINIMUM PHYSICAL LINK RATE field; and
- e) the PROGRAMMED MAXIMUM PHYSICAL LINK RATE field.

4.2 Phy test functions

Phy test functions (e.g., transmission of test patterns) are used for phy and interconnect characterization and diagnosis. The phy may be attached to test equipment while performing a phy test function. See SPL for the optional mechanisms for invoking phy test function.

Each phy test function is optional.

If the phy test function requires a specific phy test pattern and/or phy test function physical link rate, then the mechanism for invoking the phy test function (see SPL) also specifies the phy test pattern and phy test function physical link rate.

5 Physical layer

5.1 Physical layer overview

The physical layer defines:

- a) passive interconnect (e.g., connectors and cable assemblies); and
- b) transmitter and receiver device electrical characteristics.

Within this standard, references to connector gender use the terms plug and receptacle as equivalent to the terms free and fixed, respectively, that may be used in the references that define the connectors. Fixed and free terminology has no relationship to the application of the connector.

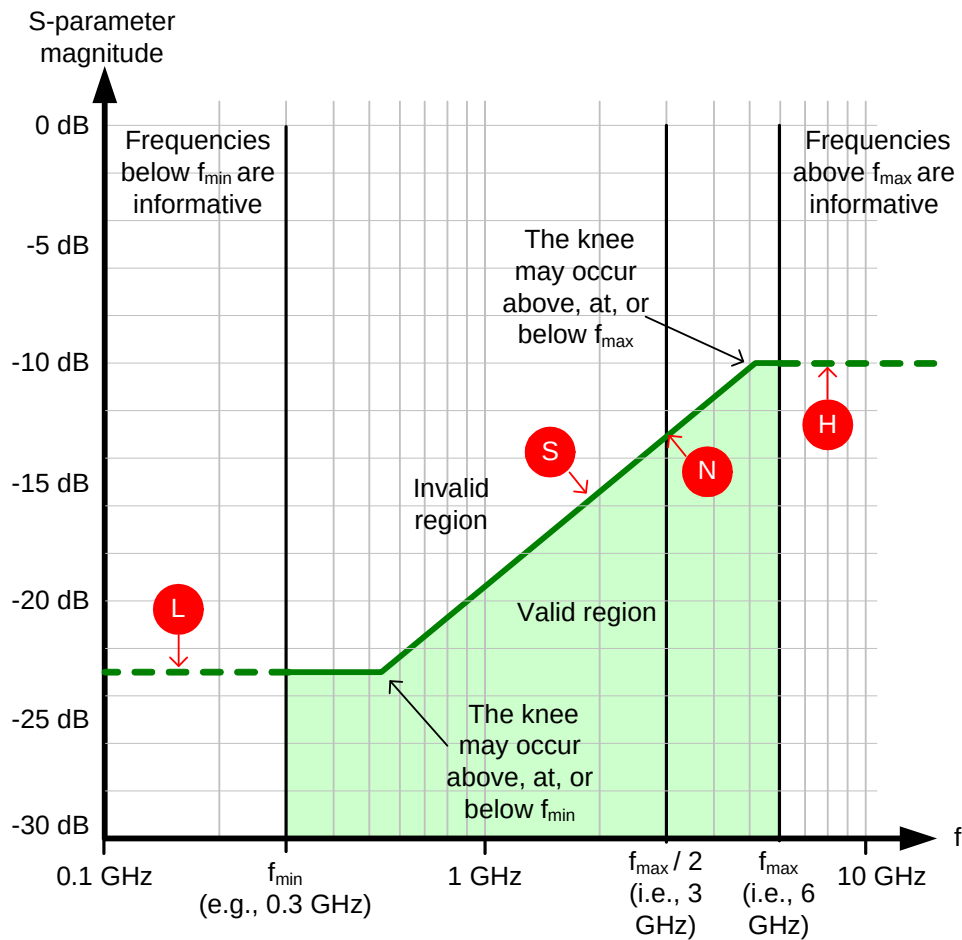
5.2 Conventions for defining maximum limits for S-parameters

The following values are specified by this standard to define the maximum limits for certain S-parameters (e.g., for cable assemblies and backplanes (see 5.5.3), transmitter devices (see 5.7.4.6.3), and receiver devices (see 5.7.5.7.2)):

- a) L is the maximum value in dB at the low frequency asymptote;
- b) N is the maximum value in dB at the Nyquist frequency (i.e., $f_{\max} / 2$) (e.g., 3 GHz for 6 Gbit/s);
- c) H is the maximum value in dB at the high frequency asymptote;
- d) S is the slope in dB/decade;
- e) $f_{\min}$ is the minimum frequency of interest; and
- f) $f_{\max}$ is the maximum frequency of interest.

The frequencies at which L and H intersect the slope S may or may not be within the region of $f_{\min}$ to $f_{\max}$.

Figure 4 shows the values in a graph.



Note: graph is not to scale

Figure 4 — Maximum limits for S-parameters definitions

5.3 Compliance points

A TxRx connection is the complete simplex signal path between the transmitter circuit and receiver circuit.

A TxRx connection segment is that portion of a TxRx connection delimited by separable connectors or changes in conductive material.

This standard defines the electrical requirements of the signal at the compliance points IT, IR, CT, and CR in a TxRx connection (see table 2). Each compliant phy shall be compatible with these electrical requirements to allow interoperability within a SAS environment.

Signal behavior at separable connectors requires compliance with signal characteristics defined by this standard only if the connectors are identified as compliance points by the supplier of the parts that contain the candidate compliance point.

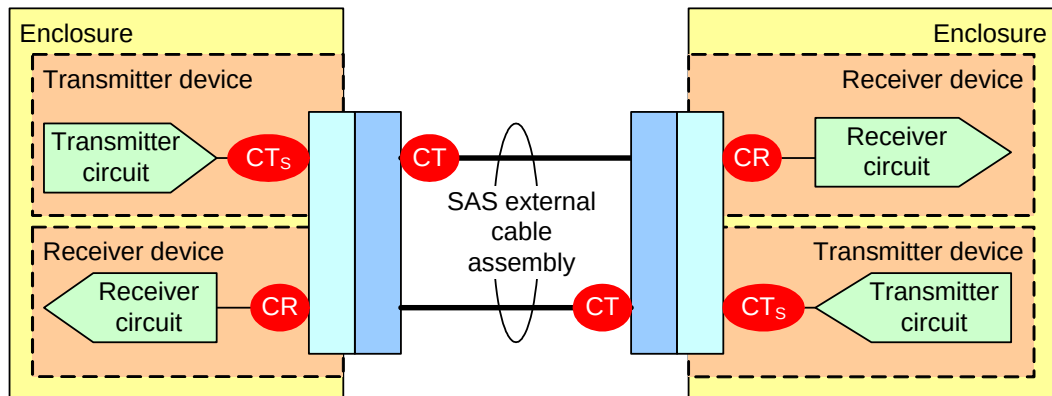
Signal characteristics for compliance points are measured at physical positions called probe points in a test load (see 5.6). Measurements at the probe points in a test load approximate measurements at the compliance point in the actual TxRx connection. Some components in the test load may be de-embedded as described in clause D.5.

Table 2 — Compliance points

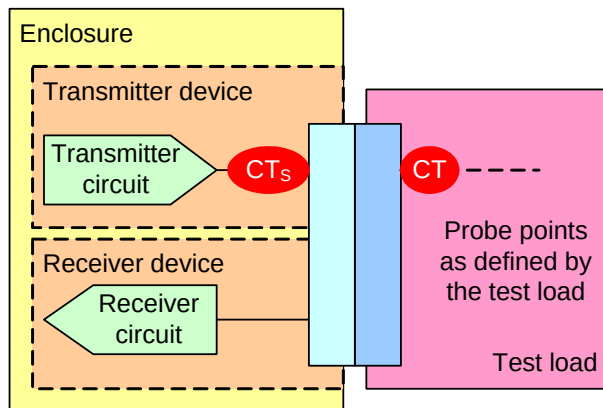
Compliance point	Type	Description
IT	intra-enclosure (i.e., internal)	The signal from a transmitter device, as measured at probe points in a test load attached with an internal connector.
IT _S ^a	intra-enclosure (i.e., internal)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the internal connector with a test load or a TxRx connection attached with an internal connector.
IR	intra-enclosure (i.e., internal)	The signal going to a receiver device, as measured at probe points in a test load attached with an internal connector.
CT	inter-enclosure (i.e., cabinet)	The signal from a transmitter device, as measured at probe points in a test load attached with an external connector.
CT _S ^a	inter-enclosure (i.e., cabinet)	The location of a transmitter device where S-parameters are measured and where the TxRx connection begins. This location is at the transmitter device side of the external connector with a test load or a TxRx connection attached with an external connector.
CR	inter-enclosure (i.e., cabinet)	The signal going to a receiver device, as measured at probe points in a test load attached with an external connector.
^a Because the trained 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s transmitter device S-parameter specifications do not include the mated connector, transmitter device S-parameter measurement points are at the IT _S compliance point and CT _S compliance point. 1.5 Gbit/s, 3 Gbit/s, and 6 Gbit/s receiver device S-parameter measurement points are at the IR compliance point and CR compliance point.		

The TxRx connection includes the characteristics of the mated connectors at both the transmitter device and receiver device ends. One end of a TxRx connection is a IT_S compliance point or CT_S compliance point, and the other end of the TxRx connection is the corresponding IR compliance point or CR compliance point.

Figure 5 shows the locations of the CT compliance points and CR compliance points using an external cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).



Testing the top-left CT:



Testing the top-right CR:

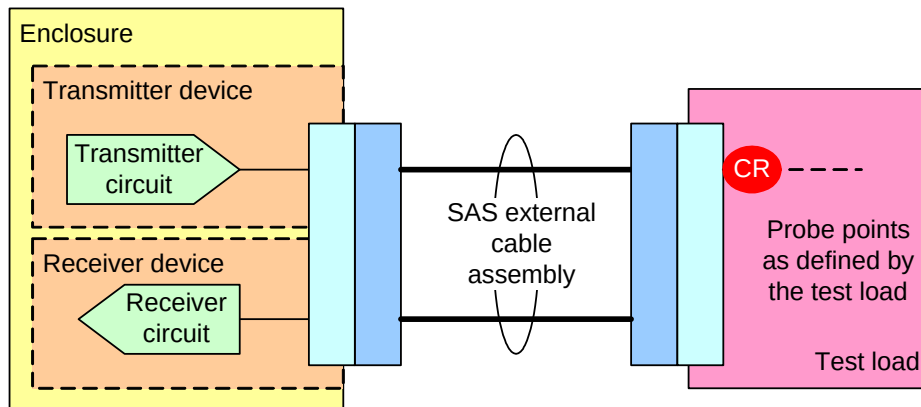


Figure 5 — External cable assembly CT compliance points and CR compliance points

Figure 6 shows the locations of the IT compliance points and IR compliance points using a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that is not using SATA, and shows how the compliance points are tested using test loads (see 5.6).

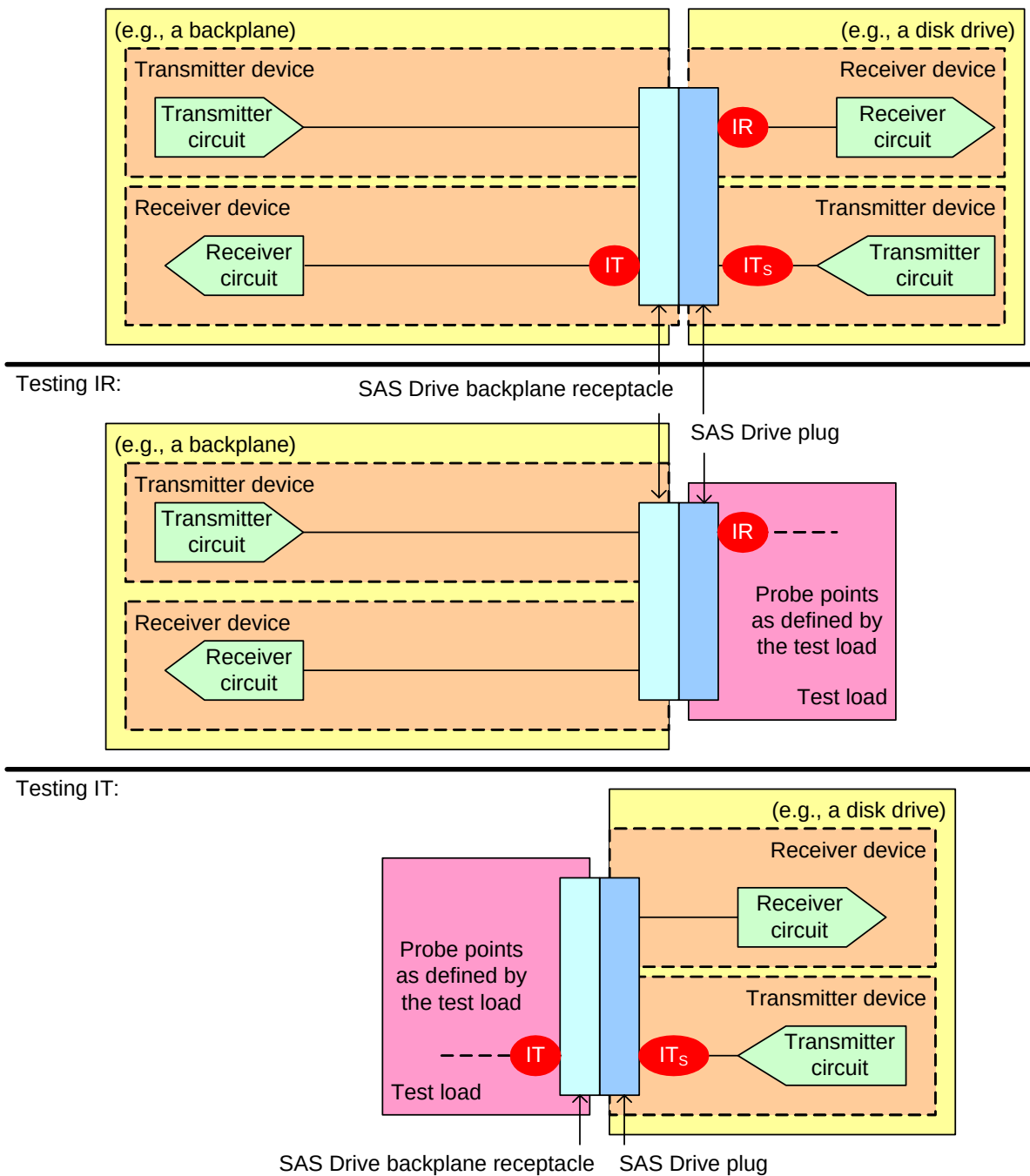


Figure 6 — Backplane with SAS Drive connector IT compliance points and IR compliance points

If the backplane supports SATA, then there are no IT compliance points or IR compliance points. SATA defines the signal characteristics that the SATA phy delivers and that the SAS backplane is required to deliver to the SATA device, as shown in figure 7.

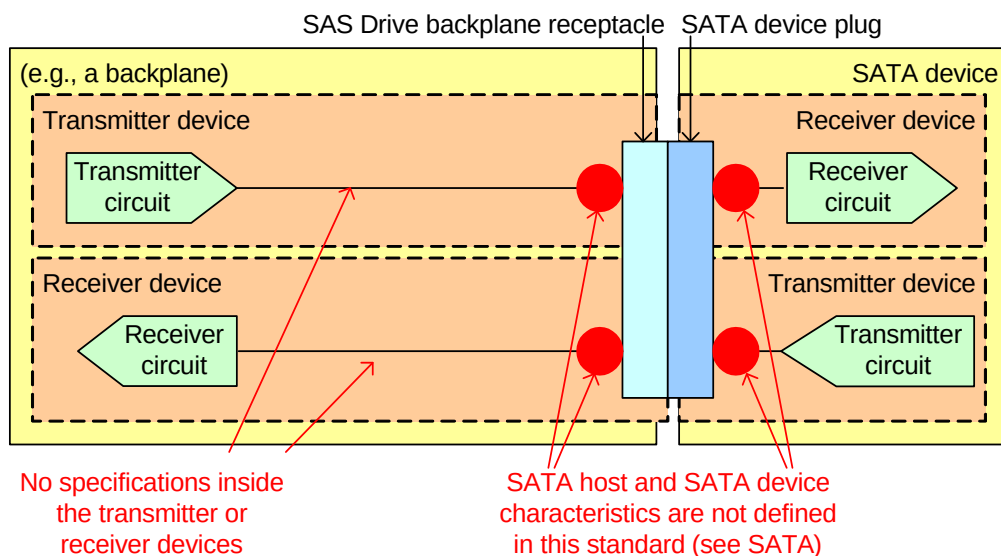


Figure 7 — Backplane with SAS Drive connector compliance points with SATA phy attached

Figure 8 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).

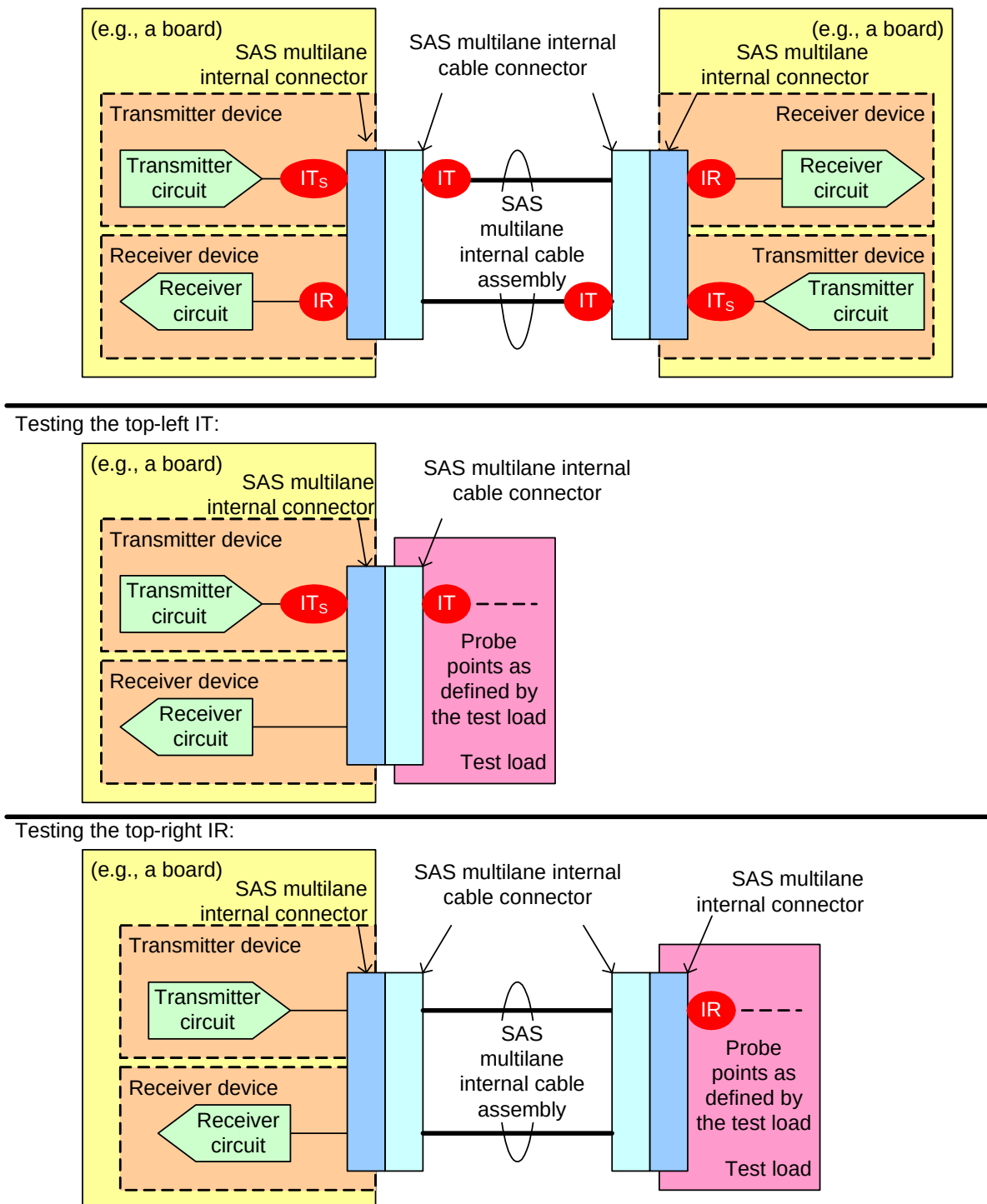


Figure 8 — SAS multilane internal cable assembly IT compliance points and IR compliance points

Figure 9 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3), where the backplane is not attached to a SATA device, and shows how two of the compliance points are tested using test loads (see 5.6).

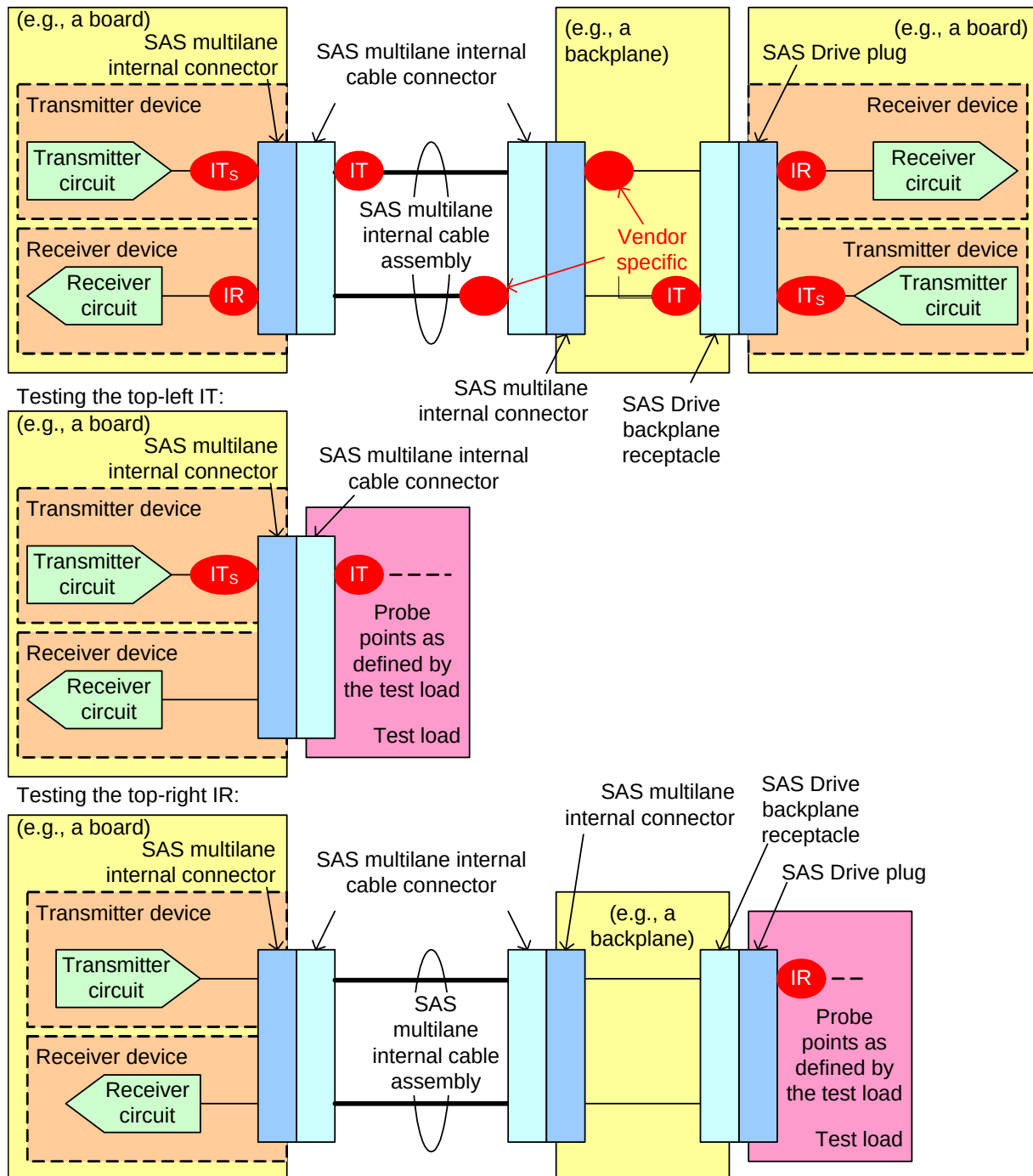


Figure 9 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points

Figure 10 shows the locations of the IT compliance points and IR compliance points using a SAS multilane internal cable assembly attached to a backplane with a SAS Drive backplane receptacle (see 5.4.3.3.1.3) that supports being attached to a SATA device. There are no IT compliance points and IR compliance points at the SAS Drive backplane receptacle connector when a SATA device is attached. In that case, SATA defines the signal characteristics that the SATA device delivers and that the SAS backplane is required to deliver to the SATA device. There are compliance points at the SAS multilane internal connector, however.

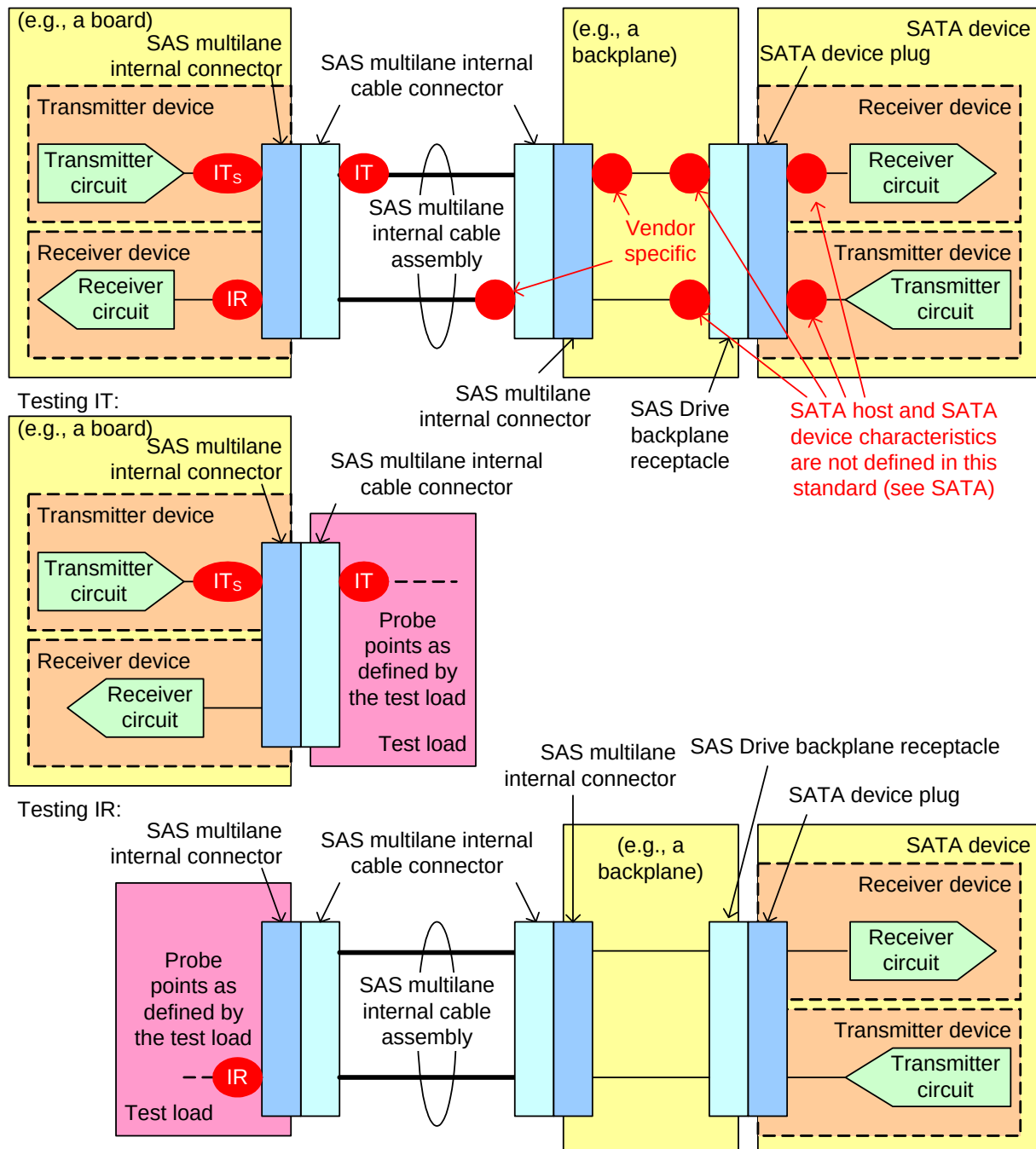
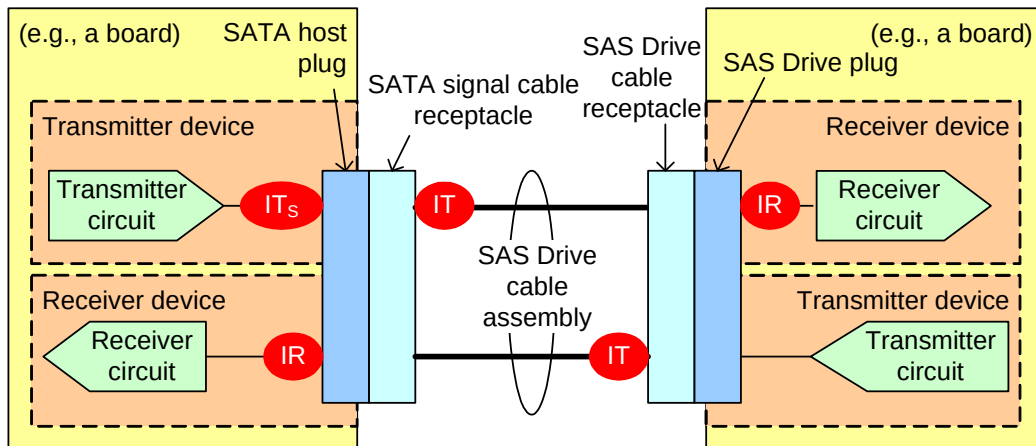
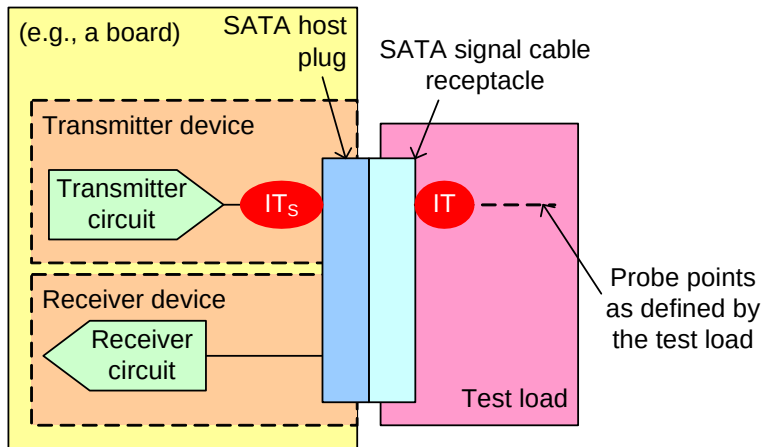


Figure 10 — SAS multilane internal cable assembly and backplane IT compliance points and IR compliance points with SATA device attached

Figure 11 shows the locations of the IT compliance points and IR compliance points using a SAS Drive cable assembly, and shows how two of the compliance points are tested using test loads (see 5.6).



Testing the top-left IT:



Testing the top-right IR:

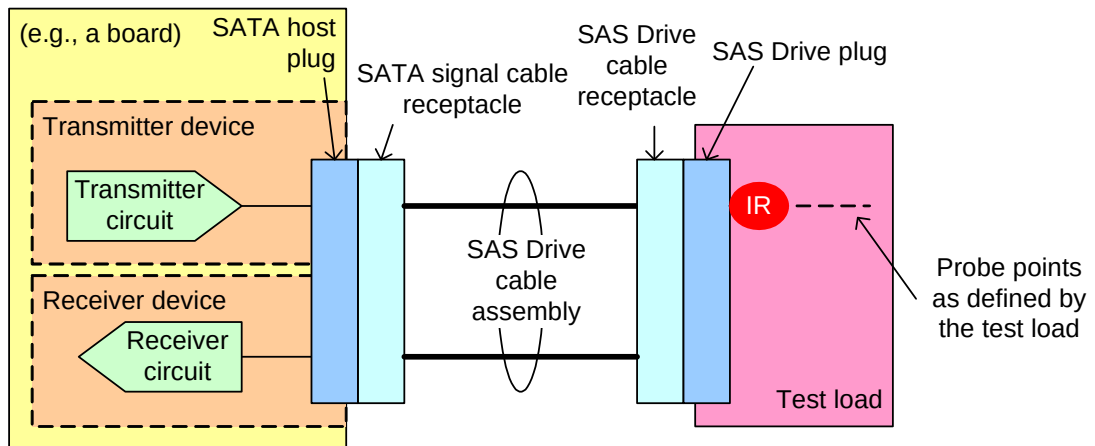


Figure 11 — SAS Drive cable assembly IT compliance points and IR compliance points

5.4 Interconnects

5.4.1 SATA connectors and cable assemblies

Figure 12 shows a representation of the connectors and cables defined by SATA. A SATA host is analogous to a SAS initiator device (see SPL) and a SATA device is analogous to a SAS target device (see SPL).

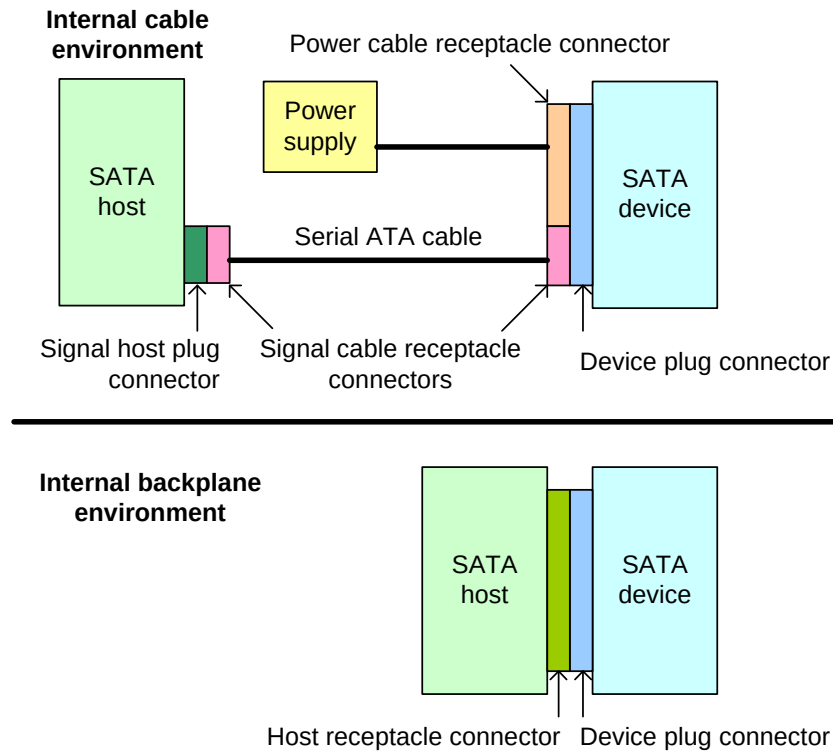


Figure 12 — SATA connectors and cables

5.4.2 SAS connectors and cables

This standard defines SAS Drive cable, SAS Drive backplane, SAS internal cable, and SAS external cable environments.

Figure 13 shows a representation of the SAS Drive cable environments.

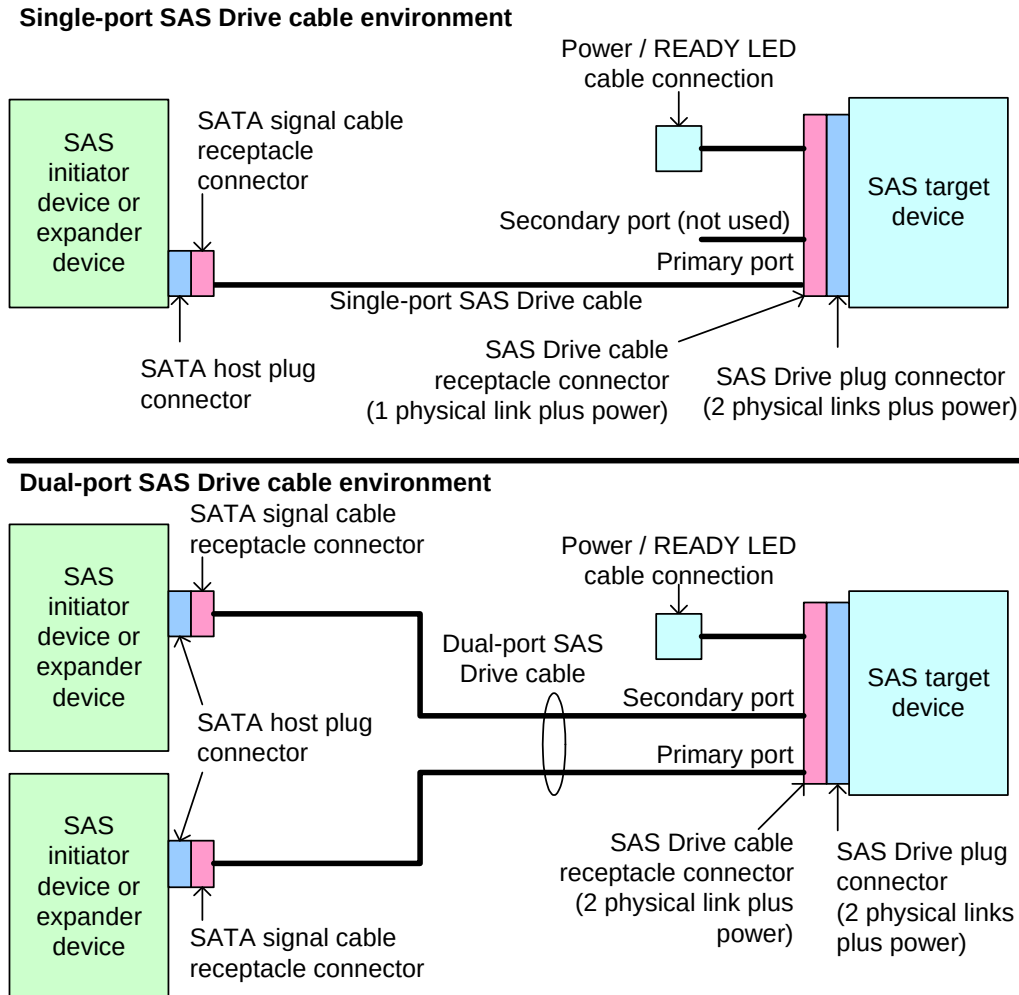


Figure 13 — SAS Drive cable environments

Figure 14 shows a representation of the SAS Drive backplane environment.

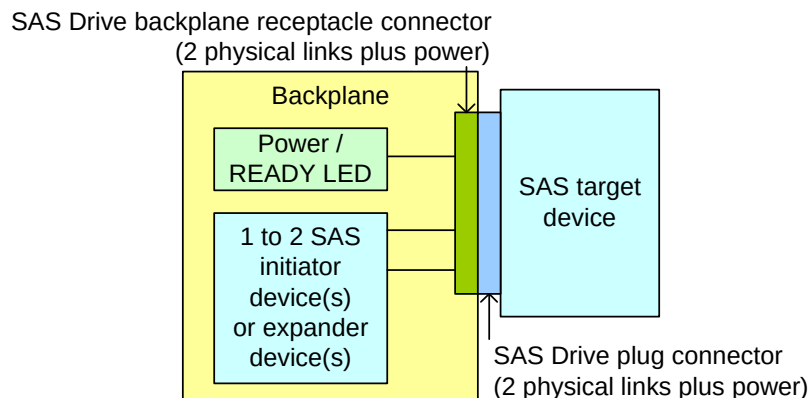


Figure 14 — SAS Drive backplane environment

Figure 15 shows a representation of the SAS external cable environment.

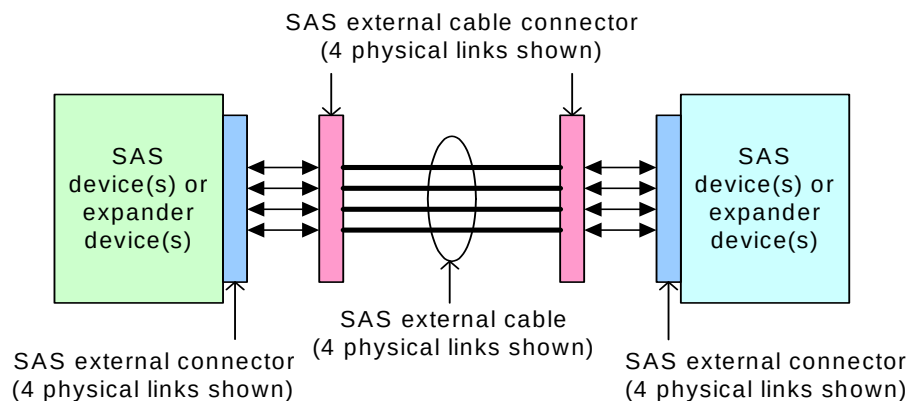


Figure 15 — SAS external cable environment

Figure 16 shows a representation of the SAS internal cable environment attaching a controller to a backplane using a SAS internal symmetric cable (see 5.4.4.1.2).

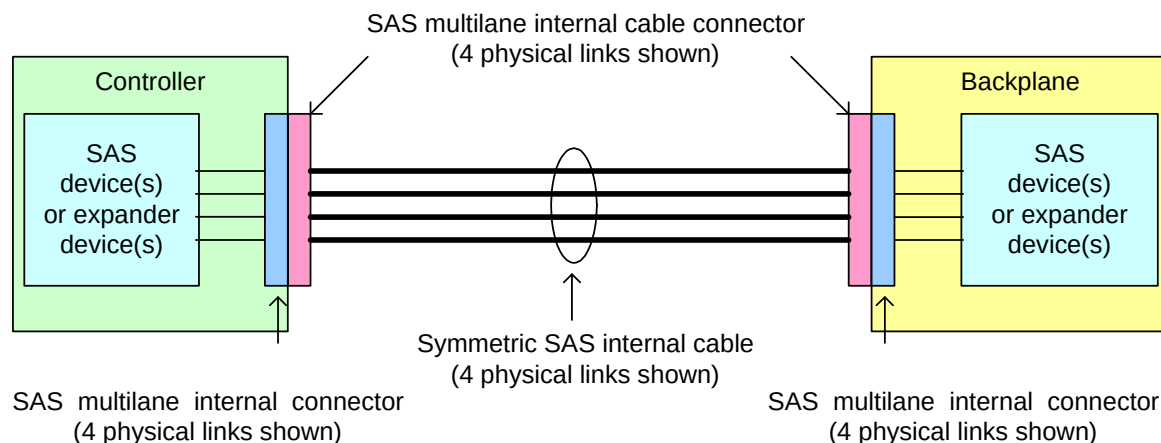


Figure 16 — SAS internal symmetric cable environment - controller to backplane

A SAS internal symmetric cable provides one to eight physical links, and may be used as any combination of wide links and narrow links (see SPL) using those physical links.

Figure 17 shows a representation of the SAS internal cable environment attaching a controller to a controller using a SAS internal symmetric cable (see 5.4.4.1.2). Two controllers may also be attached together with a SAS internal symmetric cable.

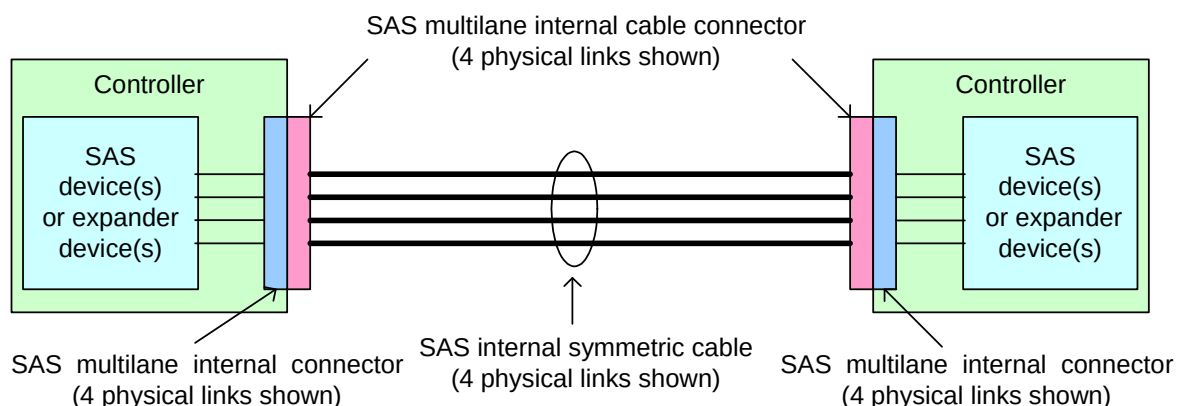


Figure 17 — SAS internal symmetric cable environment - controller to controller

Figure 18 shows a representation of the SAS internal cable environment using a SAS controller-based fanout cable (see 5.4.4.1.3).

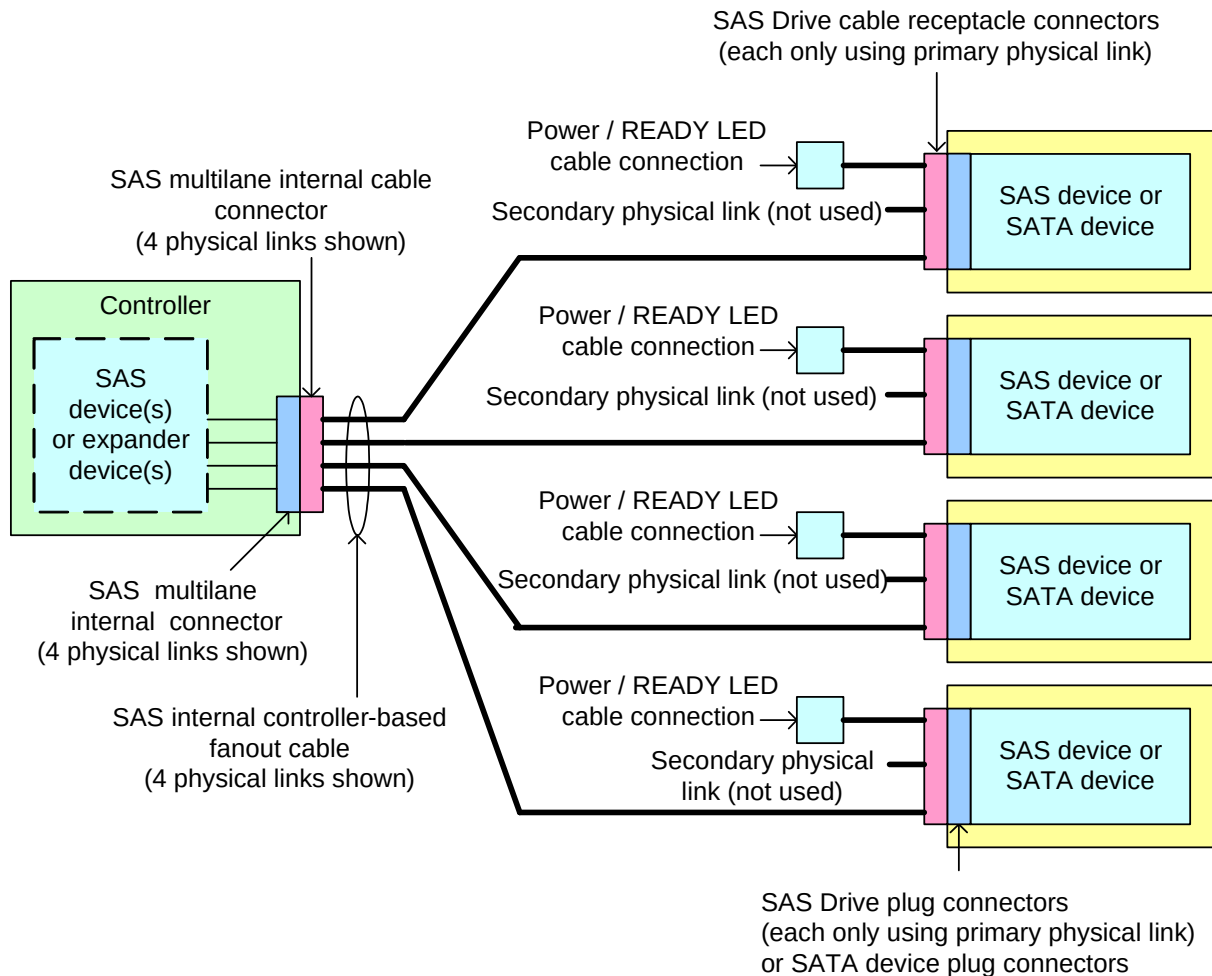


Figure 18 — SAS internal controller-based fanout cable environment

Figure 19 shows a representation of the SAS internal cable environment using a SAS backplane-based fanout cable (see 5.4.4.1.3).

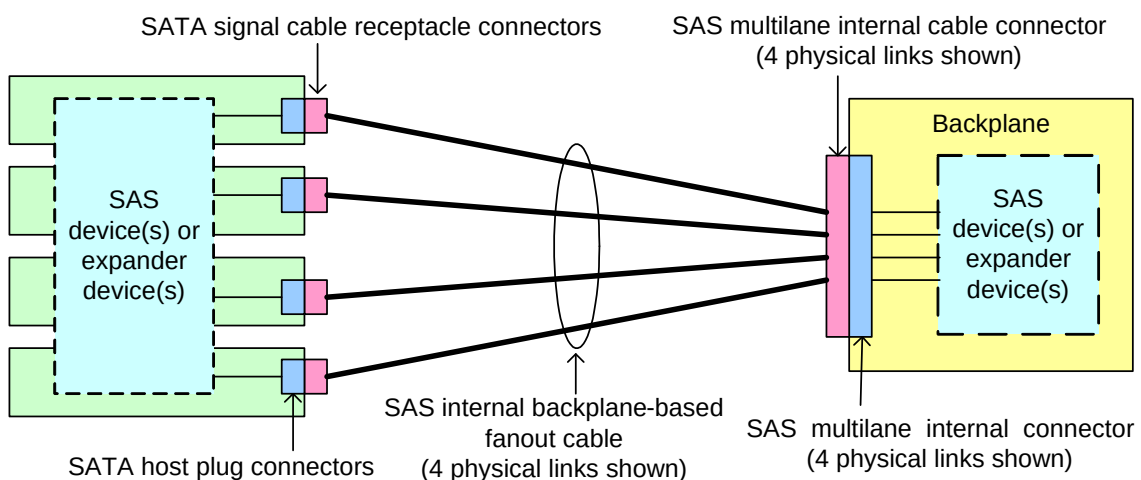


Figure 19 — SAS internal backplane-based fanout cable environment