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Edition 1.0 2009-11

INTERNATIONAL STANDARD

**Information technology – AT attachment with packet interface-7 –
Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)**



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INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

FOREWORD

- 1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards. Their preparation is entrusted to technical committees; any ISO and IEC member body interested in the subject dealt with may participate in this preparatory work. International governmental and non-governmental organizations liaising with ISO and IEC also participate in this preparation.
- 2) In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.
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International Standard ISO/IEC 24739-2 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

ISO/IEC 24739-2 is to be used in conjunction with ISO/IEC 24739-1 and ISO/IEC 24739-3.

The list of all currently available parts of the ISO/IEC 24739 series, under the general title *Information technology – AT attachment with packet interface-7*, can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

INTRODUCTION

The ISO/IEC 24739 series specifies the AT attachment interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers and suppliers of intelligent storage devices.

Part 1 defines the register delivered commands used by devices implementing the standard. Part 2 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the parallel interface. Part 3 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals and the protocols for the transporting of commands, data and status over the interface for the serial interface. Figure 1 shows the relationship of these documents. For devices implementing the PACKET command feature set, additional command layer standards are listed in Table 1 and described in Clause 2.

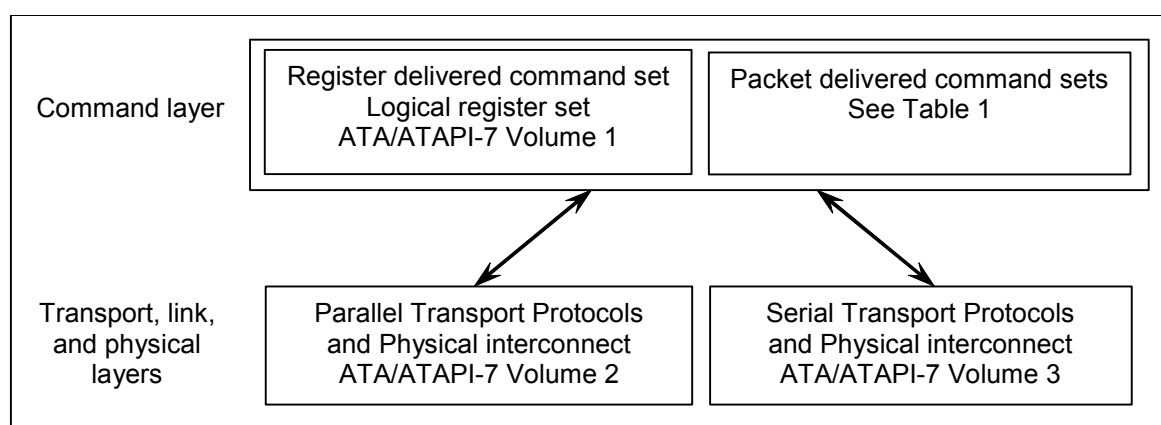


Figure 1 – ATA document relationships

Table 1 – PACKET delivered command sets

Standard
SCSI Primary Commands (SPC)
SCSI Primary Commands-2 (SPC-2)
SCSI Primary Commands-3 (SPC-3)
SCSI Block Commands (SBC-2)
SCSI Stream Commands (SSC)
Multimedia Commands (MMC)
Multimedia Commands-2 (MMC-2)
Multimedia Commands-3 (MMC-3)
Multimedia Commands-4 (MMC-4)
ATAPI for Removable Media (SFF8070I)
ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

This standard maintains compatibility with the AT Attachment with Packet Interface-6 standard (ATA/ATAPI-6) and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 2: Parallel transport protocols and physical interconnect (ATA/ATAPI-7)

1 Scope

This part of ISO/IEC 24739 specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers and suppliers of intelligent storage devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document, including any amendments, applies.

The provisions of the referenced specifications other than ISO/IEC, IEC, ISO and ITU documents, as identified in this clause, are valid within the context of this International Standard. The reference to such a specification within this International Standard does not give it any further status within ISO/IEC. In particular, it does not give the referenced specification the status of an International Standard.

ISO/IEC 14776-362, *Information technology – Small Computer System Interface (SCSI) – Part 362: Multimedia commands-2 (MMC-2)* [ANSI INCITS 333-2000]

PC Card Standard, February 1995, PCMCIA ¹

CompactFlash™ Association Specification, Revision 1.4²

3 Terms, definitions, abbreviations, conventions and keywords

3.1 Terms, definitions and abbreviations

For the purposes of this International Standard, the following definitions as well as the definitions of ISO/IEC 24739-1 and ISO/IEC 24739-3, as soon as they are available, apply.

NOTE ISO/IEC 24739-1 and ISO/IEC 24739-3 are currently in preparation (see also 3.4).

3.1.1

ASCII character

designates a 8-bit value that is encoded using the ASCII character set

¹ For the PC Card Standard published by the Personal Computer Memory Card International Association, contact PCMCIA at 408-433-2273 or <http://www.pcmcia.org>.

² For the Compact Flash Association Specification published by the Compact Flash Association, contact the Compact Flash Association at <http://www.compactflash.org>.

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3.1.2**acoustics**

measurement of airborne noise emitted by information technology and telecommunications equipment

[ISO 7779:1999]

3.1.3**ATA****AT attachment**

ATA defines the physical, electrical, transport and command protocols for the internal attachment of storage devices to host systems

3.1.4**ATA-1 device**

device that complied with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives

NOTE ANSI X3.221-1994 has been withdrawn.³

3.1.5**ATA-2 device**

device that complied with ANSI X3.279-1996, the AT Attachment Interface with Extensions

NOTE ANSI X3.279-1996 has been withdrawn.³

3.1.6**ATA-3 device**

device that complies with ANSI INCITS 298-1997, the AT Attachment-3 Interface

NOTE ANSI INCITS 298-1997 has been withdrawn.³

3.1.7**ATA/ATAPI-4 device**

device that complies with ANSI INCITS 317-1998, AT Attachment Interface with Packet Interface Extensions-4

3.1.8**ATA/ATAPI-5 device**

device that complies with ANSI INCITS 340-2000, the AT Attachment with Packet Interface-5

3.1.9**ATA/ATAPI-6 device**

device that complies with ANSI INCITS 361-2002, the AT Attachment with Packet Interface-6

3.1.10**ATA/ATAPI-7 device**

device that complies with this series of International Standards

3.1.11**ATAPI device****AT attachment packet interface device**

device implementing the packet command feature set

³ For further information contact ANSI <http://www.ansi.org/>.

3.1.12

allocation unit

AU

the minimum number of logically contiguous sectors on the media as used in the streaming feature set

NOTE An Allocation Unit may be accessed with one or more request.

3.1.13

audio-video

AV

audio-video applications use data that is related to video images and/or audio; the distinguishing characteristic of this type of data is that accuracy is of lower priority than timely transfer of the data

3.1.14

backchannel

when transmitting a FIS, the backchannel is the receive channel

3.1.15

bit error rate

BER

statistical probability of a transmitted encoded bit being erroneously received in a communication system

3.1.16

bus release

for devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed; this allows the host to select the other device or deliver another queued command

3.1.17

byte count

value placed in the byte count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command

3.1.18

byte count limit

value placed in the byte count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion

3.1.19

CompactFlash™ Association

CFA

association which created the specification for compact flash memory that uses the ATA interface

3.1.20

check condition

for devices implementing the PACKET command feature set, this indicates an error or exception condition has occurred

3.1.21

cylinder-head-sector

CHS

obsolete method of addressing the data on the device by cylinder number, head number and sector number

3.1.22**code violation**

in a serial interface implementation, a code violation is an error that occurs in the decoding of an encoded character

[see ISO/IEC 24739-3, Clause 15]

3.1.23**command aborted**

command completion with ABRT set to one in the error register and ERR set to one in the status register

3.1.24**command acceptance**

a command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the status register and the host writes to the command register

NOTE An exception exists for the DEVICE RESET command (see ISO/IEC 24739-1:2008, Clause 6). In a serial implementation, command acceptance is a positive acknowledgment of a host to device register FIS.

3.1.25**command block registers**

interface registers used for delivering commands to the device or posting status from the device

NOTE In a serial implementation, the command block registers are FIS payload fields.

3.1.26**command completion**

completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the error register, the placing of the appropriate status bits in the status register, the clearing of both BSY and DRQ to zero and Interrupt Pending

3.1.27**command packet**

data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters

3.1.28**command released**

when a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion

3.1.29**control block registers**

in a parallel implementation, interface registers used for device control and to post alternate status; in a serial interface implementation, the logical field of a FIS corresponding to the device register bits of a parallel implementation

3.1.30**control character**

in a serial interface implementation, an encoded character that represents a non-data byte

[see ISO/IEC 24739-3:2008, Clause 15]

3.1.31

cyclical redundancy check

CRC

means used to check the validity of certain data transfers

3.1.32

cylinder high register

name used for the LBA high register in previous ATA/ATAPI standards

3.1.33

cylinder low register

name used for the LBA mid register in previous ATA/ATAPI standards

3.1.34

data character

in a serial interface implementation, an encoded character that represents a data byte (see ISO/IEC 24739-3, Clause 15)

3.1.35

data-in

protocol that moves data from the device to the host

NOTE These transfers are initiated by READ commands.

3.1.36

data-out

protocol that moves data from the host to the device

NOTE These transfers are initiated by WRITE commands.

3.1.37

delayed LBA

any sector for which the performance specified by the streaming performance parameters log is not valid

3.1.38

device

storage peripheral

traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard

3.1.39

device selection

in a parallel implementation, a device is selected when the DEV bit of the device register is equal to the device number assigned to the device by means of a device 0/device 1 jumper or switch, or use of the CSEL signal

NOTE In a serial implementation the device ignores the DEV bit, the host adapter may use this bit to emulate device selection.

3.1.40

disparity

difference between the number of ones and the number of zeroes in an encoded character

[see ISO/IEC 24739-3, Clause 15]

3.1.41

DMA data transfer

direct memory access data transfer

means of data transfer between device and host memory without host processor intervention

3.1.42**don't care**

term to indicate that a value is irrelevant for the particular function described

3.1.43**driver**

active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus

3.1.44**DRQ data block**

unit of data words transferred during a single assertion of DRQ when using PIO data transfer

3.1.45**elasticity buffer**

in a serial interface implementation, a portion of the receiver where character slipping and/or character alignment is performed

3.1.46**encoded character**

in a serial interface implementation, the output of the 8b/10b encoder

[see ISO/IEC 24739-3, Clause 0]

3.1.47**first party DMA access**

method by which a device accesses host memory

NOTE First party DMA differs from DMA in that the device sends a DMA setup FIS to select host memory regions; whereas for DMA the host configures the DMA controller.

3.1.48**frame information structure****FIS**

data structure; it is the payload of a frame and does not include the SOF primitive, CRC and EOF primitive

3.1.49**frame**

unit of information exchanged between the host adapter and a device

NOTE A frame consists of an SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS and an EOF primitive.

3.1.50**forced unit access****FUA**

requires that user data be transferred to or from the device media before command completion even if caching is enabled

3.1.51**Gen1 DWORD time**

the time it takes to transmit a 40 bit encoded value at 1.5 Gbit/s

3.1.52**host**

computer system executing the software BIOS and/or operating system device driver controlling the device and the adapter hardware for the ATA interface to the device

3.1.53

host adapter

implementation of the host transport, link and physical layers

3.1.54

interrupt pending

in a parallel implementation, an internal state of a device;

in this state, the device asserts INTRQ if nIEN is cleared to zero and the device is selected [see Clause 8];

in a serial implementation, the Interrupt Pending state is an internal state of the host adapter; this state is entered by reception of a FIS with the I field set to one

[see ISO/IEC 24739-3, Clause 16]

3.1.55

logical block address

LBA

addressing of data on the device by the linear mapping of sectors

3.1.56

linear feedback shift register

LFSR

[see ISO/IEC 24739-3, Clause 0]

3.1.57

link

the link layer manages the phy layer to achieve the delivery and reception of frames (see ISO/IEC 24739-3, Clause 15)

3.1.58

logical sector

a uniquely addressable set of 256 words (512 bytes)

3.1.59

native max address

the highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command

3.1.60

overlap

a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device (if present) on the bus

3.1.61

packet delivered command

command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters. See also register delivered command

3.1.62

PHY

physical layer electronics

[see ISO/IEC 24739-3, Clause 14]

3.1.63**physical sector**

group of contiguous logical sectors that are read from or written to the device media in a single operation

3.1.64**programmed input/output data transfer****PIO data transfer**

PIO data transfers are performed by the host processor utilizing accesses to the data register

3.1.65**primitive**

in a serial interface implementation, a single DWORD of information that consists of a control character in byte 0 followed by three additional data characters in byte 1 through 3

3.1.66**queued**

command queuing allows the host to issue concurrent commands to the same device

NOTE Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred, but command completion has not occurred.

3.1.67**read command**

command that causes the device to transfer data from the device to the host (e.g., READ SECTOR(S), READ DMA, etc.)

3.1.68**register**

register may be a physical hardware register or a logical field

3.1.69**register delivered command**

command that is delivered to the device by placing the command and all of the parameters for the command in the device command block registers

NOTE See also packet delivered command.

3.1.70**register transfers**

host reading and writing any device register except the data register; register transfers are 8 bits wide

3.1.71**released**

in a parallel interface implementation, indicates that a signal is not being driven

NOTE For drivers capable of assuming a high-impedance state, this means that the driver is in the high-impedance state. For open-collector drivers, the driver is not asserted.

3.1.72**sector**

uniquely addressable set of 256 words (512 bytes)

3.1.73**sector number register**

LBA low register in previous ATA/ATAPI standards

3.1.74

shadow command block

in a serial interface implementation, a set of virtual fields in the host adapter that map the command block registers defined at the command layer to the fields within the FIS content

3.1.75

shadow control block

in a serial interface implementation, a set of virtual fields in the host adapter that map the control block registers defined at the command layer to the fields within the FIS content

3.1.76

signature

unique set of values placed in the command block registers by the device to allow the host to distinguish devices implementing the PACKET command feature set from those devices not implementing the PACKET command feature set

3.1.77

self-monitoring, analysis and reporting technology

SMART

for prediction of device degradation and/or faults

3.1.78

transport

transport layer manages the lower layers (link and phy) as well as constructing and parsing FISs

[see ISO/IEC 24739-3, Clause 16]

3.1.79

ultra DMA burst

the period from an assertion of DMACK[–] to the subsequent negation of DMACK[–] when an ultra DMA transfer mode has been enabled by the host

3.1.80

unaligned write

write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector

3.1.81

unit attention condition

state that a device implementing the PACKET command feature set maintains while the device has asynchronous status information to report to the host

3.1.82

unrecoverable error

when the device sets either the ERR bit or the DF bit to one in the status register at command completion

3.1.83

vendor specific

VS

bits, bytes, fields and code values that are reserved for vendor specific purposes

NOTE 1 These bits, bytes, fields and code values are not described in this standard and they may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE 2 Industry practice could result in conversion of a Vendor Specific bit, byte, field or code value into a defined standard value in a future standard.

3.1.84**write command**

command that causes the device to transfer data from the host to the device (e.g., WRITE SECTOR(S), WRITE DMA, etc.)

3.1.85**world wide name****WWN**

64-bit worldwide unique name based upon a company's IEEE identifier

[see IDENTIFY DEVICE Words (111:108) in ISO/IEC 24739-1, Clause 6.]

3.2 Abbreviations

ATA	AT Attachment
ATAPI	AT Attachment Packet Interface
AU	Allocation Unit
AV	Audio-Video
AWG	American Wire Gauge
BER	Bit Error Rate
CD	Card Detect
CFA	CompactFlash™ Association
CHS	Cylinder-Head-Sector
CRC	Cyclical Redundancy Check
CS	Device Chips Select
CSEL	Cable Select
DC	Direct Current
DD	Device Data
DDIAG	Device Diagnostic
DIOW	Device Input Output Write
DMA	Direct Memory Access
DMACK	DMA Knowledge
DMARQ	DMA Request
EVN	Even
FIS	Frame Information Structure
FUA	Forced Unit Access
IOWR	Input Output Read Write
LBA	Logical Block Address
LFSR	Linear Feedback Shift Register
OC	Open Collector
ODD	Odd
PC	Personal Computer
PCB	Printed Circuit Board
PD	Pull-down
PHY	Physical Layer Electronics
PIO	Programmed Input/Output data transfer
PU	Pull-Up

SMART	Self-Monitoring, Analysis And Reporting Technology
TP	Totem-Pole
TS	Tri-State
WWN	World Wide Name
VS	Vendor Specific

3.3 Conventions

3.3.1 General

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.3.7 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., LBA Mid register).

The expression "word n" or "bit n" shall be interpreted as indicating the content of word n or bit n.

3.3.2 Precedence

If there is a conflict between text, figures and tables, the precedence shall be tables, figures, then text.

3.3.3 Lists

Ordered lists, those lists describing a sequence, are of the form:

- a)
- b)
- c)

Unordered list are of the form:

- 1)
- 2)
- 3)

3.3.4 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

3.3.4.1 expected

Keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.3.4.2 mandatory

Keyword indicating items to be implemented as defined by this standard.

3.3.4.3 may

Keyword that indicates flexibility of choice with no implied preference.

3.3.4.4 obsolete

Keyword indicating that the designated bits, bytes, words, fields and code values that may have been defined in previous standards are not defined in this standard and shall not be reclaimed for other uses in future standards. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility.

Obsolete commands should not be used by the host. Commands defined as obsolete may be command aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

3.3.4.5 optional

Keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

3.3.4.6 prohibited

Keyword indicating that an item shall not be implemented by an implementation.

3.3.4.7 reserved

Keyword indicating reserved bits, bytes, words, fields and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted.

3.3.4.8 retired

Keyword indicating that the designated bits, bytes, words, fields and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, words, fields or code values are used before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

3.3.4.9 shall

Keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

3.3.4.10 should

Keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

3.3.5 Numbering

Numbers that are not immediately followed by a lowercase “b” or “h” are decimal values. Numbers that are immediately followed by a lowercase “b” (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase “h” (e.g., 3Ah) are hexadecimal values.

3.3.6 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates the signal is a low active signal. A low active signal is true when the signal is below V_{iL} and is false when the signal is above V_{iH} . No dash at the end of a signal name indicates the signal is a high active signal. A high active signal is true when the signal is above V_{iH} and is false when the signal is below V_{iL} .

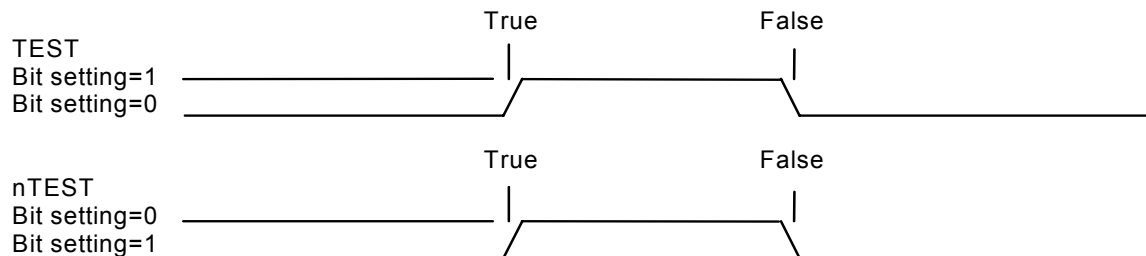
“Asserted” means that the signal is driven by an active circuit to the true state. “Negated” means that the signal is driven by an active circuit to the false state. “Released” means that the signal is not actively driven to any state (see Clause 7). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive function are identified with their function names separated by a colon (e.g., DIOW-:STOP).

SIGNAL(n:m) denotes a set of signals, for example, DD(15:0).

3.3.7 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero, the meaning of the bit is true and when nBIT is set to one, the meaning of the bit is false.



Bit (n:m) denotes a set of bits, for example, bits (7:0).

3.3.8 State diagram conventions

State diagrams shall be as shown in Figure 2.

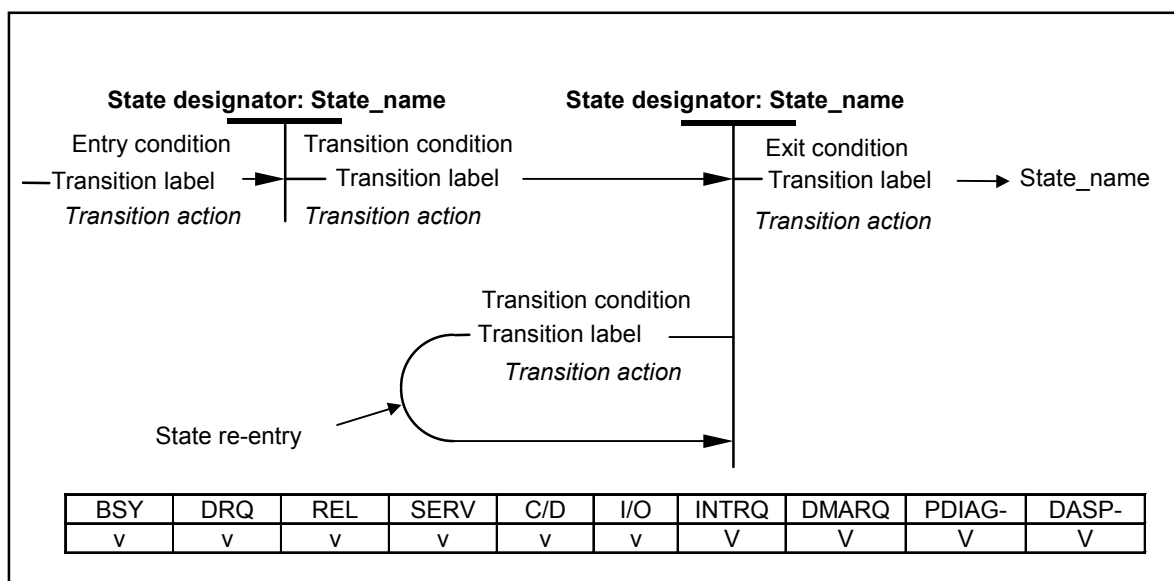


Figure 2 – State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

In device command protocol state diagrams, the state of bits and signals that change state during the execution of this state diagram are shown under the state designator:state_name and a table is included that shows the state of all bits and signals throughout the state diagram as follows:

- v = bit value changes.
- 1 = bit set to one.
- 0 = bit cleared to zero.
- x = bit is don't care.
- V = signal changes.
- A = signal is asserted.
- N = signal is negated.
- R = signal is released.
- X = signal is don't care.

Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made, followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled xx. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

Transitions from state to state shall be instantaneous.

3.3.9 Timing conventions

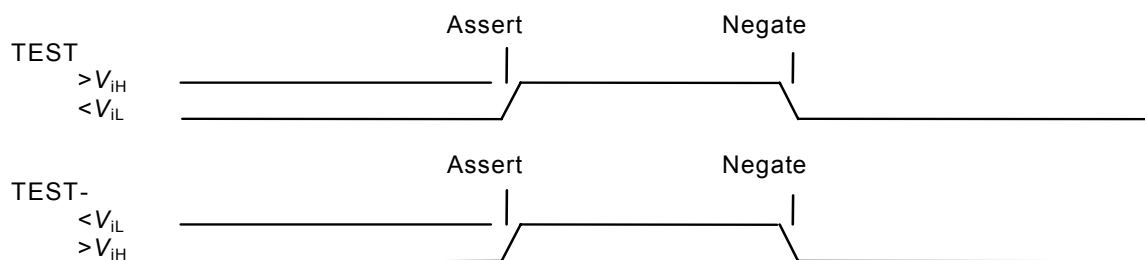
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.

$\diagup$ or $\diagdown$	- signal transition (asserted or negated)
$\langle$ or $\rangle$	- data transition (asserted or negated)
	- data valid
	- undefined but not necessarily released
	- asserted, negated or released
.....	- released
-----	- the "other" condition if a signal is shown with no change

All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



3.3.10 Byte ordering for data transfers

Data is transferred in blocks using either PIO or DMA protocols. PIO data transfers occur when the BSY bit is cleared to zero and the DRQ bit is set to one. These transfers are usually 16-bit but CFA devices may implement 8-bit PIO transfers. Data is transferred in blocks of one or more bytes known as a DRQ block. DMA data transfers occur when the host asserts DMACK- in response to the device asserting DMARQ. DMA transfers are always 16-bit. Each assertion of DMACK- by the host defines a DMA data burst. A DMA data burst is two or more bytes.

Assuming a DRQ block or a DMA burst of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block and Byte(n-1) is the last byte of the block. Table 2 shows the order the bytes shall be presented in when such a block of data is transferred on the interface using 16-bit PIO and DMA transfers. Table 3 shows the order the bytes shall be presented in when such a block or burst of data is transferred on the interface using 8-bit PIO.

Table 2 – Byte order

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

Table 3 – Byte order

	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (0)							
Second transfer	Byte (1)							
.....								
Last transfer	Byte (n-1)							

NOTE The above description is for data on the interface. Host systems and/or host adapters may cause the order of data as seen in the memory of the host to be different.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only code values 20h through 7Eh. For the string "Copyright", the character "C" is the first byte, the character "o" is the second byte, etc. When these fields are transferred, the order of transmission is:

the 1st character ("C") is on DD(15:8) of the first word,
the 2nd character ("o") is on DD(7:0) of the first word,
the 3rd character ("p") is on DD(15:8) of the second word,
the 4th character ("y") is on DD(7:0) of the second word,
the 5th character ("r") is on DD(15:8) of the third word,
the 6th character ("i") is on DD(7:0) of the third word,
the 7th character ("g") is on DD(15:8) of the fourth word,
the 8th character ("h") is on DD(7:0) of the fourth word,
the 9th character ("t") is on DD(15:8) of the fifth word,
the 10th character ("space") is on DD(7:0) of the fifth word,
etc.

Word (n:m) denotes a set of words, for example, words (103:100).

3.3.11 Byte, word and DWORD relationships

Figure 3 illustrates the relationship between bytes, words and DWORDs for serial interface implementations.

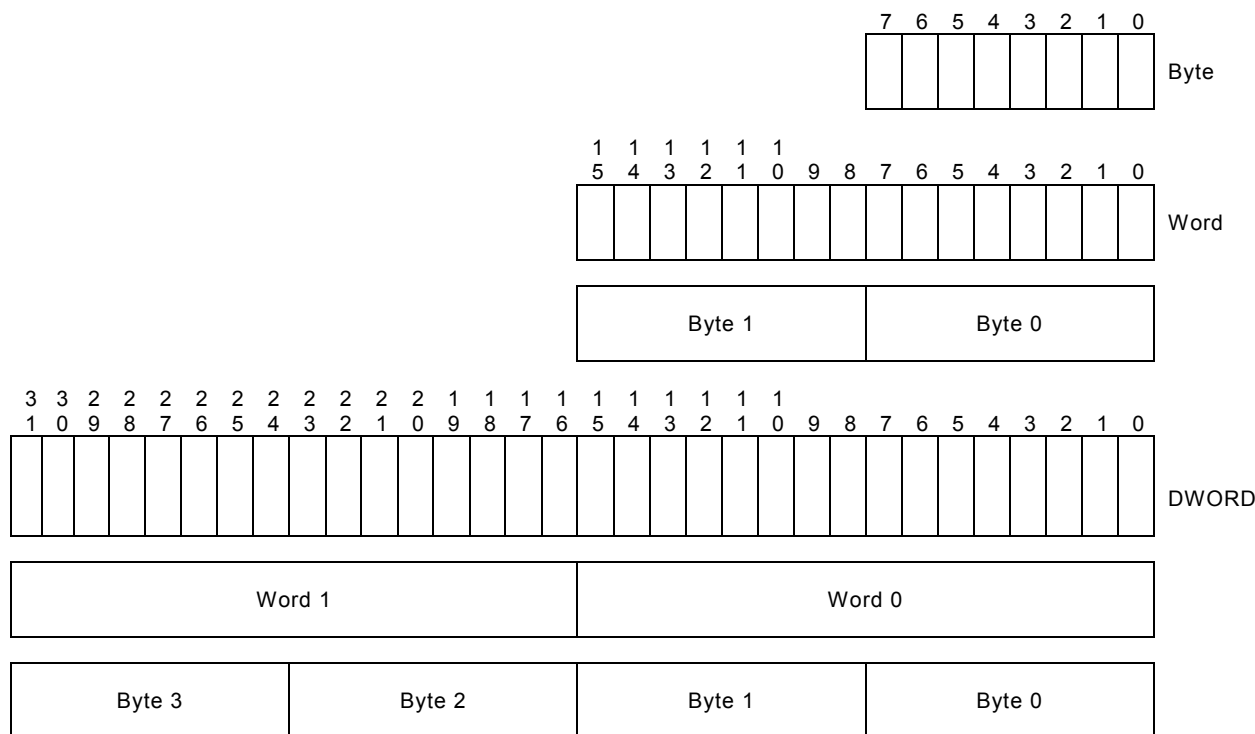


Figure 3 – Byte, word and DWORD relationships

3.4 Relationship of this part of ISO/IEC 24739 to ISO/IEC 24739-1 and ISO/IEC 24739-3

Originally, the three parts formed a single specification. For the convenience of the user, it was decided that this large specification will be published in three parts. However, to comply with other existing publications and to show the close interdependence between the three parts, the original overall structure was kept as far as practicable. Therefore, entire Clauses and Annexes have been left empty with a reference to where they can be found in either Part 1 or Part 3.

4 General operational requirements

Refer to ISO/IEC 24739-1, Clause 4 for operational requirements (see 3.4).

5 I/O register descriptions

Refer to ISO/IEC 24739-1, Clause 5 for I/O register descriptions and see also Clause 10 for parallel interface register addressing (see 3.4).

6 Command descriptions

Refer to ISO/IEC 24739-1, Clause 6 for command descriptions (see 3.4).

7 Parallel interface physical and electrical requirements

7.1 Cable configuration

This standard defines an interface containing a single host or host adapter and one or two devices. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways including but not limited to

- a switch or a jumper on the device,
- use of the Cable Select (CSEL) pin.

The host shall be placed at one end of the cable. It is recommended that, for a single device configuration, the device be placed at the opposite end of the cable from the host. If a single device configuration is implemented with the device not at the end of the cable, a cable stub results that may cause degradation of signals. Single device configurations with the device not at the end of the cable shall not be used with Ultra DMA modes.

7.2 Electrical characteristics

7.2.1 General

Table 4 defines the DC characteristics of the interface signals. Table 5 defines the AC characteristics. These characteristics apply to both host and device, unless otherwise specified.

Table 4 – DC characteristics

Description		Minimum	Maximum
I_{OL}	Driver sink current ^a	4 mA	
I_{OLDASP}	Driver sink current for DASP ^a	12 mA	
I_{OH}	Driver source current ^b	400 μ A	
$I_{OHDMARQ}$	Driver source current for DMARQ ^b	500 μ A	
I_Z	Device pull-up current on DD(15:8), DD(6:0) and STROBE when released	–100 μ A	200 μ A
I_{ZDD7}	Device pull-up current on DD7 when released	–100 μ A	10 μ A
V_{IH}	Voltage input high	2.0 VDC	5.5 VDC
V_{IL}	Voltage input low		0.8 VDC
V_{OH}	Voltage output high at I_{OH} min ^c	2.4 VDC	
V_{OL}	Voltage output low at I_{OL} min ^c		0.5 VDC
Additional DC characteristics for Ultra DMA modes greater than 4			
VDD3	DC supply voltage to drivers and receivers	3.3 V – 8 %	3.3 V + 8 %
V+	Low to high input threshold	1.5 V	2.0 V
V–	High to low input threshold	1.0 V	1.5 V
VHYS	Difference between input thresholds: ((V+current value) – (V–current value))	320 mV	
VTHRAVG	Average of thresholds: ((V+current value) + (V–current value))/2	1.3 V	1.7 V
VoH2	Voltage output high at –6 mA to +3 mA (at VoH2 the output shall be able to supply and sink current to VDD3) ^c	VDD3 – 0.51 VDC	VDD3 + 0.3 VDC
VoL2	Voltage output low at 6 mA ^c		0.51 VDC

A device shall have less than 64 μ A of leakage current into a 6.2 k Ω pull-down resistor while the INT pin is in the high state.

released state.

^a I_{oLDASP} shall be 12 mA minimum to meet legacy timing and signal integrity.

^b I_{oH} value at 400 μ A is insufficient in the case of DMARQ that is pulled low by a 5.6 k Ω resistor.

^c Voltage output high and low values shall be met at the source connector to include the effect of series termination.

Table 5 – AC characteristics

Description		Minimum	Maximum
S_{RISE}	Rising edge slew rate for any signal ^a		1.25 V/ns
S_{FALL}	Falling edge slew rate for any signal ^a		1.25 V/ns
C_{host}	Host interface signal capacitance at the host connector ^b		25 pF
C_{device}	Device interface signal capacitance at the device connector ^b		20 pF
Additional AC characteristics for Ultra DMA modes greater than mode 4			
S_{RISE2}	Rising edge slew rate for DD(15:0) and STROBE ^a	0.40 V/ns	1.0 V/ns
S_{FALL2}	Falling edge slew rate for DD(15:0) and STROBE ^a	0.40 V/ns	1.0 V/ns
VDSSOH	Induced signal to conductor side of device connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the device ^c	VDD3 - 500 mV	
VDSSOL	Same as VDSSOH except non-switching data signal at VoL ^c		500 mV
VHSSOH	Induced signal to conductor side of host connector for any non-switching data signal at VoH due to simultaneous switching of all other data lines high and low by the host ^c	VDD3 – 600 mV	
VHSSOL	Same as VHSSOH except non-switching data signal at VoL ^c		600 mV
V_{RING}	AC voltage at recipient connector ^d	-1.0 V	6.0 V
$C_{device2}$	Device capacitance measured at the connector pin ^b		17 pF
C_{ratio}	Ratio of the highest DD(15:0) or STROBE signal capacitance as measured at the connector to the lowest DD(15:0) or STROBE signal capacitance.		1.5
V_{ihPEAK}	The highest voltage reached on a rising transition at the recipient connector within 3 ns of crossing 1.5 V ^e	2.2 V	
V_{ihRING}	The lowest voltage on a high signal at the recipient connector at any time after the rising edge crosses V_{ihPEAK} until activity driven low by a subsequent falling transition ^e	1.7 V	
V_{ilPEAK}	The lowest voltage reached on a falling transition at the recipient connector within 3 ns of crossing 1.5 V ^e		0.8 V
V_{ilRING}	The highest voltage on a low signal at the recipient connector at any time after the falling edge crosses V_{ilPEAK} until activity driven high by a subsequent rising transition ^e		1.3 V
^a Signal integrity may be improved by using slower slew rates at slower transfer rates. ^b Capacitance measured at 1 MHz . ^c See 7.2.2.2 for measurement details. ^d The sender shall not generate voltage peaks higher then these absolute limits on DD(15:0) with all data lines switching simultaneously and a single recipient at end of cable. The test load shall be an 18" long, 40-conductor cable in Ultra DMA mode 2, as well as, an 18", long 80-conductor cable operated in the highest Ultra DMA mode supported. ^e V_{ihPEAK} , V_{ihRING} , V_{ilPEAK} and V_{ilRING} shall be met in a functioning system across all patterns and shall be met when measured at any connector.			

7.2.2 AC characteristics measurement techniques

7.2.2.1 Slew rate

The sender's signals shall be tested while driving an 45.7 cm (18 in) long, 80-conductor cable with PVC insulation material. The signal under test shall be cut at a test point so that it has no trace, cable, or recipient loading after the test point. All other signals should remain connected through to the recipient. The test point may be located at any point between the sender's series termination resistor and 12.7 mm (0.5 in) or less of conductor exiting the connector. If the test point is on a cable conductor rather than the PCB, an adjacent ground conductor shall also be cut within 12.7 mm (0.5 in) of the connector. The test load and test points should then be soldered directly to the exposed source side connectors. The test load shall consist of a 15 pF or 40 pF, 5 %, 2.03 mm (0.08 in) by 1.27 mm (0.05 in), surface mount (or smaller size) capacitor from the test point to ground. Slew rates shall be met for both capacitor values. Measurements shall be taken at the test point using a 1 GHz or faster test probe with less than 1 pF capacitance and greater than 100 k Ω impedance connected to a 500 MHz or faster oscilloscope. The average rate shall be measured from 20 % to 80 % of the settled V_{OH} level with data transitions at least 120 ns apart. The settled V_{OH} level shall be measured as the average output high level under the defined testing conditions from 100 ns after 80 % of a rising edge until 20 % of the subsequent falling edge.

7.2.2.2 V_{SSO}

V_{SSO} shall be tested with the same test cable configuration as described for slew rate testing except with the test load described here and the cut-cable-conductor configuration. For both V_{OL} and V_{OH} measurements, the test load shall consist of a 90.9 Ω 1 % resistor (this also may be accomplished by using 1 k Ω 1 % and 100 Ω 1 % resistors in parallel) and a 0.1 μ F 20 % capacitor in series to ground. Both resistor and capacitor shall be 2.03 mm (0.08 in) by 1.27 mm (0.05 in) or smaller surface mount. The order of components should be signal-resistor-capacitor-ground. Refer to 7.2.4.4 for PCB layout requirements related to V_{SSO} .

To generate a test pattern for V_{SSOH} a 32-sector or longer data transfer shall be sent to the recipient. The first 30 sectors shall contain Fh in order to generate an "all 1s" pattern to pre-charge the capacitor to V_{OH} . The final sectors of the command shall contain the required pattern for V_{SSOH} for at least 2 sectors (i.e., a pattern that holds the data line under test at V_{OH} while driving a "1010..." pattern on all other data lines. V_{SSOH} shall be measured within the first 32 words after the pre-charge pattern is complete and the V_{SSOH} pattern begins.

To generate a test pattern for V_{SSOL} a 32-sector or longer data transfer shall be sent to the recipient. The first 30 sectors shall contain 0h in order to generate an "all 0's" pattern to pre-charge the capacitor to V_{OL} . The final sectors of the command shall contain the required pattern for V_{SSOL} for at least 2 sectors (i.e., a pattern that holds the data line under test at V_{OL} while driving a "1010..." pattern on all other data lines. V_{SSOL} shall be measured within the first 32 words after the pre-charge pattern is complete and the V_{SSOL} pattern begins.

7.2.3 Driver types and required termination

Table 6 – Driver types and required termination

Signal	Source	Driver type ^a	Host ^b	Device ^b	Footnotes to table
RESET-	Host	TP			
DD(15:0)	Bidir	TS			^c
DMARQ	Device	TS	5.6 kΩ PD		
DIOR-:HDMARDY-:HSTROBE	Host	TS			
DIOW-:STOP	Host	TS			
IORDY:DDMARDY-:DSTROBE	Device	TS	4.7 kΩ PU		^{f, k}
CSEL	Host		Ground	10 kΩ PU	^{d, f}
DMACK-	Host	TP			
INTRQ	Device	TS	10 kΩ		^e
DA(2:0)	Host	TP			
PDIAG-:CBLID-	Device	TS		10 kΩ PU	^{b, f, g, h}
CS0- CS1-	Host	TP			
DASP-	Device	OC		1 kΩ PU	^{f, i}

^a TS = Tri-state; OC = Open collector; TP = Totem-pole; PU = Pull-up; PD = Pull-down.

^b All resistor values are the minimum (lowest allowed) except for the 10 kΩ PU on PDIAG-:CBLID- which shall have a tolerance of ±5 % or less.

^c Devices shall not have a pull-up resistor on DD7. The host shall have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up so that a host shall detect BSY as being cleared when attempting to read the Status register of a device that is not present.

^d When used as CSEL, this line is grounded at the host and a 10 kΩ pull-up is required at both devices.

^e A 10 kΩ pull-up or 6.2 kΩ pull-down, depending upon the level sensed, should be implemented at the host.

^f Pull-up values are based on +5 V_{CC}. Except for the pull-up on PDIAG-:CBLID- which shall be to +5 V_{CC} for backward compatibility, pull-ups may be to V_{DD3}. For systems supporting Ultra DMA modes greater than 4, the host pull-up on IORDY:DDMARDY-:DSTROBE should be to V_{DD3}.

^g Hosts that do not support Ultra DMA modes greater than mode 2 shall not connect to the PDIAG-:CBLID- signal.

^h The 80-conductor cable assembly shall meet the following requirements: the PDIAG-:CBLID- signal shall be connected to ground in the host connector of the cable assembly; the PDIAG-:CBLID- signal shall not be connected between the host and the devices; and the PDIAG-:CBLID- signal shall be connected between the devices.

ⁱ The host shall not drive DASP-. If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain V_{OH} and V_{OL} compatibility, given the I_{OH} and I_{OL} requirements of the DASP- device drivers.

^k For host systems not supporting modes greater than Ultra DMA mode 4, a pull-up of 1 kΩ may be used.

7.2.4 Electrical characteristics for Ultra DMA

7.2.4.1 General

Hosts that support Ultra DMA transfer modes greater than mode 2 shall not share signals between primary and secondary I/O ports. They shall provide separate drivers and separate receivers for each cable.

7.2.4.2 Cable configuration

Table 7 defines the host transceiver configurations for a dual cable system configuration for all transfer modes.

Table 7 – Host transceiver configurations

Transfer mode	Optional host transceiver configuration	Recommended host transceiver configuration	Mandatory host transceiver configuration
All PIO and Multiword DMA	One transceiver may be used for signals to both ports.	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port.
Ultra DMA 0, 1, 2	One transceiver may be used for signals to both ports except DMACK-.	DIOR-, DIOW- and IORDY should have a separate transceiver for each port.	Either DIOR-, DIOW- and IORDY or CS0- and CS1- shall have a separate transceiver for each port. DMACK- shall have a separate transceiver for each port.
Ultra DMA modes >2	One transceiver may be used for signals to both ports for RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP-.	RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP- should have a separate transceiver for each port.	All signals shall have a separate transceiver for each port except for RESET-, INTRQ, DA(2:0), CS0-, CS1- and DASP-.

Table 8 defines the system configuration for connection between devices and systems for all transfer modes. For Ultra DMA modes requiring an 80-conductor cable, that cable shall meet the requirements for 80-conductor cables (see 7.3.2.3).

Table 8 – System configuration for connection between devices and systems for all transfer modes

Transfer mode	Single device direct connection configuration ^a	40-conductor cable connection configuration ^b	80-conductor cable connection configuration ^b
All PIO and Multiword DMA	May be used.	May be used.	May be used ^c
Ultra DMA 0, 1, 2	May be used.	May be used.	May be used ^c
Ultra DMA modes >2	May be used (See NOTE 4).	Shall not be used.	May be used ^d

^a Direct connection is a direct point-to-point connection between the host connector and the device connector.

^b The 40-conductor cable assembly and the 80-conductor cable assembly are defined in 7.3.

^c 80-conductor cable assemblies may be used in place of 40-conductor cable assemblies to improve signal quality for data transfer modes that do not require an 80-conductor cable assembly.

^d Either a single device direct connection configuration or an 80-conductor cable connection configuration shall be used for systems operating with Ultra DMA modes greater than 2.

7.2.4.3 Series termination required for Ultra DMA

Series termination resistors are required at both the host and the device for operation in any of the Ultra DMA modes. Table 9 describes typical values for series termination at the host and the device.

For host systems and devices supporting Ultra DMA modes greater than 4, the output and bi-directional series termination values for DD(15:0) and STROBE signals shall be chosen so that the sum of the driver output resistance at V_{OL2} or V_{OH2} and the series termination resistance is

between 50 Ω and 85 Ω . For these systems, the STROBE input shall use the same series termination resistance value as the data lines.

Host systems supporting Ultra DMA modes greater than 5 and having PCB traces longer than 4" shall use series termination resistors of no less than 22 Ω on DD(15:0) and STROBE signals. The termination resistors shall be placed within 12.7 mm (0.5 in) of the host connector.

Table 9 – Typical series termination for Ultra DMA

Signal	Host termination Ω	Device termination Ω
DIOR-:HDMARDY-:HSTROBE	22	82
DIOW-:STOP	22	82
CS0-, CS1-	33	82
DA0, DA1, DA2	33	82
DMACK-	22	82
DD15 through DD0	33	33
DMARQ	82	22
INTRQ	82	22
IORDY:DDMARDY-:DSTROBE	82	22
RESET-	33	82

Only those signals that require termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA mode. Figure 4 shows signals also requiring a pull-up or pull-down resistor at the host. The actual termination values should be selected to compensate for transceiver and trace impedance to match the characteristic cable impedance.

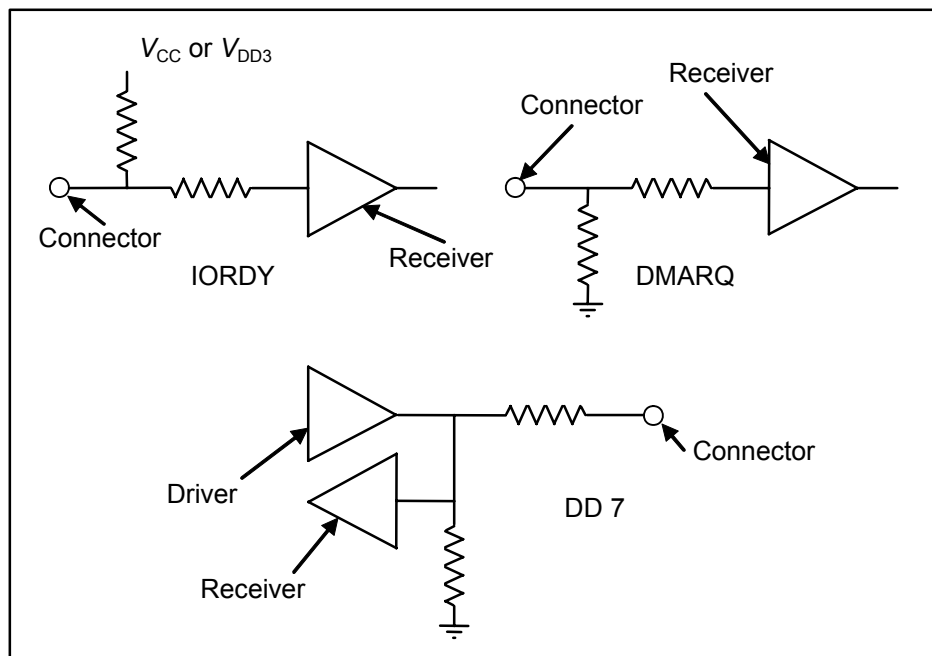


Figure 4 – Ultra DMA termination with pull-up or pull-down

7.2.4.4 PCB trace requirements for Ultra DMA

PCB trace layout is a factor in meeting the V_{SSO} values in Table 4.

The longest DD(15:0) or STROBE trace for any device supporting Ultra DMA modes greater than 5 shall be 101.6 mm (4 in).

On any PCB for a host or device supporting Ultra DMA: The longest DD(15:0) trace shall be no more than 12.7 mm (0.5 in) longer than either STROBE trace as measured from the IC pin to the connector. The shortest DD(15:0) trace shall be no more than 12.7 mm (0.5 in) shorter than either STROBE trace as measured from the IC pin to the connector.

Any DD(15:0) or STROBE trace on a PCB for a host or device supporting Ultra DMA modes greater than 5 shall meet the following:

$$L / (1 + (D / H)^2) < 0.8 \quad (1)$$

where

L is the trace length in mm/25.4 (inches);

D is the center-to-center trace spacing of adjacent traces. If both traces are the same width, this is equivalent to one trace width plus the trace separation.

H is the height of the trace above a continuous, unbroken supply plane. The plane may be power or ground but if a power plane is used, it must be bypassed to the ground plane on both sides of the DD(15:0) bus near the connector ground pins and at the IC.

The units used for *D* and *H* shall be the same.

7.3 Connectors and cable assemblies

7.3.1 General

The device shall implement one of the connector options described in this subclause.

7.3.2 40-pin connector

7.3.2.1 General

The I/O connector is a 40-pin connector. The header mounted to a host or device is shown in Figure 5 and the dimensions are shown in Table 10. The connector mounted to the end of the cable is shown in

Figure 6 and the dimensions are shown in Table 11. Signal assignments on these connectors are shown in Table 12.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle may or may not be polarized and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable can connect devices. As shown in Figure 7, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180° between a device with top-mounted receptacles and a device with bottom-mounted receptacles.

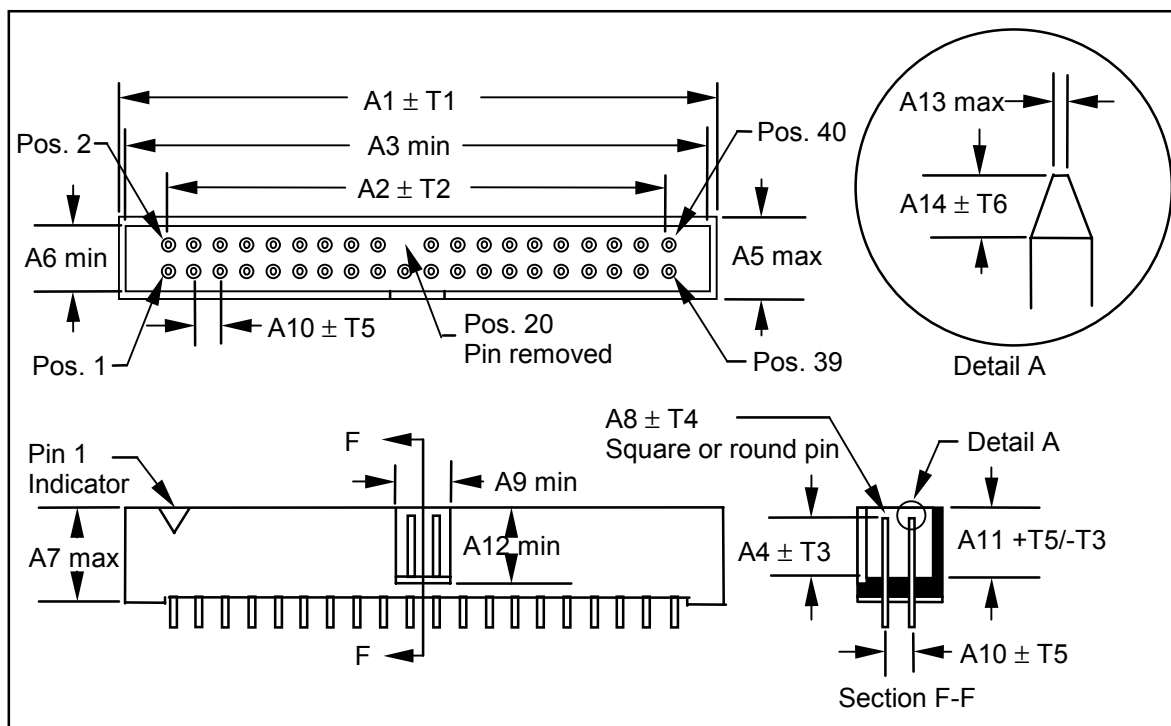


Figure 5 – Host or device 40-pin I/O header

Table 10 – Host or device 40-pin I/O header

Dimension	mm	in
A1	58.17	2.290
A2	48.26	1.900
A3	56.01	2.205
A4	5.84	0.230
A5	9.55	0.376
A6	6.22	0.245
A7	10.16	0.400
A8	0.64	0.025
A9	4.06	0.160
A10	2.54	0.100
A11	6.35	0.250
A12	6.48	0.255
A13	0.33	0.013
A14	0.58	0.023
T1	0.51	0.020
T2	0.13	0.005
T3	0.25	0.010
T4	0.03	0.001
T5	0.08	0.003
T6	0.18	0.007

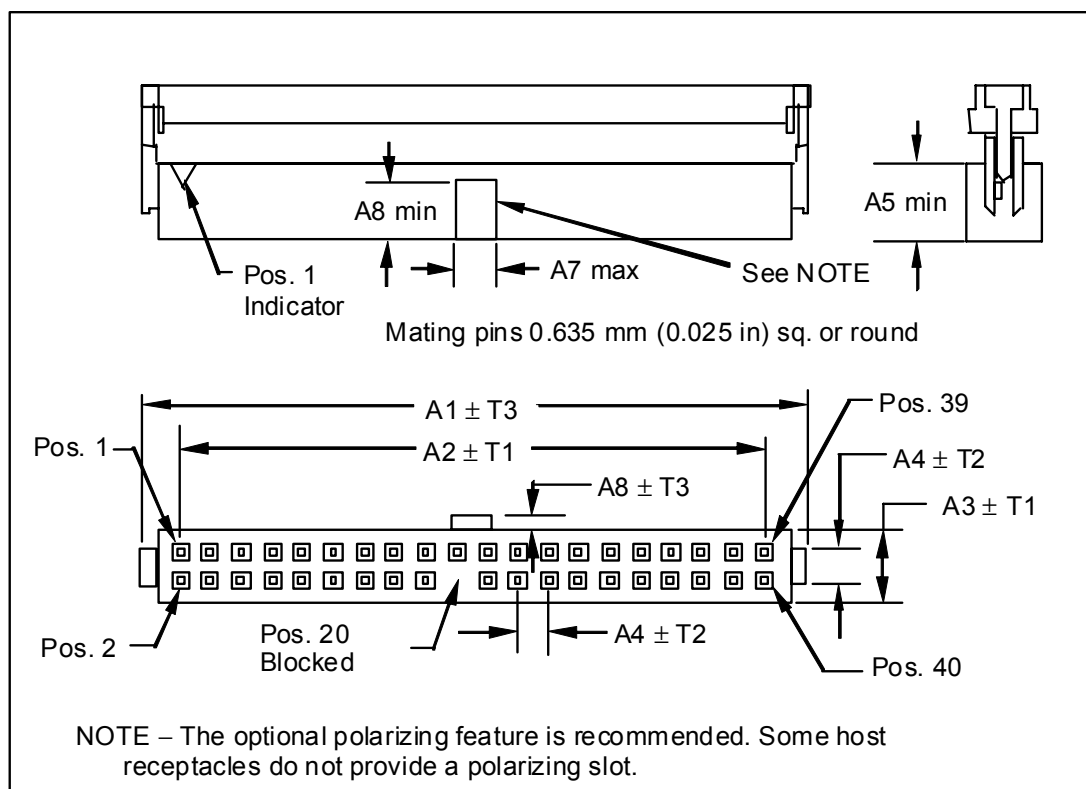


Figure 6 – 40-pin I/O cable connector

Table 11 – 40-pin I/O cable connector

Dimension	mm	in
A1	55.37	2.180
A2	48.26	1.900
A3	6.10	0.240
A4	2.54	0.100
A5	6.48	0.255
A6	4.57	0.180
A7	3.81	0.150
A8	1.27	0.050
T1	0.13	0.005
T2	0.08	0.003
T3	0.25	0.010

Table 12 – 40-pin I/O connector interface signals

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY- :HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY- :DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	Obsolete ^a
DA1	33	33	34	34	PDIAG-:CBLID-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

^a Pin 32 was defined as IOCS16 in ATA-2, ANSI X3.279-1996.

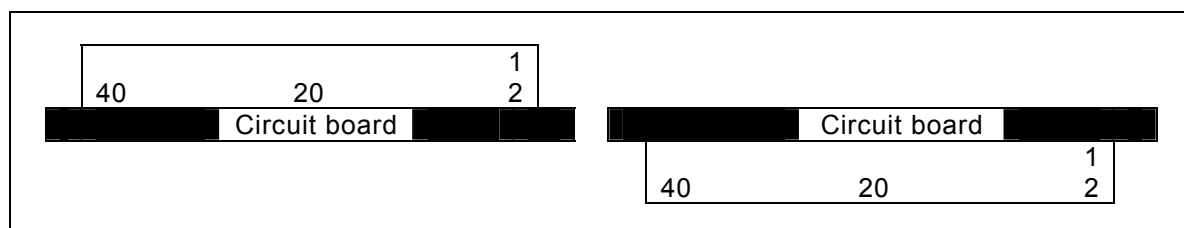


Figure 7 – 40-pin I/O header mounting

7.3.2.2 40-conductor cable

The 40-conductor cable assembly is shown in Figure 8 with dimensions in Table 13. Cable capacitance shall not exceed 35 pF.

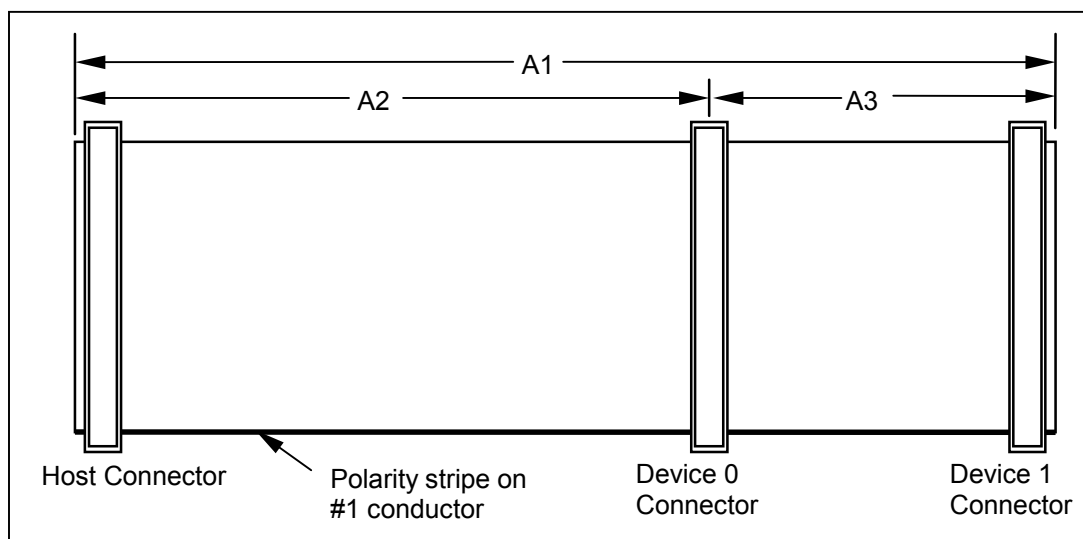


Figure 8 – 40-conductor cable configuration

Table 13 – 40-conductor cable configuration

Dimension	mm	in
1	254.00 min.	10.00 min.
	457.20 max.	18.00 max.
A2	127.00 min.	5.00 min.
	304.80 max.	12.00 max.
A3	127.00 min.	5.00 min.
	152.40 max.	6.00 max.

7.3.2.3 80-conductor cable assembly using the 40-pin connector

To provide better signal integrity, the optional 80-conductor cable assembly is specified for use with 40-pin connectors. Use of this assembly is mandatory for systems operating at Ultra DMA modes greater than 2. The mating half of the connector is as described in 7.3.2. Every other conductor in the 80-conductor cable is connected to the ground pins in each connector.

The electrical requirements of the 80-conductor ribbon cable are shown in Table 14 and the physical requirements are described in Figure 9 and Table 15.

Figure 10 and Table 16 describe the physical dimensions of the cable assembly. The connector in the center of the cable assembly labelled Device 1 Connector is optional. The System Board connector shall have a blue base and a black or blue retainer. The Device 0 Connector shall have a black base and a black retainer. The Device 1 Connector shall have a gray base and a black or gray retainer. The cable assembly may be printed with connector identifiers.

There are alternative cable conductor to connector pin assignments depending on whether the connector attaches all even or odd conductors to ground. Table 17 shows the signal assignments for connectors that ground the even numbered conductors. Table 18 shows the signal assignments for connectors that ground the odd numbered conductors. Only one connector type, even or odd, shall be used in a given cable assembly. Connectors shall be labelled as grounding the even or odd conductors, as shown in Figure 11. Cable assemblies conforming to Table 17 are interchangeable with cable assemblies conforming to Table 18.

All connectors shall have position 20 blocked to provide keying. Pin 28 in Device 1 Connector shall not be attached to any cable conductor, the connector contact may be removed to meet this requirement (see 8.2.13.3). Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).

Table 14 – 80-conductor cable electrical requirements

Conductor		0.050 92 mm ² (30 AWG)
Ground-signal-ground		
Single ended impedance	(Ω)	70 to 90
Capacitance	(pF/ft)	13 to 22
	(pF/m)	42 to 72
Inductance	(μH)	0.08 to 0.16
Propagation delay	(ns/ft)	1.35 to 1.65
	(ns/m)	4.43 to 5.41

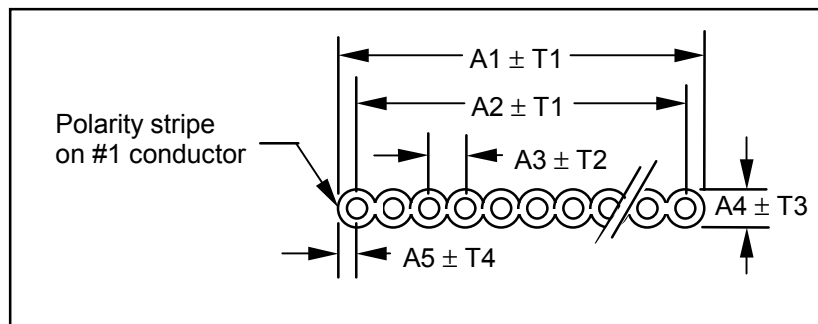


Figure 9 – 80-conductor ribbon cable

Table 15 – 80-conductor ribbon cable

Dimension	mm	in
A1	50.800	2.000
A2	50.165	1.975
A3	0.635	0.025
A4	0.685 8	0.027
A5	0.317 5	0.012 5
T1	0.127	0.005
T2	0.0406	0.001 6
T3	0.050 8	0.002
T4	0.102	0.004

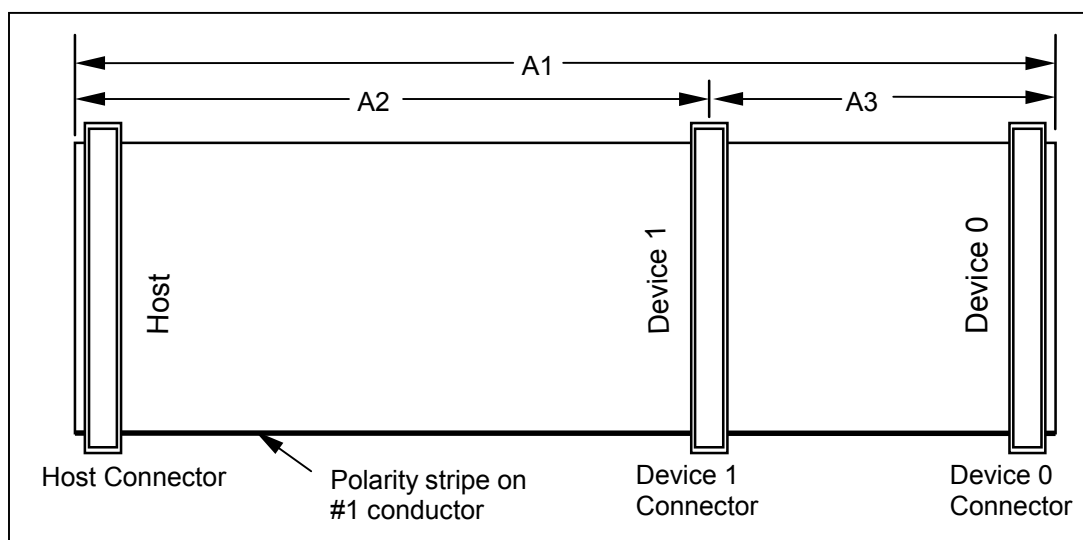


Figure 10 – 80-conductor cable configuration

Table 16 – 80-conductor cable configuration

Dimension	mm	in
A1	457.20 max.	18.00 max.
A2	127.00 min.	5.00 min.
A3	152.40 max.	6.00 max.
A2 min. shall be greater than or equal to A3.		

Table 17 – Signal assignments for connectors grounding even conductors

Signal name	Connector contact	Conductor		Signal name
RESET-	1	1	2	Ground
Ground	2	3	4	Ground
DD7	3	5	6	Ground
DD8	4	7	8	Ground
DD6	5	9	10	Ground
DD9	6	11	12	Ground
DD5	7	13	14	Ground
DD10	8	15	16	Ground
DD4	9	17	18	Ground
DD11	10	19	20	Ground
DD3	11	21	22	Ground
DD12	12	23	24	Ground
DD2	13	25	26	Ground
DD13	14	27	28	Ground
DD1	15	29	30	Ground
DD14	16	31	32	Ground
DD0	17	33	34	Ground
DD15	18	35	36	Ground
Ground	19	37	38	Ground
(keypin)	20	39	40	Ground
DMARQ	21	41	42	Ground
Ground	22	43	44	Ground
DIOW-	23	45	46	Ground
Ground	24	47	48	Ground
DIOR-	25	49	50	Ground
Ground	26	51	52	Ground
IORDY	27	53	54	Ground
CSEL	28	55	56	Ground
DMACK-	29	57	58	Ground
Ground	30	59	60	Ground
INTRQ	31	61	62	Ground
Reserved	32	63	64	Ground
DA1	33	65	66	Ground
PDIAG-	34 ^a	67	68	Ground
DA0	35	69	70	Ground
DA2	36	71	72	Ground
CS0-	37	73	74	Ground
CS1-	38	75	76	Ground
DASP-	39	77	78	Ground
Ground	40	79	80	Ground
^a Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).				

Table 18 – Signal assignments for connectors grounding odd conductors

Signal name	Conductor		Connector contact	Signal name
Ground	1	2	1	RESET-
Ground	3	4	2	Ground
Ground	5	6	3	DD7
Ground	7	8	4	DD8
Ground	9	10	5	DD6
Ground	11	12	6	DD9
Ground	13	14	7	DD5
Ground	15	16	8	DD10
Ground	17	18	9	DD4
Ground	19	20	10	DD11
Ground	21	22	11	DD3
Ground	23	24	12	DD12
Ground	25	26	13	DD2
Ground	27	28	14	DD13
Ground	29	30	15	DD1
Ground	31	32	16	DD14
Ground	33	34	17	DD0
Ground	35	36	18	DD15
Ground	37	38	19	Ground
Ground	39	40	20	(keypin)
Ground	41	42	21	DMARQ
Ground	43	44	22	Ground
Ground	45	46	23	DIOW-
Ground	47	48	24	Ground
Ground	49	50	25	DIOR-
Ground	51	52	26	Ground
Ground	53	54	27	IORDY
Ground	55	56	28	CSEL
Ground	57	58	29	DMACK-
Ground	59	60	30	Ground
Ground	61	62	31	INTRQ
Ground	63	64	32	Reserved
Ground	65	66	33	DA1
Ground	67	68	34 ^a	PDIAG-
Ground	69	70	35	DA0
Ground	71	72	36	DA2
Ground	73	74	37	CS0-
Ground	75	76	38	CS1-
Ground	77	78	39	DASP-
Ground	79	80	40	Ground

^a Pin 34 in the Host Connector shall not be attached to any cable conductor and shall be attached to Ground within the connector (see 9.4).

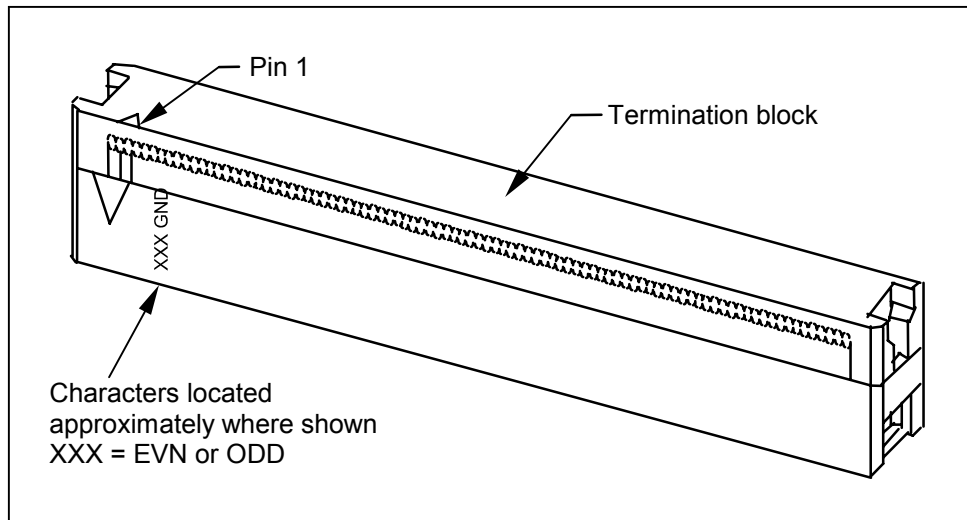


Figure 11 – Connector labeling for even or odd conductor grounding

7.3.3 4-pin power connector

7.3.3.1 General

The power connector is a 4-pin connector. The header mounted to a device is shown in Figure 12 and the dimensions are shown in Table 19. The connector mounted to the end of the cable is shown in Figure 13 and the dimensions are shown in Table 20. Pin assignments for these connectors are shown in Table 21.

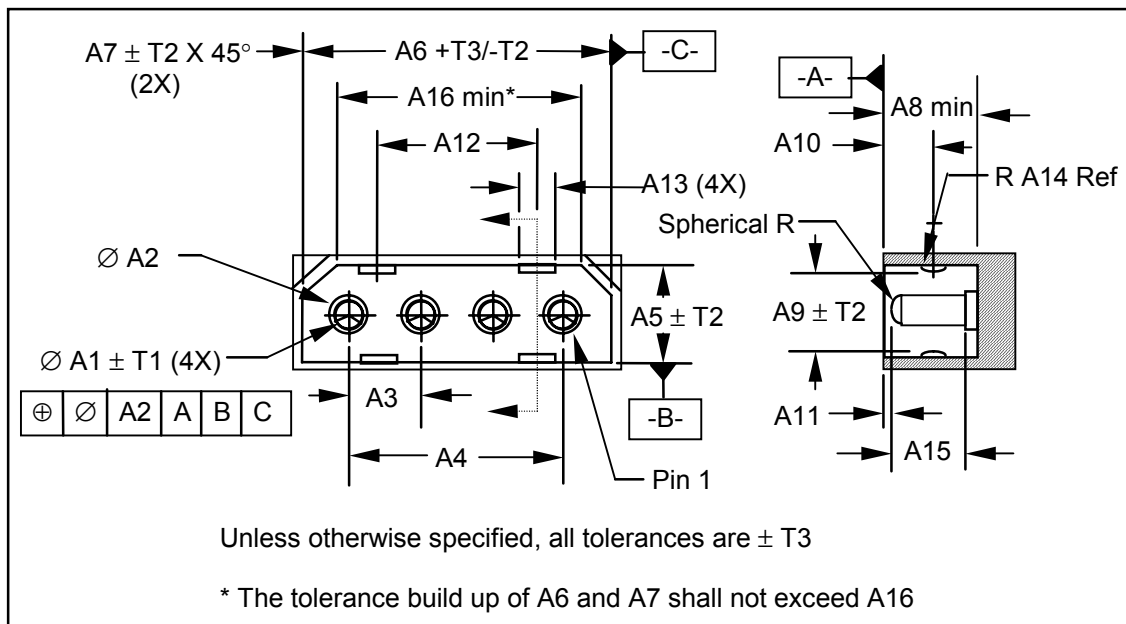


Figure 12 – Device 4-pin power header

Table 19 – Device 4-pin power header

Dimension	mm	in
A1	2.10	0.083
A2	3.50	0.138
A3	5.08	0.200
A4	15.24	0.600
A5	6.60	0.260
A6	21.32	0.839
A7	1.65	0.065
A8	7.50	0.295
A9	6.00	0.236
A10	4.95	0.195
A11	1.00	0.039
A12	11.18	0.440
A13	3.80	0.150
A14	3.00	0.118
A15	5.10	0.201
A16	17.80	0.701
T1	0.04	0.0016
T2	0.15	0.006
T3	0.25	0.010

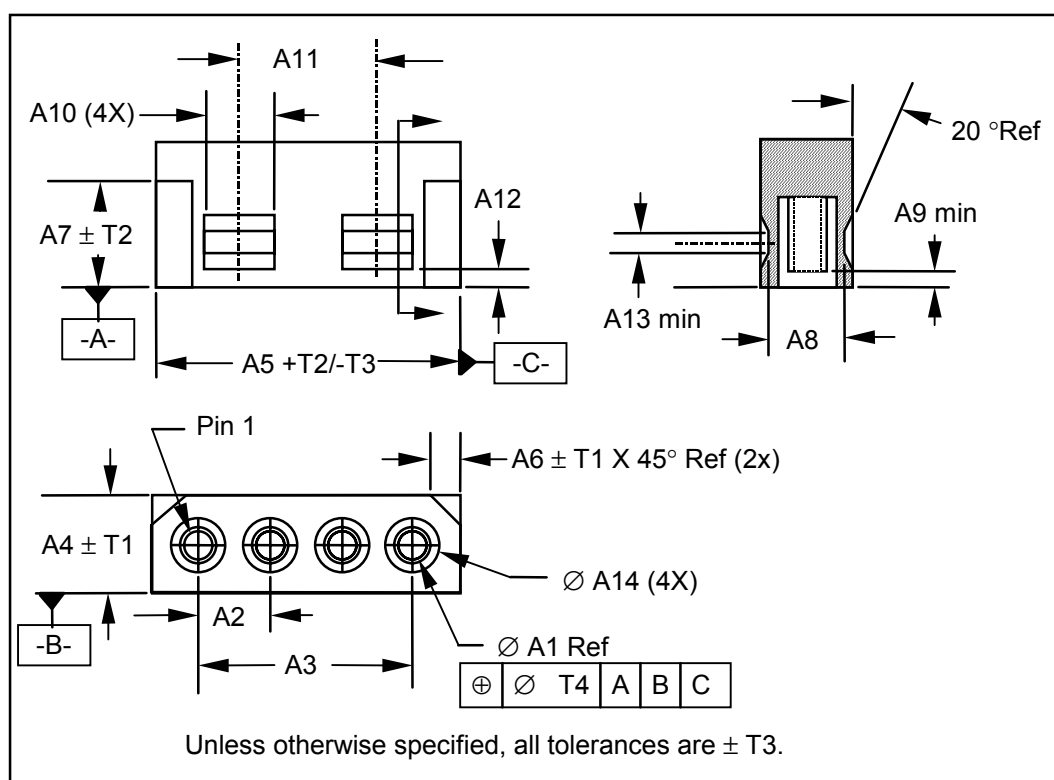
**Figure 13 – 4-pin power cable connector**

Table 20 – 4-pin power cable connector

Dimension	mm	in
A1	2.03	0.080
A2	5.08	0.200
A3	15.24	0.600
A4	6.35	0.250
A5	21.00	0.827
A6	1.78	0.070
A7	7.87	0.310
A8	5.51	0.217
A9	1.19	0.047
A10	5.08	0.200
A11	11.18	0.440
A12	1.19	0.047
A13	2.00	0.079
A14	4.06	0.160
T1	0.10	0.004
T2	0.15	0.006
T3	0.25	0.010
T4	0.60	0.024

Table 21 – 4-pin power connector pin assignments

Power line	Pin
+12 V	1
+12 V return	2
+5 V return	3
+5 V	4

7.3.3.2 Mating performance

Mating force should be 1.75 kg (3.85 lbs) maximum per contact.

Unmating force should be 113.5 g (0.25 lbs) minimum per contact.

7.3.4 Unitized connectors

The 40-pin I/O signal header and the 4-pin power connector may be implemented in one of two unitized connectors that provide additional pins for configuration jumpers. The dimensioning of the 40-pin I/O signal area shall be as defined in Figure 5 and the dimensioning of the 4-pin power connector area shall be as defined in Figure 12 for both unitized connectors.

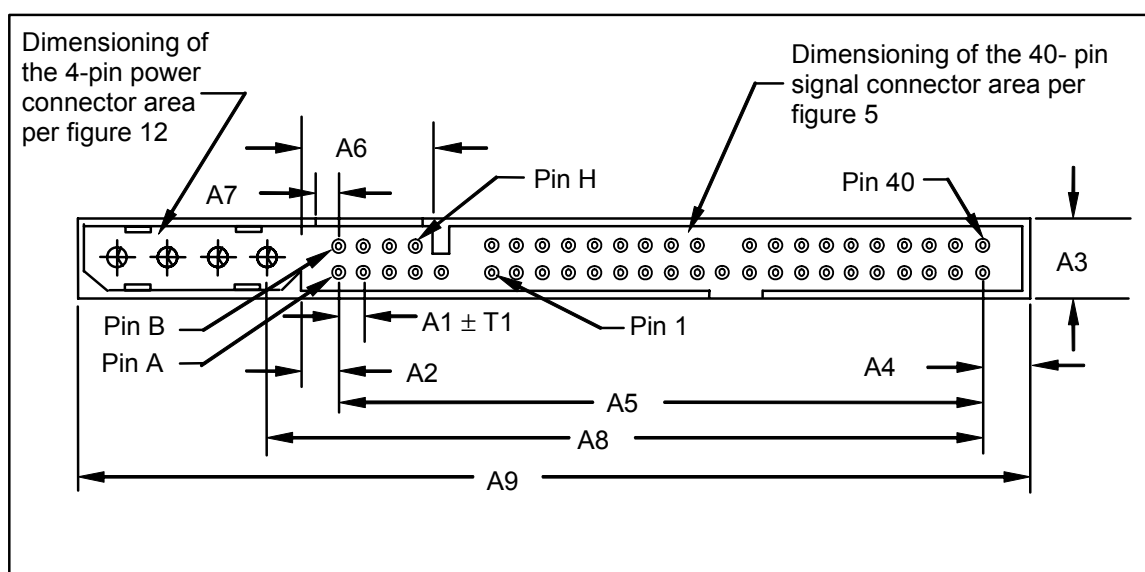
The first of the unitized connectors is shown in Figure 14 with dimensions as shown in Table 22. The jumper pins, A through I, have been assigned as follows:

- E-F - CSEL
- G-H - Master
- G-H and E-F - Master with slave present

- No jumper - Slave
- A through D - Vendor specific
- I - Reserved

The second of the unitized connectors is shown in Figure 15 with dimensions as shown in Table 23. The jumper pins, A through J, have been assigned as follows:

- A-B - CSEL
- C-D - Slave
- E-F - Master
- G through J - Vendor specific



Tolerances ± 0.254 mm (0.010 in) unless otherwise specified.

Figure 14 – Unitized connector

Table 22 – Unitized connector

Dimension	mm	in
A1	2.54	0.100
A2	4.06	0.160
A3	8.40	0.331
A4	5.26	0.207
A5	63.50	2.500
A6	13.54	0.533
A7	2.54	0.100
A8	70.825	2.788
A9	95.50	3.760
T1	0.15	0.006

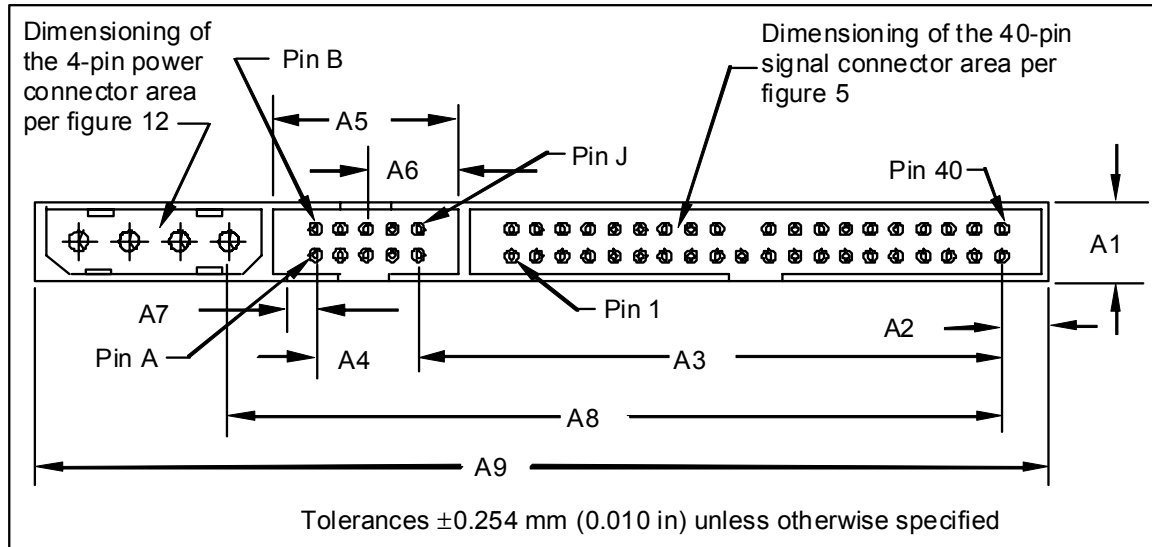


Figure 15 – Unitized connector

Table 23 – Unitized connector

Dimension	mm	in
A1	8.51	0.335
A2	5.51	0.217
A3	57.15	2.250
A4	10.16	0.400
A5	17.88	0.704
A6	8.94	0.352
A7	2.54	0.100
A8	75.29	2.964
A9	100.33	3.950

7.3.5 50-pin 65 mm (2.5 in) form factor style connector

An alternative connector is often used for 65 mm (2.5 in) or smaller devices. This connector is shown in Figure 16 with dimensions shown in Table 24. Signal assignments are shown in Table 25. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used.

Pins E, F and 20 are keys and are removed.

Some devices may use pins A, B, C and D for option selection via physical jumpers. If a device uses pins A, B, C and D for device selection, when no jumper is present the device should be designated as Device 0. When a jumper is present between pins B and D, the device should respond to the CSEL signal to determine the device number.