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Edition 1.0 2010-03

INTERNATIONAL STANDARD

**Information technology – AT attachment with packet interface-7 –
Part 3: Serial transport protocols and physical interconnect (ATA/ATAPI-7 V3)**



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INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 3: Serial transport protocols and physical interconnect (ATA/ATAPI-7 V3)

FOREWORD

- 1) ISO (International Organization for Standardization) and IEC (International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards. Their preparation is entrusted to technical committees; any ISO and IEC member body interested in the subject dealt with may participate in this preparatory work. International governmental and non-governmental organizations liaising with ISO and IEC also participate in this preparation.
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International Standard ISO/IEC 24739-3 was prepared by subcommittee 25: Interconnection of information technology equipment, of ISO/IEC joint technical committee 1: Information technology.

ISO/IEC 24739-3 is to be used in conjunction with ISO/IEC 24739-1 and ISO/IEC 24739-2.

The list of all currently available parts of the ISO/IEC 24739 series, under the general title *Information technology – AT attachment with packet interface-7*, can be found on the IEC web site.

This International Standard has been approved by vote of the member bodies, and the voting results may be obtained from the address given on the second title page.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

INTRODUCTION

The ISO/IEC 24739 series specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

ISO/IEC 24739-1 defines the register delivered commands used by devices implementing the standard. ISO/IEC 24739-2 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals, and the protocols for the transporting of commands, data, and status over the interface for the parallel interface. ISO/IEC 24739-3 defines the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals, and the protocols for the transporting of commands, data, and status over the interface for the serial interface. Figure 1 shows the relationship of these documents. For devices implementing the PACKET command feature set, additional command layer standards are listed in Table 1 and described in Clause 2.

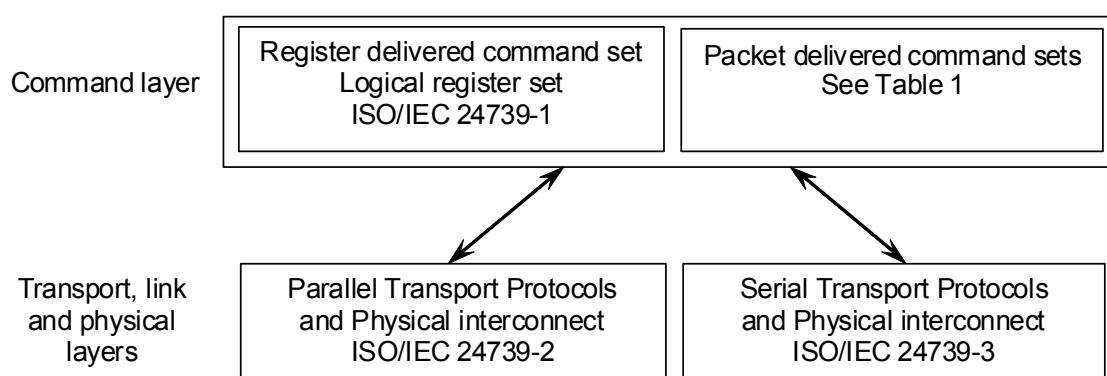


Figure 1 – ATA document relationships

Table 1 – PACKET delivered command sets

Standard
SCSI Primary Commands (SPC)
SCSI Primary Commands-2 (SPC-2)
SCSI Primary Commands-3 (SPC-3)
SCSI Block Commands (SBC-2)
SCSI Stream Commands (SSC)
Multimedia Commands (MMC)
Multimedia Commands-2 (MMC-2)
Multimedia Commands-3 (MMC-3)
Multimedia Commands-4 (MMC-4)
ATAPI for Removable Media
ATA Packet Interface (ATAPI) for Streaming Tape QIC-157 revision D

This standard maintains compatibility with the AT Attachment with Packet Interface - 6 standard (ATA/ATAPI-6) and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

INFORMATION TECHNOLOGY – AT ATTACHMENT WITH PACKET INTERFACE-7 –

Part 3: Serial transport protocols and physical interconnect (ATA/ATAPI-7 V3)

1 Scope

This part of ISO/IEC 24739 specifies the connectors and cables for physical interconnection between host and storage device, the electrical and logical characteristics of the interconnecting signals, and the protocols for the transporting of commands, data, and status over the interface for the serial interface.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

The provisions of the referenced specifications other than ISO/IEC, IEC, ISO and ITU documents, as identified in this Clause, are valid within the context of this International Standard. The reference to a specification within this International Standard does not give it any further status within ISO/IEC. In particular, it does not give the referenced specification the status of an International Standard.

ISO/IEC 14776-331, *Information technology – Small computer system interface (SCSI) – Part 331: Stream Commands (SSC)*¹

ISO 7779:1999, *Acoustics – Measurement of airborne noise emitted by information technology and telecommunications equipment*

ANSI INCITS 317-1998 (R2003) *AT Attachment with Packet Interface Extension (ATA/ATAPI-4)*

3 Terms and definitions, abbreviations and conventions

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

3.1.1

ASCII character

8-bit value that is encoded using the ASCII character set

3.1.2

acoustics

measurement of airborne noise emitted by information technology and telecommunications equipment

[ISO 7779:1999(E)]

3.1.3

ATA

AT attachment

physical, electrical, transport and command protocols for the internal attachment of storage devices to host systems

¹ See also ANSI INCITS 335-2000 (PACKET command feature set commands)

3.1.4**ATA/ATAPI-4 device**

device that complies with ANSI INCITS 317-1998, AT Attachment Interface with Packet Interface Extensions-4

3.1.5**ATA/ATAPI-5 device**

device that complies with ANSI INCITS 340-2000, the AT Attachment with Packet Interface-5

3.1.6**ATA/ATAPI-6 device**

device that complies with ANSI INCITS 361-2002, the AT Attachment with Packet Interface-6

3.1.7**ATA/ATAPI-7 device**

device that complies with the ISO/IEC 24739 series

3.1.8**ATAPI device****AT attachment packet interface device**

device implementing the packet command feature set

3.1.9**allocation unit****AU**

minimum number of logically contiguous sectors on the media as used in the streaming feature set

NOTE An Allocation Unit may be accessed with one or more requests.

3.1.10**audio-video****AV**

audio-video applications use data that is related to video images and/or audio; the distinguishing characteristic of this type of data is that accuracy is of lower priority than timely transfer of the data

3.1.11**backchannel**

receive channel when transmitting an FIS

3.1.12**bit error rate****BER**

statistical probability of a transmitted encoded bit being erroneously received in a communication system

3.1.13**bus release**

for devices implementing overlap, the term bus release is the act of clearing both DRQ and BSY to zero before the action requested by the command is completed; this allows the host to select the other device or deliver another queued command

3.1.14**byte count**

value placed in the byte count register by the device to indicate the number of bytes to be transferred during this DRQ assertion when executing a PACKET PIO data transfer command

3.1.15**byte count limit**

value placed in the byte count register by the host as input to a PACKET PIO data transfer command to specify the maximum byte count that may be transferred during a single DRQ assertion

3.1.16

CompactFlash™ Association CFA

association which created the specification for compact flash memory that uses the ATA interface

3.1.17

check condition

for devices implementing the PACKET command feature set, this indicates an error or exception condition has occurred

3.1.18

cylinder-head-sector CHS

obsolete method of addressing the data on the device by cylinder number, head number and sector number

3.1.19

code violation

in a serial interface implementation, a code violation is an error that occurs in the decoding of an encoded character (see Clause 15)

3.1.20

command aborted

command completion with ABRT set to one in the error register and ERR set to one in the status register

3.1.21

command acceptance

a command is considered accepted whenever the currently selected device has the BSY bit cleared to zero in the status register and the host writes to the command register

NOTE An exception exists for the DEVICE RESET command (see ISO/IEC 24739-1:2009, Clause 6). In a serial implementation, command acceptance is a positive acknowledgment of a host to device register FIS.

3.1.22

command block registers

interface registers used for delivering commands to the device or posting status from the device

NOTE In a serial implementation, the command block registers are FIS payload fields.

3.1.23

command completion

completion by the device of the action requested by the command or the termination of the command with an error, the placing of the appropriate error bits in the error register, the placing of the appropriate status bits in the status register, the clearing of both BSY and DRQ to zero and Interrupt Pending

3.1.24

command packet

data structure transmitted to the device during the execution of a PACKET command that includes the command and command parameters

3.1.25

command released

when a device supports overlap or queuing, a command is considered released when a bus release occurs before command completion

3.1.26

control block registers

in a parallel implementation, interface registers used for device control and to post alternate status; in a serial interface implementation, the logical field of a FIS corresponding to the device register bits of a parallel implementation

3.1.27**control character**

in a serial interface implementation, an encoded character that represents a non-data byte (see Clause 15)

3.1.28**cyclical redundancy check****CRC**

means used to check the validity of certain data transfers

3.1.29**cylinder high register**

name used for the LBA high register in previous ATA/ATAPI standards

3.1.30**cylinder low register**

name used for the LBA mid register in previous ATA/ATAPI standards

3.1.31**data character**

in a serial interface implementation, an encoded character that represents a data byte (see Clause 15)

3.1.32**data-in**

protocol that moves data from the device to the host

NOTE These transfers are initiated by READ commands.

3.1.33**data-out**

protocol that moves data from the host to the device

NOTE These transfers are initiated by WRITE commands.

3.1.34**delayed LBA**

any sector for which the performance specified by the streaming performance parameters log is not valid

3.1.35**device**

storage peripheral

NOTE Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided the device adheres to this standard.

3.1.36**device selection**

in a parallel implementation, a device is selected when the DEV bit of the device register is equal to the device number assigned to the device by means of a device 0/device 1 jumper or switch, or use of the CSEL signal

NOTE In a serial implementation the device ignores the DEV bit, the host adapter may use this bit to emulate device selection.

3.1.37**disparity**

difference between the number of ones and the number of zeroes in an encoded character (see Clause 15)

3.1.38**DMA (direct memory access) data transfer**

means of data transfer between device and host memory without host processor intervention

3.1.39

don't care

term to indicate that a value is irrelevant for the particular function described

3.1.40

driver

active circuit inside a device or host that sources or sinks current to assert or negate a signal on the bus

3.1.41

DRQ data block

unit of data words transferred during a single assertion of DRQ when using PIO data transfer

3.1.42

elasticity buffer

in a serial interface implementation, a portion of the receiver where character slipping and/or character alignment is performed

3.1.43

encoded character

in a serial interface implementation, the output of the 8b/10b encoder (see Clause 15)

3.1.44

first party DMA access

method by which a device accesses host memory

NOTE First party DMA differs from DMA in that the device sends a DMA setup FIS to select host memory regions; whereas for DMA the host configures the DMA controller.

3.1.45

frame information structure

FIS

data structure; it is the payload of a frame and does not include the SOF primitive, CRC and EOF primitive

3.1.46

frame

unit of information exchanged between the host adapter and a device

NOTE A frame consists of an SOF primitive, a Frame Information Structure, a CRC calculated over the contents of the FIS and an EOF primitive.

3.1.47

forced unit access

FUA

requires that user data be transferred to or from the device media before command completion even if caching is enabled

3.1.48

Gen1 DWORD time

the time it takes to transmit a 40 bit encoded value at 1,5 Gbit/s

3.1.49

host

computer system executing the software BIOS and/or operating system device driver controlling the device and the adapter hardware for the ATA interface to the device

3.1.50

host adapter

implementation of the host transport, link and physical layers

3.1.51

interrupt pending

in a parallel implementation, an internal state of a device;

in this state, the device asserts INTRQ if nIEN is cleared to zero and the device is selected (see ISO/IEC 24739-2:2010, Clause 8);
in a serial implementation, the Interrupt Pending state is an internal state of the host adapter; this state is entered by reception of a FIS with the I field set to one (see Clause 16)

3.1.52

logical block address (LBA)

addressing of data on the device by the linear mapping of sectors

3.1.53

linear feedback shift register (LFSR)

(see Clause 15)

3.1.54

link

the link layer manages the phy layer to achieve the delivery and reception of frames (see Clause 15)

3.1.55

logical sector

a uniquely addressable set of 256 words (512 bytes)

3.1.56

native max address

the highest address a device accepts in the factory default condition, that is, the highest address that is accepted by the SET MAX ADDRESS command

3.1.57

overlap

a protocol that allows devices that require extended command time to perform a bus release so that commands may be executed by the other device (if present) on the bus

3.1.58

packet delivered command

command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters; see also register delivered command

3.1.59

PHY

physical layer electronics, see Clause 14

3.1.60

physical sector

group of contiguous logical sectors that are read from or written to the device media in a single operation

3.1.61

programmed input/output data transfer

PIO data transfer

transfers performed by the host processor utilizing accesses to the data register

3.1.62

primitive

in a serial interface implementation, a single DWORD of information that consists of a control character in byte 0 followed by three additional data characters in byte 1 through 3

3.1.63

queued

command queuing allows the host to issue concurrent commands to the same device

NOTE Only commands included in the Overlapped feature set may be queued. In this standard, the queue contains all commands for which command acceptance has occurred, but command completion has not occurred.

3.1.64

read command

command that causes the device to transfer data from the device to the host (e.g., READ SECTOR(S), READ DMA, etc.)

3.1.65

register

register may be a physical hardware register or a logical field

3.1.66

register delivered command

command that is delivered to the device by placing the command and all of the parameters for the command in the device command block registers

NOTE See also packet delivered command.

3.1.67

register transfers

host reading and writing any device register except the data register; register transfers are 8 bits wide

3.1.68

released

in a parallel interface implementation, indicates that a signal is not being driven

NOTE For drivers capable of assuming a high-impedance state, this means that the driver is in the high-impedance state. For open-collector drivers, the driver is not asserted.

3.1.69

sector

uniquely addressable set of 256 words (512 bytes)

3.1.70

sector number register

LBA low register in previous ATA/ATAPI standards

3.1.71

shadow command block

in a serial interface implementation, a set of virtual fields in the host adapter that map the command block registers defined at the command layer to the fields within the FIS content

3.1.72

shadow control block

in a serial interface implementation, a set of virtual fields in the host adapter that map the control block registers defined at the command layer to the fields within the FIS content

3.1.73

signature

unique set of values placed in the command block registers by the device to allow the host to distinguish devices implementing the PACKET command feature set from those devices not implementing the PACKET command feature set

3.1.74

self-monitoring, analysis and reporting technology

SMART

for prediction of device degradation and/or faults

3.1.75

transport

transport layer manages the lower layers (link and phy) as well as constructing and parsing FISs, see Clause 16

3.1.76**ultra DMA burst**

the period from an assertion of DMACK– to the subsequent negation of DMACK– when an ultra DMA transfer mode has been enabled by the host

3.1.77**unaligned write**

write command that does not start at the first logical sector of a physical sector or does not end at the last logical sector of a physical sector

3.1.78**unit attention condition**

state that a device implementing the PACKET command feature set maintains while the device has asynchronous status information to report to the host

3.1.79**unrecoverable error**

when the device sets either the ERR bit or the DF bit to one in the status register at command completion

3.1.80**vendor specific (VS)**

bits, bytes, fields and code values that are reserved for vendor specific purposes

NOTE 1 These bits, bytes, fields and code values are not described in this standard and they may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE 2 Industry practice could result in conversion of a Vendor Specific bit, byte, field or code value into a defined standard value in a future standard.

3.1.81**write command**

command that causes the device to transfer data from the host to the device (e.g., WRITE SECTOR(S), WRITE DMA, etc.)

3.1.82**world wide name (WWN)**

64-bit worldwide unique name based upon a company's IEEE identifier, (see IDENTIFY DEVICE Words 108 to 111 in ISO/IEC 24739-1:2009, Clause 6.)

3.2 Abbreviations

ABRT	Abort
a/r	As Required
BSY	Busy
C/D	Command/Data
CFA	Compact Flash Association
DASP	Drive Active / Slave Present
DD	Device Data
DEV	Device
DF	Device fault
DF/SE	Device Fault / Stream Error
DIOW	Device Input Output Write
DMA	Direct Memory Access
DMACK	DMA acknowledge
DMARQ	DMA request
DRDY	Device ready
DRQ	Date Request
ECC	Error Correcting Code

ENB	Enable
ERR	Error
ERR/CHK	Error check
FIFO	First in / First Out
HOB	High Order Bit
ID	Identification
INTRQ	Interrupt Request
I/O	Input / Output
LBA	Logical Block Address
na	Not Aplicable
nIEN	Negative Interrupt Enable
NM	No media
NOP	No Operation
obs	Obsolete
OVL	Overlap
PDIAG	Passed Diagnostics
PIO	programmed input/output
REL	Release
R/W	Read / Write
SERV	Service
SRST	Soft Reset

3.3 Conventions

3.3.1 General

Lowercase is used for words having the normal English meaning. Certain words and terms used in this standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in Clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.3.7 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., LBA Mid register).

The expression "word n" or "bit n" shall be interpreted as indicating the content of word n or bit n.

3.3.2 Precedence

If there is a conflict between text, figures and tables, the precedence shall be tables, figures, then text.

3.3.3 Lists

Ordered lists, those lists describing a sequence, are of the form:

- a)
- b)
- c)

Unordered list are of the form:

- 1)
- 2)
- 3)

3.3.4 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

expected

A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

mandatory

A keyword indicating items to be implemented as defined by this standard.

may

Indicates flexibility of choice with no implied preference.

obsolete

Indicates that the designated bits, bytes, words, fields and code values that may have been defined in previous standards are not defined in this standard and shall not be reclaimed for other uses in future standards. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility.

Obsolete commands should not be used by the host. Commands defined as obsolete may be commands aborted by devices conforming to this standard. However, if a device does not command abort an obsolete command, the minimum that is required by the device in response to the command is command completion.

optional

Describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, the feature shall be implemented in the way defined by the standard.

prohibited

indicates that an item shall not be implemented by an implementation

reserved

indicates reserved bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be cleared to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as a command parameter error and reported by returning command aborted

retired

indicates that the designated bits, bytes, words, fields, and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards. If retired bits, bytes, words, fields, or code values are used before they are reclaimed, they shall have the meaning or functionality as described in previous standards

shall

indicates a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other products that conform to this standard.

should

indicates flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”

3.3.5 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

3.3.6 Signal conventions

Signal names are shown in all uppercase letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates the signal is a low active signal. A low active signal is true when the signal is below V_{iL} , and is false when the signal is above V_{iH} . No dash at the end of a signal name indicates the signal is a high active signal. A high active signal is true when the signal is above V_{iH} , and is false when the signal is below V_{iL} .

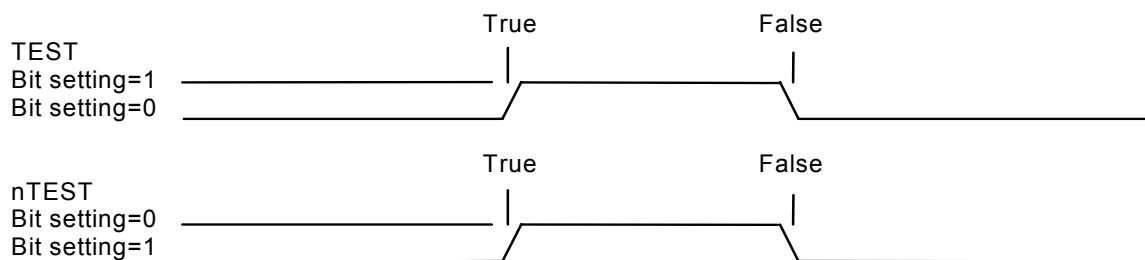
Asserted means that the signal is driven by an active circuit to the true state. Negated means that the signal is driven by an active circuit to the false state. Released means that the signal is not actively driven to any state (see ISO/IEC 24739-2:2010, Clause 7). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive functions are identified with their function names separated by a colon (e.g., DIOW:-STOP).

SIGNAL(n:m) denotes a set of signals, for example, DD(15:0).

3.3.7 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.



Bit (n:m) denotes a set of bits, for example, bits (7:0).

3.3.8 State diagram conventions

State diagrams are as shown in Figure 2.

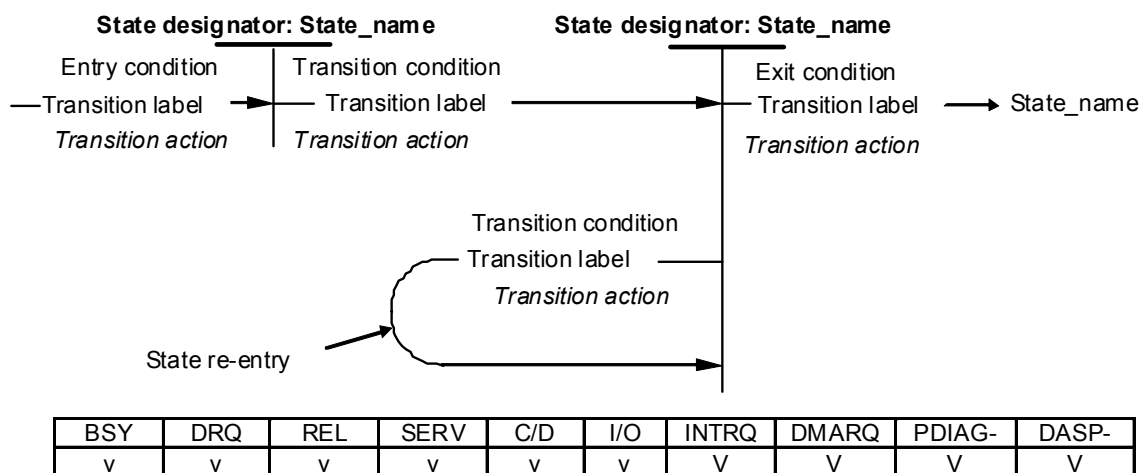


Figure 2 – State diagram convention

Each state is identified by a state designator and a state name. The state designator is unique among all states in all state diagrams in this document. The state designator consists of a set of letters that are capitalized in the title of the figure containing the state diagram followed by a unique number. The state name is a brief description of the primary action taken during the state, and the same state name may appear in other state diagrams. If the same primary function occurs in other states in the same state diagram, they are designated with a unique letter at the end of the name. Additional actions may be taken while in a state and these actions are described in the state description text.

In device command protocol state diagrams, the state of bits and signals that change state during the execution of this state diagram are shown under the state designator:state_name, and a table is included that shows the state of all bits and signals throughout the state diagram as follows:

- v = bit value changes.
- 1 = bit set to one.
- 0 = bit cleared to zero.
- x = bit is don't care.
- V = signal changes.
- A = signal is asserted.
- N = signal is negated.
- R = signal is released.
- X = signal is don't care.

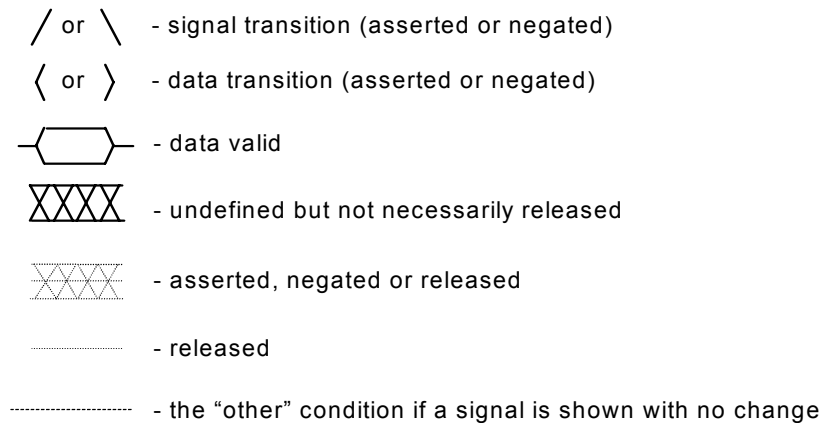
Each transition is identified by a transition label and a transition condition. The transition label consists of the state designator of the state from which the transition is being made followed by the state designator of the state to which the transition is being made. In some cases, the transition to enter or exit a state diagram may come from or go to a number of state diagrams, depending on the command being executed. In this case, the state designator is labeled xx. The transition condition is a brief description of the event or condition that causes the transition to occur and may include a transition action, indicated in italics, that is taken when the transition occurs. This action is described fully in the transition description text.

Upon entry to a state, all actions to be executed in that state are executed. If a state is re-entered from itself, all actions to be executed in the state are executed again.

Transitions from state to state shall be instantaneous.

3.3.9 Timing conventions

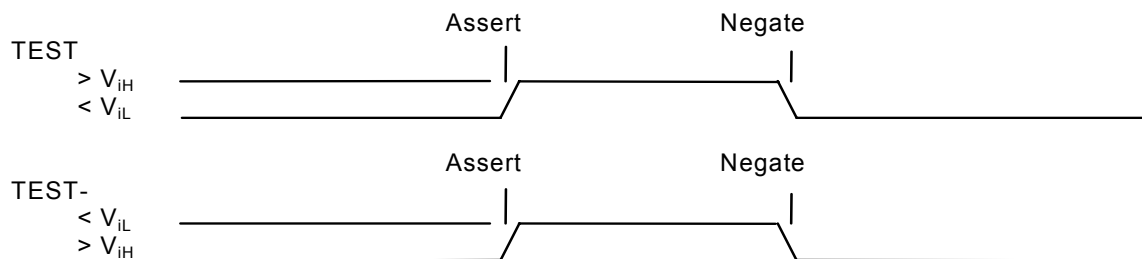
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.



All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



3.3.10 Byte ordering for data transfers

Data is transferred in blocks using either PIO or DMA protocols. PIO data transfers occur when the BSY bit is cleared to zero and the DRQ bit is set to one. These transfers are usually 16-bit but CFA devices may implement 8-bit PIO transfers. Data is transferred in blocks of one or more bytes known as a DRQ block. DMA data transfers occur when the host asserts DMACK- in response to the device asserting DMARQ. DMA transfers are always 16-bit. Each assertion of DMACK- by the host defines a DMA data burst. A DMA data burst is two or more bytes.

Assuming a DRQ block or a DMA burst of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block, and Byte(n-1) is the last byte of the block. Table 2 shows the order the bytes shall be presented when such a block of data is transferred on the interface using 16-bit PIO and DMA transfers. Table 3 shows the order the bytes shall be presented in when such a block or burst of data is transferred on the interface using 8-bit PIO.

Table 2 – 16-bit Transfer Byte order

	DD 15	DD 14	DD 13	DD 12	DD 11	DD 10	DD 9	DD 8	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (<i>n</i> -1)								Byte (<i>n</i> -2)							

Table 3 – 8-bit Transfer Byte order

	DD 7	DD 6	DD 5	DD 4	DD 3	DD 2	DD 1	DD 0
First transfer	Byte (0)							
Second transfer	Byte (1)							
.....								
Last transfer	Byte (<i>n</i> -1)							

NOTE The above description is for data on the interface. Host systems and/or host adapters may cause the order of data as seen in the memory of the host to be different.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only code values 20h through 7Eh. For the string "Copyright", the character "C" is the first byte, the character "o" is the second byte, etc. When such fields are transferred, the order of transmission is:

the 1st character ("C") is on DD(15:8) of the first word,
the 2nd character ("o") is on DD(7:0) of the first word,
the 3rd character ("p") is on DD(15:8) of the second word,
the 4th character ("y") is on DD(7:0) of the second word,
the 5th character ("r") is on DD(15:8) of the third word,
the 6th character ("i") is on DD(7:0) of the third word,
the 7th character ("g") is on DD(15:8) of the fourth word,
the 8th character ("h") is on DD(7:0) of the fourth word,
the 9th character ("t") is on DD(15:8) of the fifth word,
the 10th character ("space") is on DD(7:0) of the fifth word,
etc.

Word (*n*:*m*) denotes a set of words, for example, words (103:100).

Byte, word and DWORD relationships.

Figure 3 illustrates the relationship between bytes, words and DWORDs.

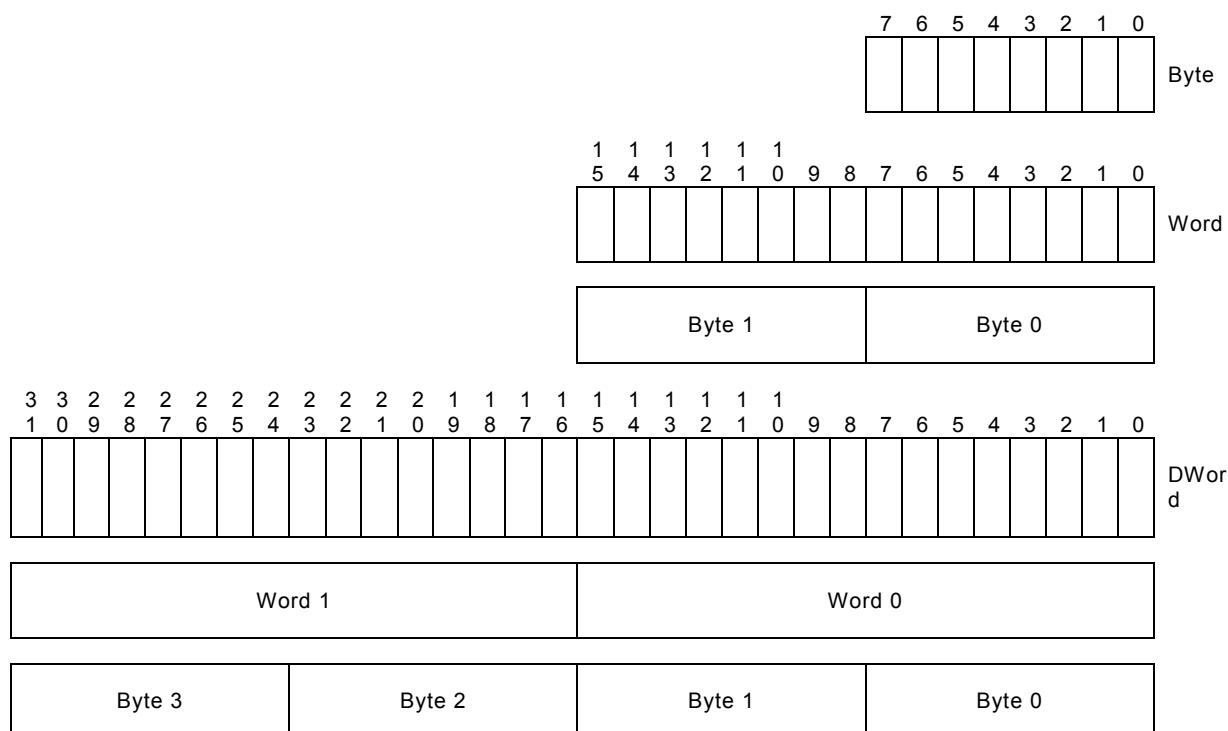


Figure 3 – Byte, word and DWORD relationships

4 General operational requirements

Refer to Clause 4 of ISO/IEC 24739-1:2009 for general operational requirements.

5 I/O register descriptions

Refer to Clause 5 of ISO/IEC 24739-1:2009 for I/O register. In addition, see also Clauses 10 and 11 of ISO/IEC 24739-2.

6 Command descriptions

Refer to Clause 6 of ISO/IEC 24739-1:2009 for command descriptions.

7 Parallel interface physical and electrical requirements

Refer to Clause 7 of ISO/IEC 24739-2:2009 for parallel interface physical and electrical requirements.

8 Parallel interface signal assignments and descriptions

Refer to Clause 8 of ISO/IEC 24739-2:2009 for parallel interface signal assignments and descriptions.

9 Parallel interface general operating requirements of the physical, data link, and transport layers

Refer to Clause 9 of ISO/IEC 24739-2:2009 for parallel interface general operating requirements of the physical, data link, and transport layers.

10 Parallel interface register addressing

Refer to Clause 10 and Clause 11 of ISO/IEC 24739-2 for parallel interface register addressing.

11 Parallel interface transport protocols

Refer to Clause 11 of ISO/IEC 24739-2:2010 for parallel interface transport protocols.

12 Parallel interface timing

Refer to Clause 12 of ISO/IEC 24739-2:2010 for parallel interface timing.

13 Serial interface general overview

13.1 Overview

The serial implementation of ATA is a high-speed serial replacement for the parallel implementation of ATA attachment of mass storage devices. The serial interface employed is a high-speed differential layer that utilizes Gigabit technology and 8b/10b encoding.

Figure 4 illustrates how two devices are connected to a Parallel ATA host adapter. This method allows up to two devices to be connected to a single port using a Device 0/Device 1 communication technique. Each device is connected via a ribbon cable that “daisy chains” the devices.

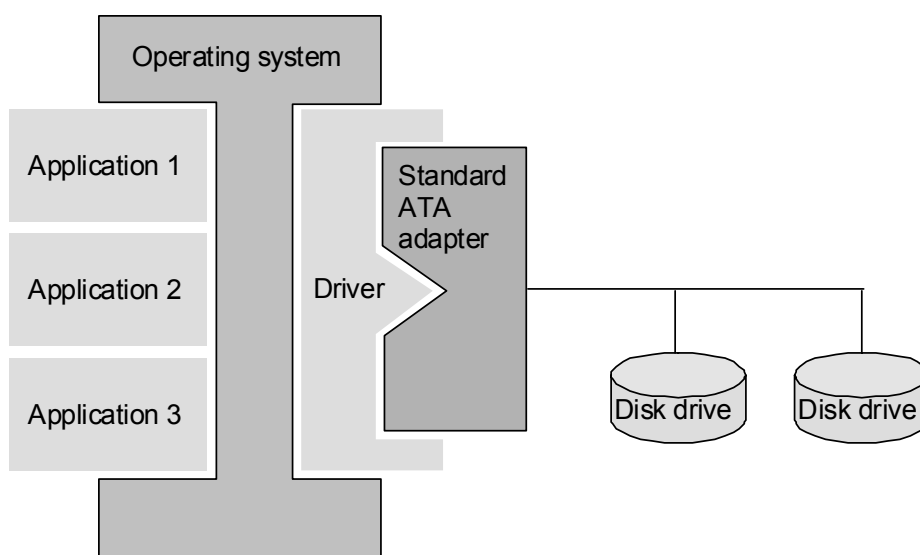


Figure 4 – Standard ATA device connectivity

Figure 5 illustrates how the same two devices are connected using a serial implementation of an ATA host adapter. In this diagram the dark grey portion is functionally similar to the dark grey portion of the previous diagram. ATA host software accesses the serial implementation of ATA subsystem in the same manner and functions in the same way as previous parallel implementation definitions. In this case, however, the software views the two devices as if they were both Device 0 on two separate ports. The right hand portion of the host adapter is of a new design that converts the operations of the software into a serial data/control stream. The serial interface structure connects each of the two drives with their own respective cables in a point-to-point fashion.

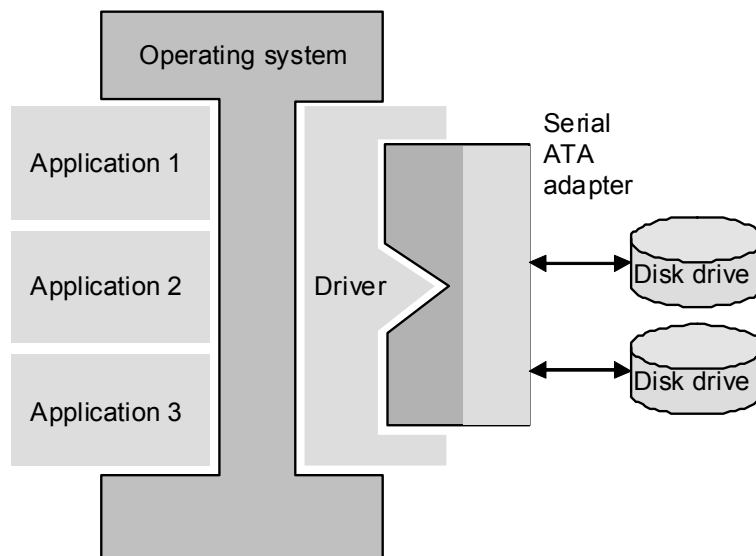


Figure 5 – The serial implementation of ATA connectivity

13.2 Sub-module operation

The Transport control state machine and the Link state machine are the two core sub-modules that control overall operation. The Link state machine controls the operation(s) related to the serial line and the Transport control state machine controls the operation(s) relating to the host platform. The two state machines coordinate their actions and utilize resources to transfer data between a host computer and attached mass storage device. The host Link state machine communicates via the serial line to a corresponding Link state machine located in the device. The host Transport machine also likewise communicates with a corresponding device Transport state machine. The two Link state machines ensure that control sequences between the two Transport control state machines are properly exchanged. Figure 6 shows how the machines communicate their various needed parameters in the traditional layered model. Each layer communicates with its counterpart directly or indirectly.

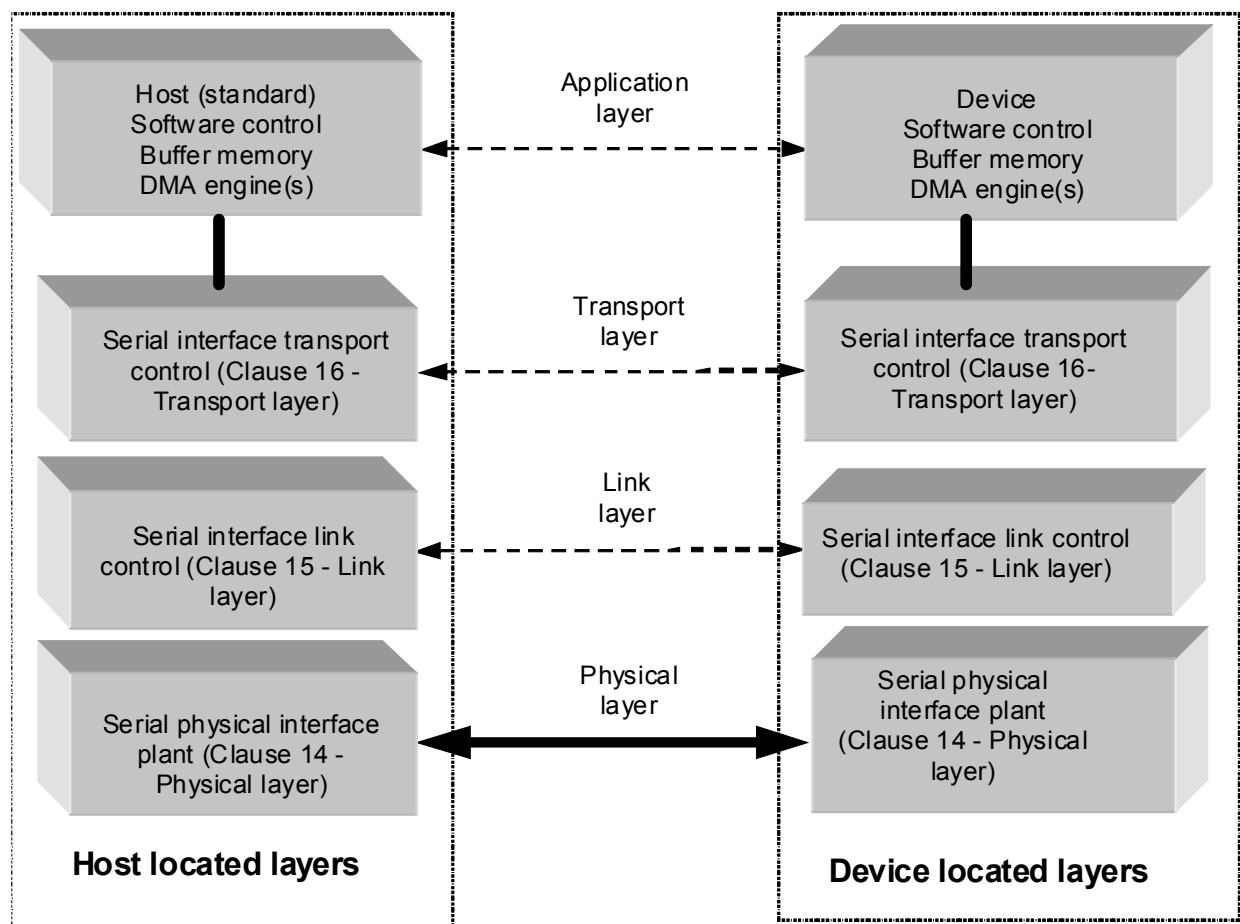


Figure 6 – Communication layers

The host interacts with the Transport control state machine through a register interface that is equivalent to that presented by a parallel implementation of an ATA host adapter. This allows host software to follow existing standards and conventions when accessing the register interface and follows standard command protocol conventions. The Transport control state machine breaks down these operations into a sequence of actions that are exchanged with the Link state machine.

13.3 Parallel ATA emulation

This subclause is optional.

13.3.1 General

See Clause 18 for state diagrams.

See 18.2 for additional information about nIEN.

Emulation of parallel implementations of ATA device behavior as perceived by the host BIOS or software driver, is a cooperative effort between the device and a serial interface host adapter hardware. The behavior of Command and Control Block registers, PIO and DMA data transfers, resets and interrupts are all emulated.

The host adapter contains a set of registers that Shadow the contents of the traditional device registers, referred to as the Shadow Command Block and Shadow Control Block. The Command Block registers are used for sending commands to the device or posting status from the device. These registers include the LBA High, LBA Mid, Device, Sector Count, Command, Status, Features, Error and Data registers. The Control Block registers are used

for device control and to post alternate status. These registers include the Device Control and Alternate Status registers.

All serial implementations of ATA devices behave like Device 0 devices. Devices shall ignore the DEV bit in the Device field of received Register FISes, and it is the responsibility of the host adapter to gate transmission of Register FISes to devices, as appropriate, based on the value of the DEV bit.

After a reset or power-on, the host bus adapter emulates the behavior of a traditional ATA system during device discovery. Immediately after reset, the host adapter shall place the value 0x7Fh in its Shadow Status register and Shadow Alternate Status Register and shall place the value 0xFFh in all the other Shadow Command Block registers (0xFFFFh in the Data register). In this state the host bus adapter shall not accept writes to the Shadow Command Block and Shadow Control Block. When the host Phy detects presence of an attached device, see 20.2.2.1 and 19.2.2, the host bus adapter shall set bit 7 in the Shadow Status register yielding the value 0xFFh or 0x80h, and the host bus adapter shall allow writes to the Shadow Command Block and Shadow Control Block. If a device is present, the Phy shall take no longer than 10 ms to indicate that it has detected the presence of a device and has set bit 7 in the Shadow Status register. The Serial implementation of ATA time limit of 10 ms is different than the parallel implementation of ATA. (See 11 of ISO/IEC 24739-2). When the attached device establishes communication with the host bus adapter, it shall send a register FIS to the host, resulting in the Shadow Command Block and Shadow Control Block being updated with values appropriate for the attached device.

The host adapter may present a Device 0-only emulation to host software, that is, each device is a Device 0, and each Device 0 is accessed at a different set of host bus addresses. The host adapter may optionally present a Device 0/Device 1 emulation to host software, that is, two devices on two separate serial ports are represented to host software as a Device 0 and a Device 1 accessed at the same set of host bus addresses.

13.3.2 Software reset

Issuing a software reset is performed by toggling the SRST bit in the Shadow Device Control register. The toggle period is no shorter than a minimum timeout (see Clause 11 of ISO/IEC 24739-2). As a result of the SRST bit changing in the Shadow Device Control register, host adapters shall issue at least two Register FISes to the device (one with the SRST bit set and a subsequent one with the SRST bit cleared). See 16.2.3.2 for a detailed definition of Register FIS. Although host software is required to toggle the SRST bit no faster than specified in parallel implementations of ATA, serial devices shall not rely on the inter-arrival time of received Register FISes also meeting this timing. Because of flow control, frame handshaking and other protocol interlocks, serial devices may receive the resulting Register FISes back-to-back.

Due to flow control, protocol interlocks, power management state, or other transmission latencies, the subsequent Register frame transmission clearing the SRST bit during a software reset may be triggered prior to the previous Register FIS transmission having been completed. Host adapters are required to allow host software to toggle the SRST with the minimum timing specified for the parallel implementation of ATA, even if frame transmission latencies result in the first Register FIS transmission taking longer than specified in the parallel implementation. Host adapters are required to ensure transmission of the two resulting Register FISes to the device regardless of the transmission latency of each individual FIS.

13.3.3 Device 0-only emulation

A serial implementation of an ATA host adapter behaves the same as if a parallel implementation Device 0 only device were attached with no Device 1 present. It is the responsibility of the host adapter to properly interact with host software and present the correct behavior for this type of configuration. All serial implementations of ATA devices, therefore, need not be aware of Device 0/Device 1 issues and ignore parallel implementation I/O register information that deals with a secondary device. When the DEV bit in the Device register is set to one, selecting the non-existent Device 1, the host adapter shall respond to register reads and writes as specified for a Device 0 with no Device 1 present, as defined in the parallel implementation. This includes not setting the BSY bit in the Shadow Status

register when Device 1 is selected, as described in the parallel implementation. When Device 0 is selected, the host adapter shall execute the serial implementation protocols for managing the Shadow Command Block and Shadow Control Block contents as defined in Clause 17.

When Device 0 is selected and the Command register is written in the Shadow Command Block, the host adapter sets the BSY bit in its Shadow Status register. The host adapter then transmits a frame to the device containing the new Control and Command Block register contents. When the Device Control register is written in the Shadow Control Block with a change of state of the SRST bit, the host adapter sets the BSY bit in its Shadow Status register and transmits a frame to the device containing the new register contents. Transmission of register contents when the Device Control register is written with any value that is not a change of state of the SRST bit shall not set the BSY bit in the Shadow Status register, and transmission of a frame to the device containing new register contents is optional. Similarly, the host adapter sets the BSY bit in its Shadow Status register to one when a hard reset (COMRESET) is requested or the SRST bit is set to one in the Device Control register, see Figure 95.

The device updates the contents of the host adapter Shadow Command Block and Shadow Control Block by transmitting a register frame to the host. This allows the device to set the proper ending status in the host adapter at the completion of a command or control request. Specific support is added to ensure proper timing of the DRQ and BSY bits in the Status register for PIO transfers.

Finally the host adapter provides an Interrupt Pending flag in the host adapter. This flag is set by the host adapter when the device sends a serial bus frame including the request to set the Interrupt Pending flag. The host adapter asserts the interrupt to the host processor any time the Interrupt Pending flag is set, the DEV bit is cleared to zero in the Shadow Device register, and the nIEN bit in the Shadow Device Control register is cleared to zero. The host adapter clears the Interrupt Pending flag any time a COMRESET is requested, the SRST bit in the Shadow Device Control register is set to one, the Shadow Command register is written and DEV is cleared to zero, or the Shadow Status register is read and DEV is cleared to zero. This allows the emulation of the host interrupt and its proper timing.

13.3.4 Device 0/Device 1 emulation (optional)

13.3.4.1 General

All devices behave as if they are Device 0 devices. However, the host adapter may optionally implement emulation of the behavior of a Device 0/Device 1 configuration by pairing two serial ports, and managing their associated Shadow Command Block and Shadow Control Block accordingly, as though they were a Device 0 and Device 1 at the same set of host bus addresses.

A host adapter that emulates Device 0/Device 1 behavior shall manage the two sets of Shadow Command Block and Shadow Control Block (one set for each of the two devices) based on the value of the DEV bit in the Shadow Device register. Based on the value of the DEV bit, the host adapter shall direct accesses to the Shadow Command Block and Shadow Control Block to the appropriate set of Shadow Command Block and Shadow Control Block in the correct device. It is the responsibility of the host adapter to ensure that communication with one or both of the attached devices is handled properly, and that information gets routed to the devices correctly. Each device shall process any communication with the host adapter as if it is targeted for the device regardless of the value of the DEV bit.

If a host adapter is emulating Device 0/Device 1 behavior, and there is no device attached to the cable designated as the Device 1 cable, the host adapter shall emulate Device 0 behavior with no Device 1 present as described in the parallel implementation.

When device 1 is selected and device 0 is responding for device 1 (see Table 44 in ISO/IEC 24739-2:2009), a host adapter with Device 0/Device 1 emulation generates the non-packet device response for both packet and non-packet devices.

13.3.4.2 Software reset

Host adapters that emulate Device 0/Device 1 behavior shall emulate parallel implementation behavior for software reset. Based on the Phy initialization status, the host adapter knows whether a device is attached to each of the two ports used in a Device 0/Device 1 emulation configuration. Device Control Register writes, that have the SRST bit set to one, shall result in the associated Shadow Control Block being written for each port to which a device is attached. The frame transmission protocol for each associated port executed, results in a Register FIS being transmitted to each attached device. Similarly, the subsequent write to the Device Control register that clears the SRST bit shall result in a Register FIS being sent to each attached device. The host adapter shall then await a response from each attached device (or timeout), and shall merge the contents of the Error and Status registers for the attached devices, in accordance with the parallel implementation, to produce the Error and Status register values visible to host software.

13.3.4.3 EXECUTE DEVICE DIAGNOSTICS

Host adapters that emulate Device 0/Device 1 behavior shall emulate the parallel implementation behavior for EXECUTE DEVICE DIAGNOSTICS (see ISO/IEC 24739-1:2009, Clause 6 and ISO/IEC 24739-2:2010, Clause 11). The host adapter shall detect the EXECUTE DEVICE DIAGNOSTIC command being written to the Command register. Host adapter detection of the EXECUTE DEVICE DIAGNOSTICS command shall result in the associated Shadow Command Block and Shadow Control Block being written for each port to which a device is attached. A Register FIS is transmitted to each attached device. The host adapter shall then await a response from each attached device (or timeout), and shall merge the contents of the Error and Status registers for the attached devices, in accordance with the parallel implementation to produce the Error and Status register values visible to host software.

13.3.4.4 Restrictions and limitations

Superset capabilities that are unique to the Serial implementation of ATA and not supported by the parallel implementation of ATA are not required to be supported in Device 0/Device 1 emulation. Device 0/Device 1 emulation is recommended only in configurations where legacy software drivers are used and the number of attached devices exceeds the number of interfaces the legacy software supports.

14 Serial interface physical layer

14.1 Overview

14.1.1 General

This clause describes the physical layer of the serial implementation of ATA. Unless otherwise described, the information is normative. The information that is provided and marked informative is provided to help the reader better understand the normative clauses and should be taken as examples only. Exact implementations may vary.

14.1.2 List of services

The following services are provided.

- 1) Transmit a 1.5 Gb/s differential NRZ serial stream at specified voltage levels.
- 2) Provide matched termination at the transmitter.
- 3) Serialize a 10, 20, 40, or other width parallel input from the Link for transmission.
- 4) Receive a 1.5 Gb/s differential NRZ serial stream.
- 5) Provide a matched termination at the receiver.
- 6) Extract data (and, optionally, clock) from the serial stream.
- 7) Deserialize the serial stream.
- 8) Detect the K28.5 comma character and provide a bit and word aligned 10, 20, 40, or other width parallel output.
- 9) Provide specified OOB signal detection and transmission.
- 10) Perform proper power-on sequencing and speed negotiation.
- 11) Provide interface status to Link layer.

- 12) Host/device present.
- 13) Host/device absent.
- 14) Host/device present but failed to negotiate communications.
- 15) Optionally support power management modes.
- 16) Optionally perform transmitter and receiver impedance calibration.
- 17) Handle the input data rate frequency variation due to a spread spectrum transmitter clock.
- 18) Accommodate request to go into Far-End retimed loopback test mode of operation when commanded.

14.2 Connectors specifications

14.2.1 Overview

This clause covers the serial implementation of ATA connectors and cable assemblies. It defines the

- 1) connector mating interfaces,
- 2) connector location on the device,
- 3) electrical, mechanical and reliability requirements of the connectors and cable assemblies,
- 4) connector and cable testing procedures.

It does not define how the connector and cable assembly are implemented, such as

- 1) the mounting feature of the connectors,
- 2) the cabling and cable terminations,
- 3) the methods on how the PCB connects to other components of the system.

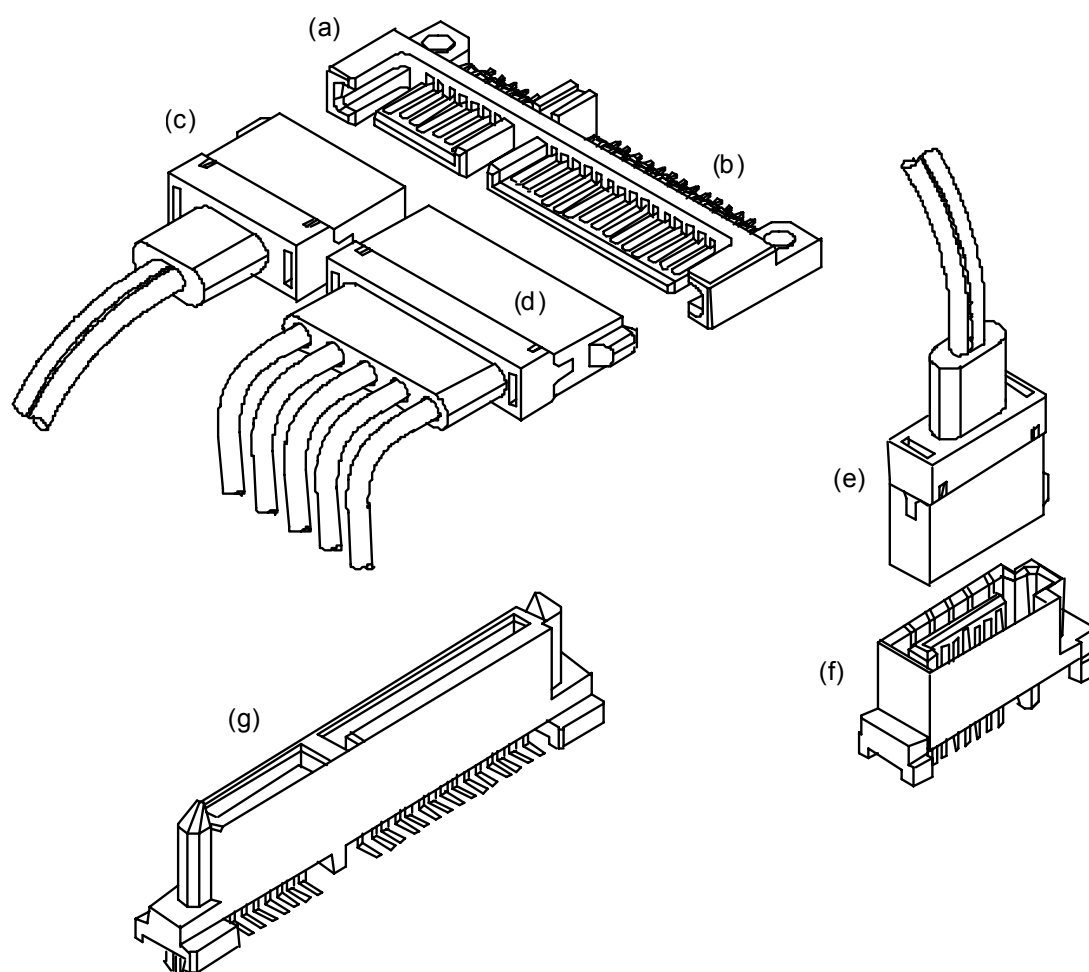
14.2.2 General descriptions

A serial implementation of an ATA device may be either directly connected to a host or connected to a host through a cable.

For direct connection, the device plug connector, shown as (a) and (b) in Figure 7, is inserted directly into a host receptacle connector, illustrated as (g) in Figure 7. The device plug connector and the host receptacle connector incorporate features that enable the direct connection to be hot pluggable and blind mateable.

For connection via cable, the device signal plug connector, shown as (a) in Figure 7, mates with the signal cable receptacle connector on one end of the cable, illustrated as (c) in Figure 7. The signal cable receptacle connector on the other end of the cable is inserted into a host signal plug connector, shown as (f) in Figure 7. The signal cable wire consists of two twinax sections in a common outer sheath.

There is also a separate power cable for the cabled connection. A Serial ATA power cable includes a power cable receptacle connector, shown as (d) in Figure 7, on one end and may be directly connected to the host power supply on the other end or may include a power cable receptacle on the other end. The power cable receptacle connector on one end of the power cable mates with the device power plug connector, shown as (b) in Figure 7. The host end of the power cable is not covered in this standard.



Components

- (a) device signal plug segment or connector;
- (b) device power plug segment or connector;
- (c) signal cable receptacle connector, to be mated with (a);
- (d) power cable receptacle connector, to be mated with (b);
- (e) signal cable receptacle connector, to be mated with (f), the host signal plug connector;
- (g) host receptacle connector mating directly with device plug connector (a) and (b).

Figure 7 – Serial implementation connector examples

14.2.3 Connector drawings

14.2.3.1 Device plug connector

Figure 8, Figure 9 and Table 4 show the interface dimensions for the device plug connector with both signal and power segments. All dimensions are in millimeters.

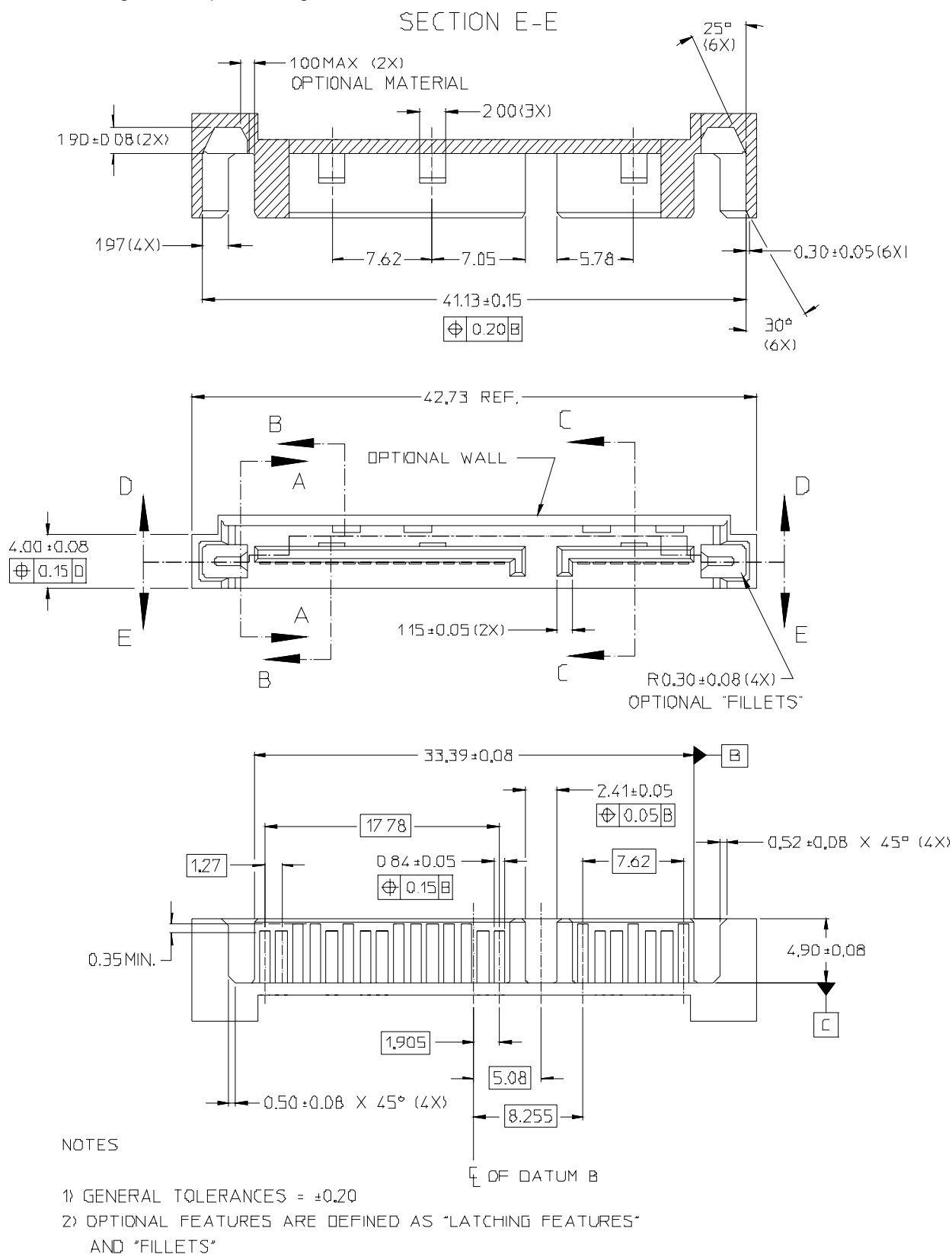
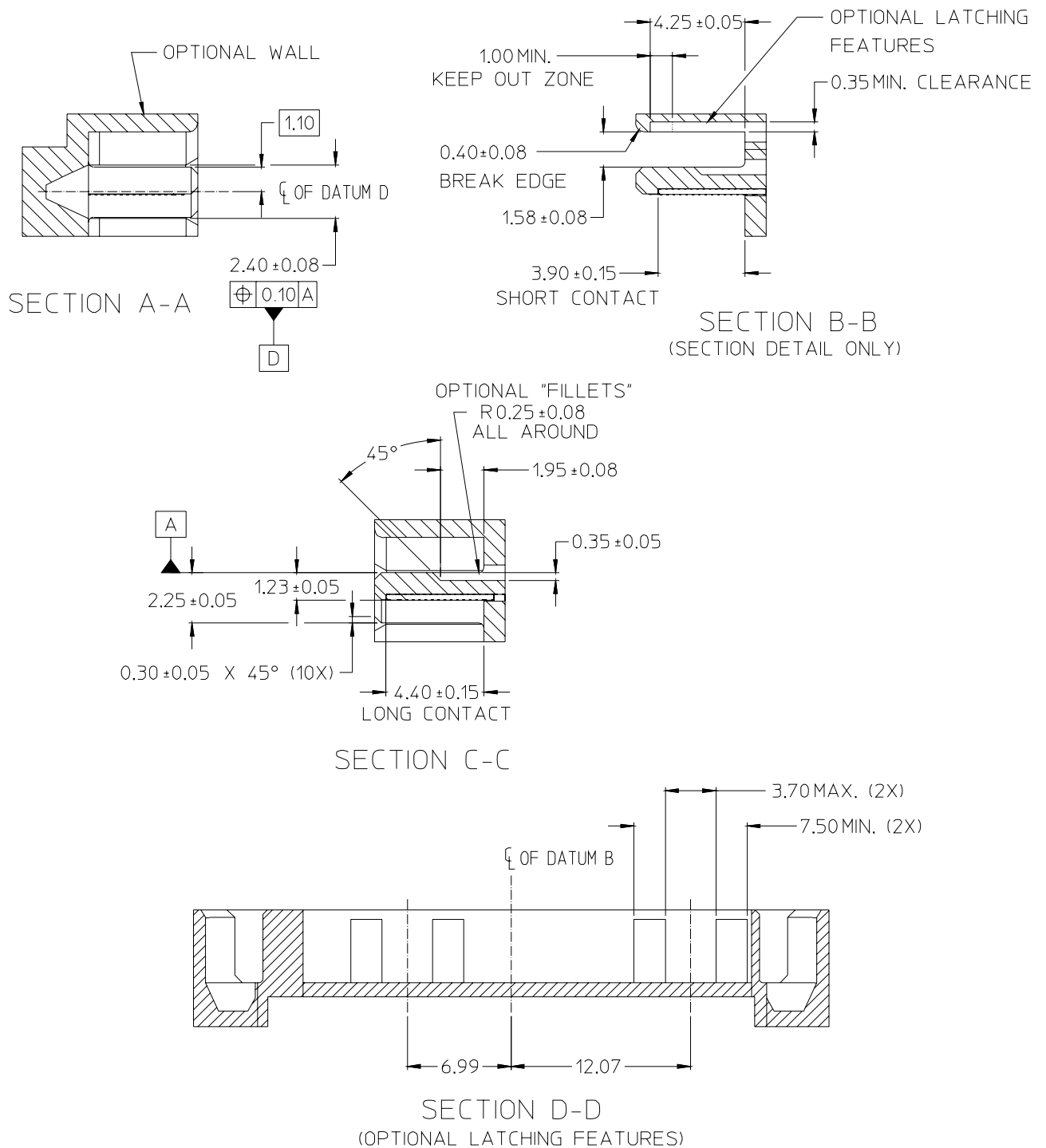


Figure 8 – Device plug connector part 1 of 2



NOTES:

- 1) GENERAL TOLERANCES = ±0.20
- 2) OPTIONAL FEATURES ARE DEFINED AS "LATCHING FEATURES" AND "FILLETS"

Figure 9 – Device plug connector part 2 of 2

14.2.3.2 Signal cable receptacle connector

Figure 10 shows the interface dimensions for the signal cable receptacle connector. There are two identical receptacles at the two ends of the Serial ATA cable assembly. The cable

receptacle mates with either the signal segment of the device plug connector on the device, or the host plug connector on the host. All dimensions are in millimeters.

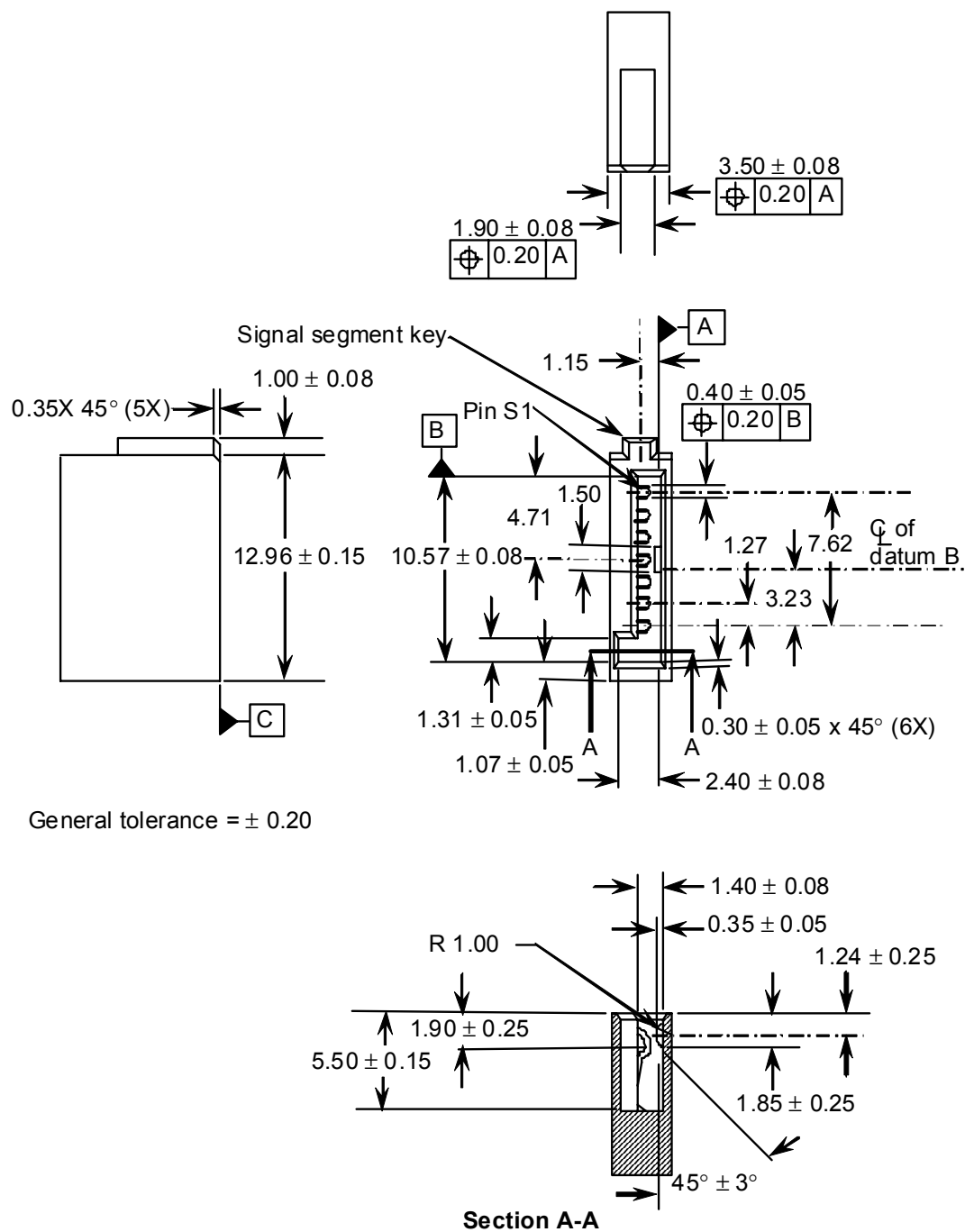


Figure 10 – Non-Latching Signal Cable receptacle connector interface dimensions

Figure 11 shows the additional dimensions for the optional Latching Signal Cable Receptacle. All dimensions are in millimeters.

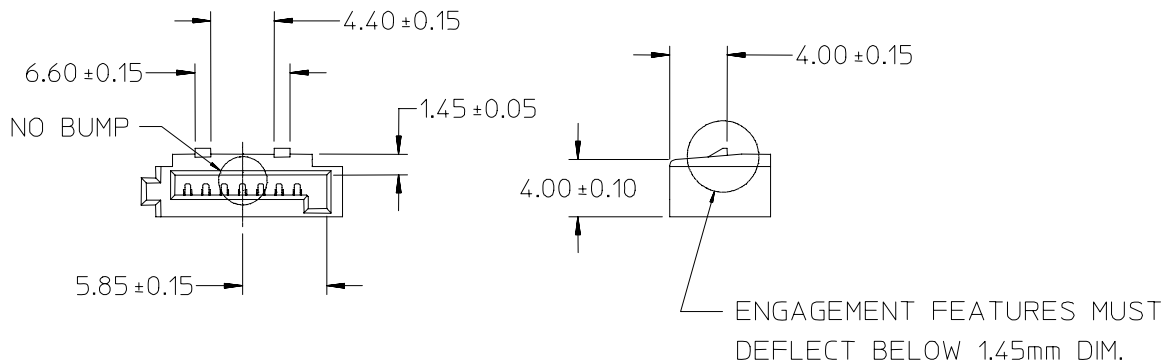


Figure 11 – Optional Latching Signal Cable Receptacle connector interface dimensions

14.2.3.3 Signal host plug connector

The signal host plug connector is to be mated with one end of the Serial ATA cable assembly. So the pinout of the host plug connector is the mirror image of the signal cable receptacle. Figure 12 shows the host plug connector interface definition.

For applications where multiple Serial ATA ports or connectors are stacked together on the host, there is a clearance or spacing requirement to prevent the cable assemblies from interfering with each other. Figure 21 shows the recommended clearance or spacing. All dimensions are in millimeters.

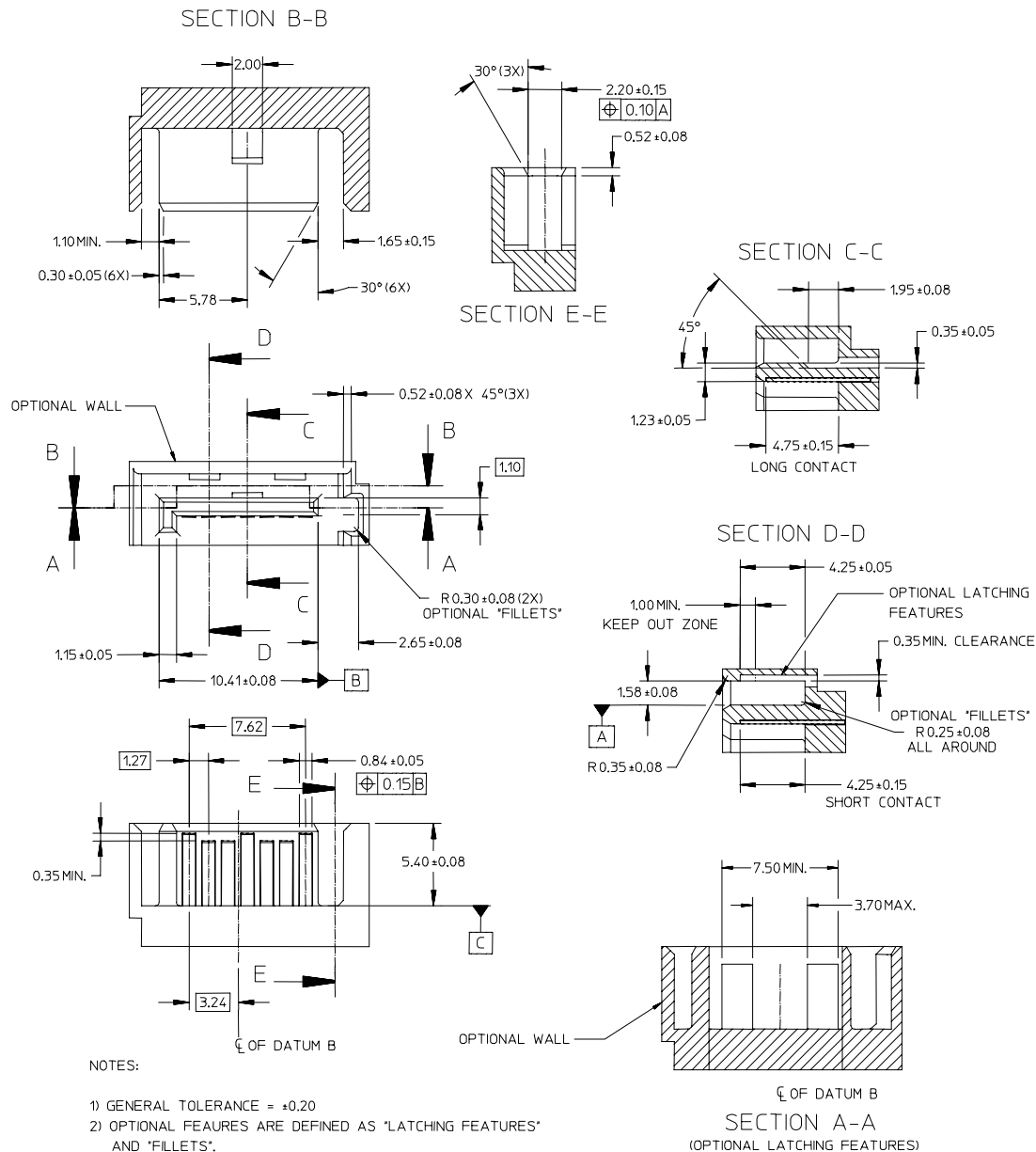


Figure 12 – Host plug connector interface dimension

14.2.3.4 Host receptacle connector

The host receptacle connector is to be blind-mated directly with the device plug connector. The interface dimensions for the host receptacle connector are shown in Figure 13. Note that dimension B allows two values: 8.15 mm and 14.15 mm. There are two levels of contacts in the host receptacle connector. The advancing ground contacts P4 and P12 mate first with the corresponding ground pins on the device plug connector, followed by the engaging of the pre-charged power pins. An appropriate external retention mechanism independent of the connector is required to keep the host PCB and the device in place and is not specified by this standard. The host receptacle connector is not designed with any retention mechanism. All dimensions are in millimeters.

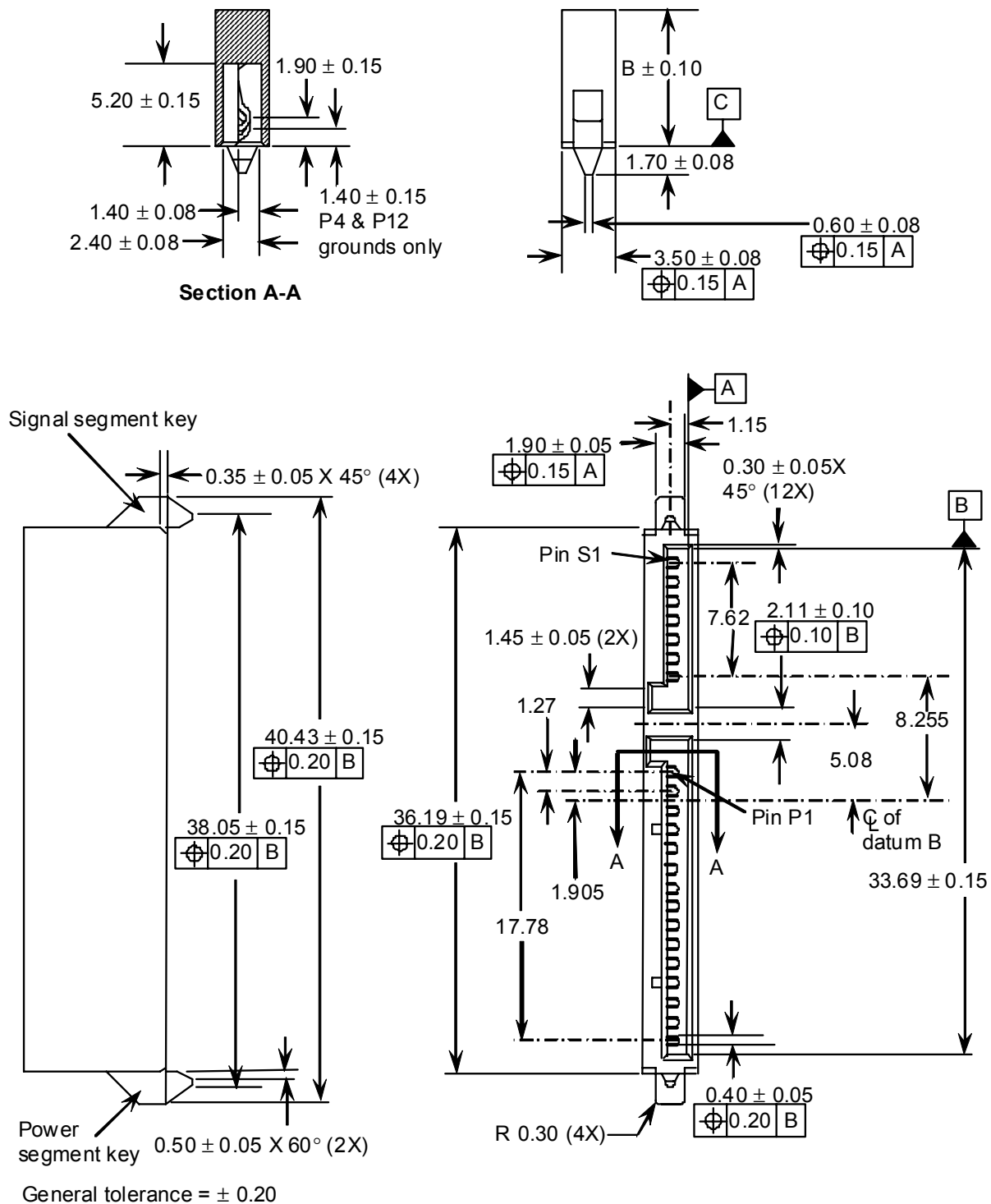


Figure 13 – Host receptacle connector interface dimensions

14.2.3.5 Power cable receptacle connector

The power cable receptacle connector mates with the power segment of the device plug, bringing power to the device. Figure 14 shows the interface dimensions of the power receptacle connector. The pinout of the connector is the mirror image of the power segment of the device plug shown in Table 4. All dimensions are in millimeters.

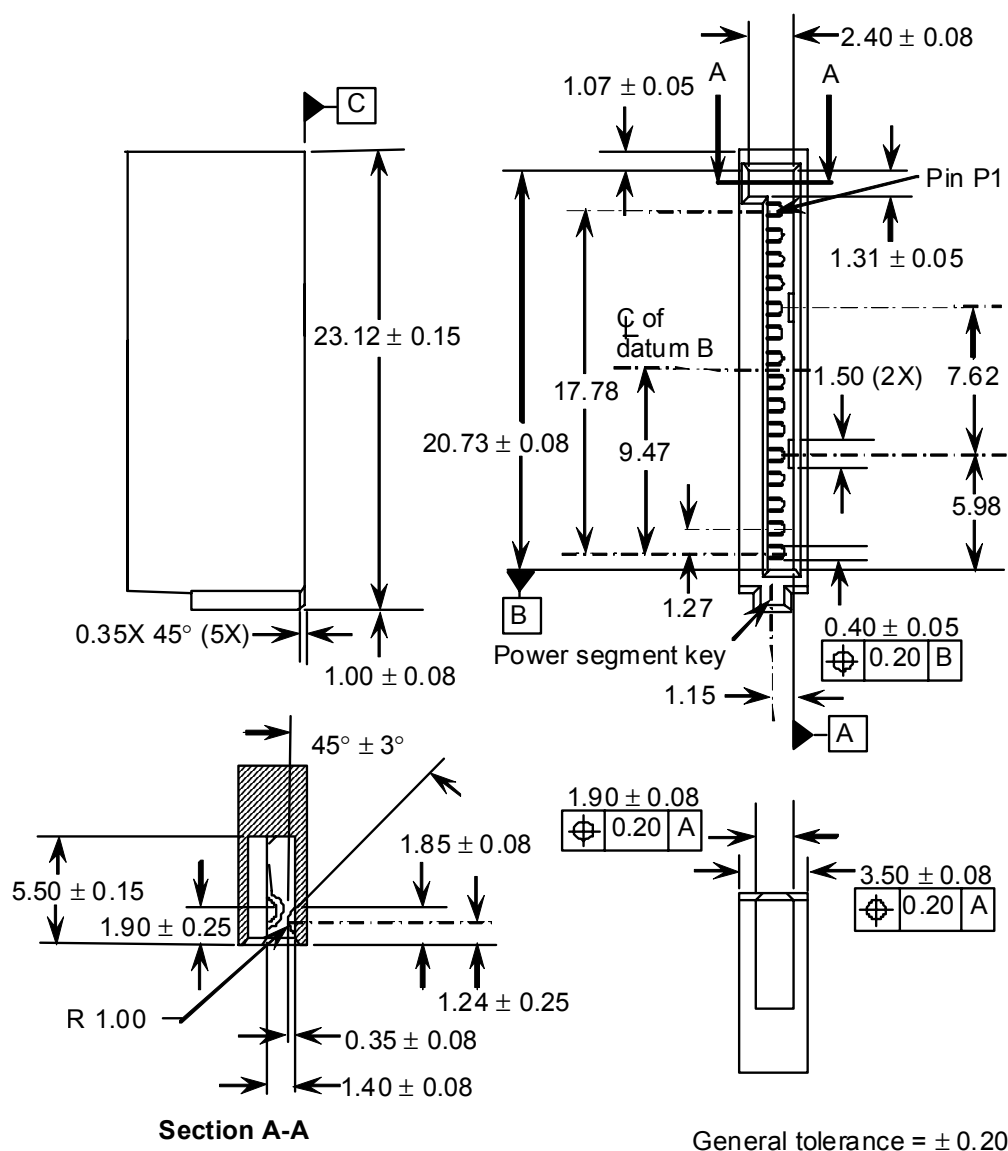


Figure 14 – Non-Latching Power cable receptacle connector interface dimensions

Figure 15 shows the dimensions for the optional latching feature for the power cable receptacle. All dimensions are in millimeters.

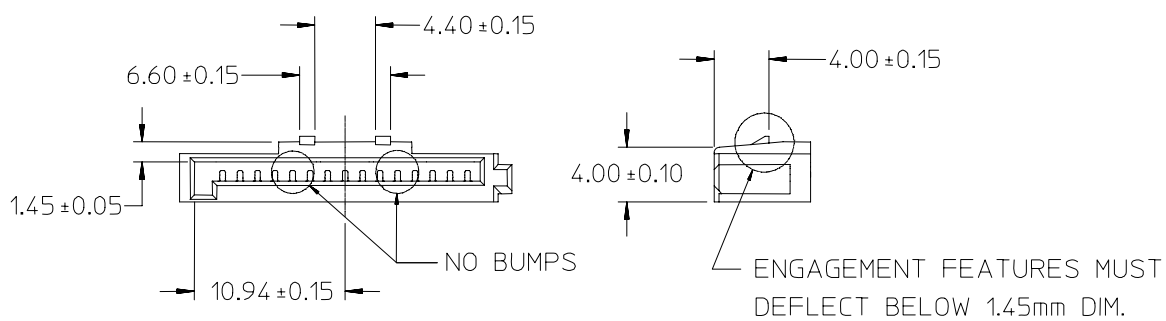


Figure 15 – Optional Latching Power Cable Receptacle

14.2.4 Connector pinouts

There are a total of 7 pins in the signal segment and 15 pins in the power segment. The pin definitions are shown in Table 4.

Table 4 – Device plug connector pin definition

Signal segment key			
Signal segment	S1	Gnd	Second mate
	S2	A+	Differential signal pair A from Phy
	S3	A-	
	S4	Gnd	Second mate
	S5	B-	Differential signal pair B from Phy
	S6	B+	
	S7	Gnd	Second mate
Signal segment “L”			
Central connector polarizer			
Power segment “L”			
Power segment	P1	V33	3.3 V power
	P2	V33	3.3 V power
	P3	V33	3.3 V power, pre-charge, second mate
	P4	Gnd	First mate
	P5	Gnd	Second mate
	P6	Gnd	Second mate
	P7	V5	5 V power, pre-charge, second mate
	P8	V5	5 V power
	P9	V5	5 V power
	P10	Gnd	Second mate
	P11	Reserved	1) The pin corresponding to P11 in the backplane receptacle connector is also reserved 2) The corresponding pin to be mated with P11 in the power cable receptacle connector shall be grounded
	P12	Gnd	First mate
	P13	V12	12 V power, pre-charge, 2nd mate
	P14	V12	12 V power
	P15	V12	12 V power
Power segment key			
NOTE 1 The comments on the mating sequence in Table 3 apply to the case of backplane blind-mate connector only. In this case, the mating sequences are: (1) the ground pins P4 and P12; (2) the pre-charge power pins and the other ground pins; and (3) the signal pins and the rest of the power pins.			
NOTE 2 There are three power pins for each voltage. One pin from each voltage is used for pre-charge in the backplane blind-mate situation.			
NOTE 3 V33 pins shall be connected together in the device.			
NOTE 4 V5 pins shall be connected together in the device.			
NOTE 5 V12 pins shall be connected together in the device.			

14.2.5 Backplane connector configuration and blind-mating tolerance

The maximum blind-mate misalignment tolerances are ± 1.50 mm and ± 1.00 mm, respectively, for two perpendicular axes illustrated in Figure 16. Any skew angle of the plug, with respect to the receptacle, reduces the blind-mate tolerances. All dimensions are in millimeters.

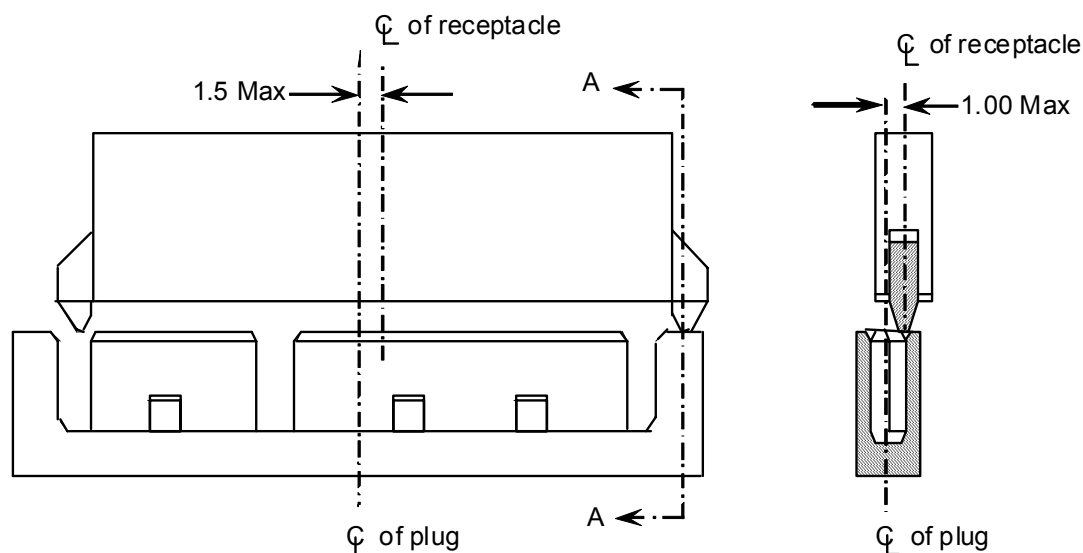


Figure 16 – Connector pair blind-mate misalignment tolerance

The device-to-backplane mating configuration is shown in Figure 17. Note that two values (8.45 and 14.45 mm) are allowed for dimension A. All dimensions are in millimeters.

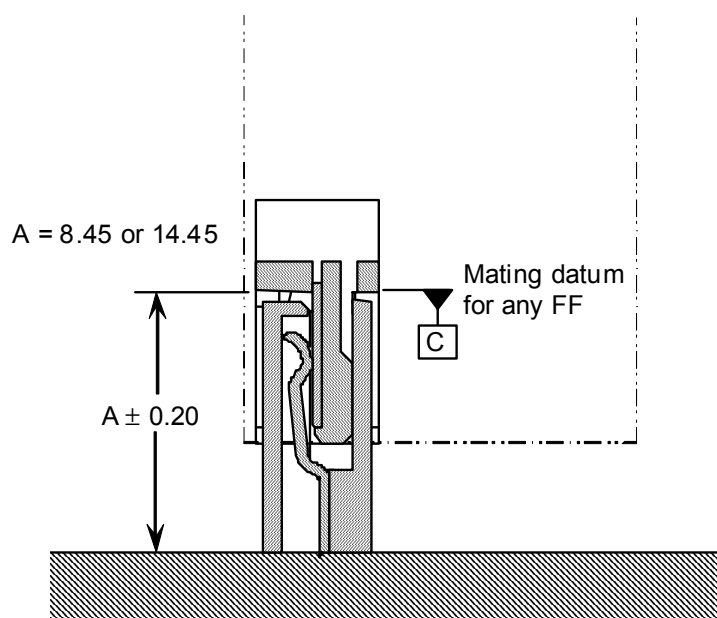


Figure 17 – Device-backplane mating configuration

14.2.6 Connector locations

The device connector location is defined to facilitate blind mating. Figure 18 and Figure 19 define the connector locations on 95 mm (3.5") and 65 mm (2.5") devices, respectively. All dimensions are in millimeters.

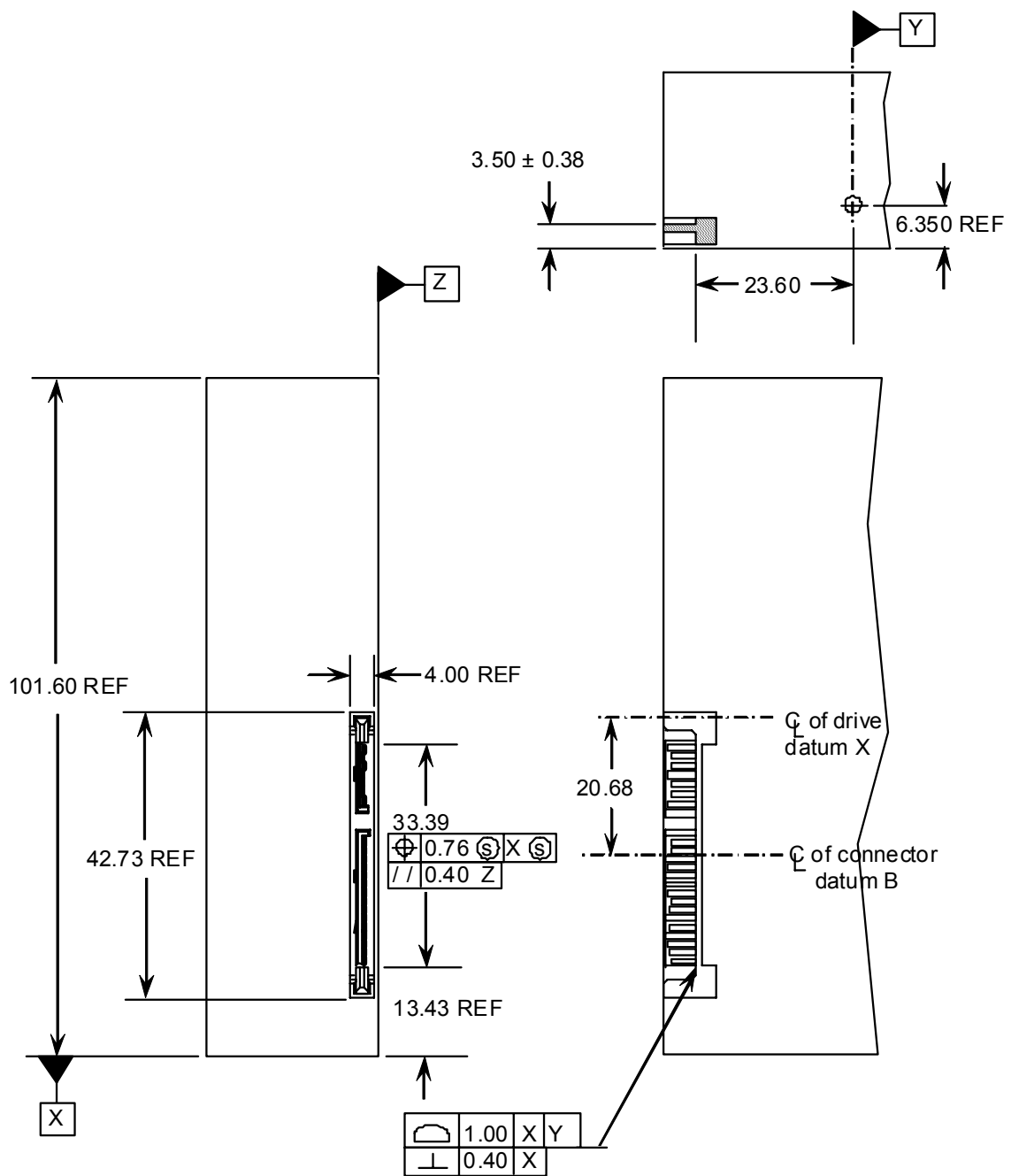


Figure 18 – Device plug connector location on 95 mm (3.5") device

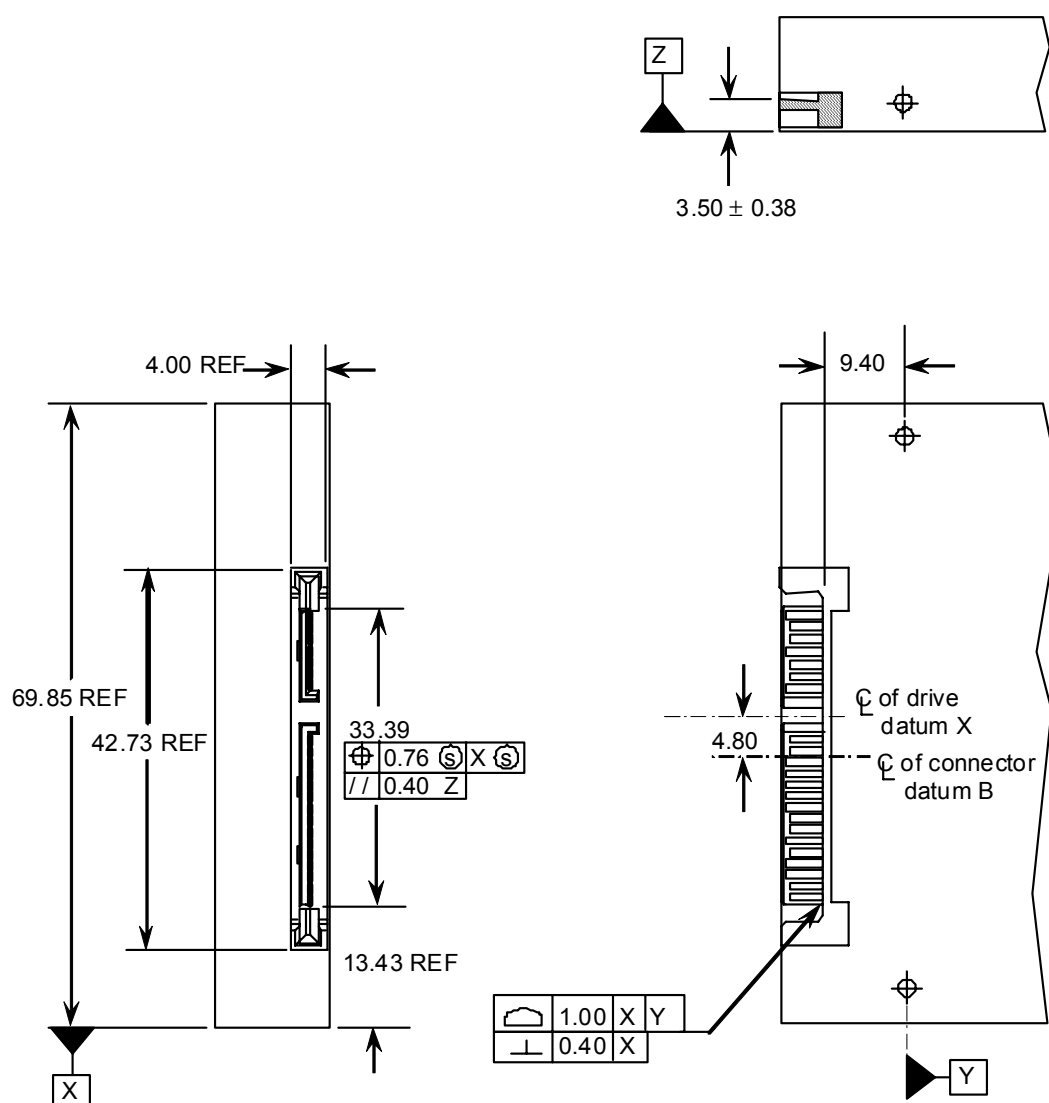


Figure 19 – Device plug connector location on 65 mm (2.5”) device

Recommended host plug connector clearance is shown in Figure 20. All dimensions are in millimeters.

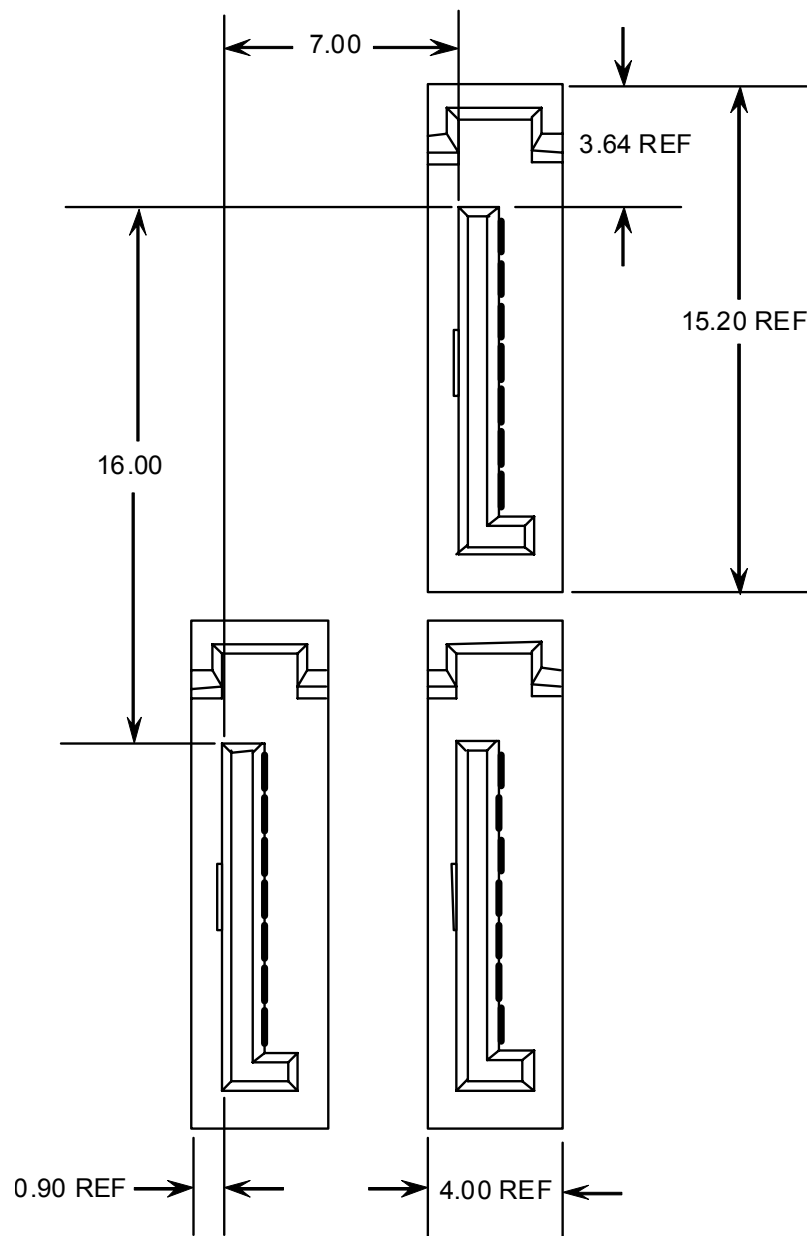


Figure 20 – Recommended host plug spacing for Non-Latching Connectors