

First edition
2007-02-01

Corrected version
2007-04-15

**Information technology —
Telecommunications and information
exchange between systems — MAC-PHY
Interface for ISO/IEC 26907**

*Technologies de l'information — Télécommunications et échange
d'informations entre systèmes — Interface MAC-PHY pour
ISO/CEI 26907*



Reference number
ISO/IEC 26908:2007(E)

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Published in Switzerland

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work. In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 2.

The main task of the joint technical committee is to prepare International Standards. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights.

ISO/IEC 26908 was prepared by Ecma International (as ECMA-369) and was adopted, under a special “fast-track procedure”, by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, in parallel with its approval by national bodies of ISO and IEC.

This corrected and reprinted version of ISO/IEC 26908:2007 incorporates the following correction:

- the addition of “*Telecommunications and information exchange between systems*” as the second title element, which was missing in the original.

Introduction

ISO/IEC 26907 specifies the PHY and MAC for a high rate ultra wideband wireless transceiver.

Implementations of ISO/IEC 26907 may expose the interface between the PHY and MAC as specified herein.

Information technology — Telecommunications and information exchange between systems — MAC-PHY Interface for ISO/IEC 26907

1 Scope

This International Standard specifies the interface between implementations of the PHY and MAC as specified in ISO/IEC 26907.

2 Conformance

PHY and MAC implementations of ISO/IEC 26907 conform to this International Standard by implementing the interface specified herein.

3 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 26907:2006, *Information technology — Telecommunications and information exchange between systems — High Rate Ultra Wideband PHY and MAC Standard*

4 Definitions

For the purposes of this document, the definitions given in ISO/IEC 26907 apply.

5 Notational Conventions

The use of the word *shall* is meant to indicate a requirement which is mandated by the Standard, i.e. it is required to implement that particular feature with no deviation in order to conform to the Standard. The use of the word *should* is meant to recommend one particular course of action over several other possibilities, however without mentioning or excluding these others. The use of the word *may* is meant to indicate that a particular course of action is permitted. The use of the word *can* is synonymous with is able to – it is meant to indicate a capability or a possibility.

All floating-point values have been rounded to 4 decimal places.

An exclamation mark preceding a signal indicates that the signal is active low.

6 Abbreviations and Acronyms

BM	Burst Mode
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Code
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission

FCS	Frame Check Sequence
FFI	Fixed-Frequency Interleaving
FRC	Free Running Clock
HCS	Header Check Sequence
LQI	Link Quality Indicator
lsb	Least-Significant Bit
MAC	Medium Access Control
MIFS	Minimum Interframe Space
msb	Most-Significant Bit
OFDM	Orthogonal Frequency Division Modulation
PHY	Physical (layer)
PLCP	Physical Layer Convergence Protocol
PPM	Parts per Million
PT	Preamble Type
RSSI	Received Signal Strength Indicator
RX	Receive or Receiver
SIFS	Short Interframe Space
TF	Time-Frequency
TFC	Time-Frequency Code
TFI	Time-Frequency Interleaving
TX	Transmit or Transmitter
UWB	Ultra Wideband

7 Overview

[Clause 8](#) defines the interface signals, their directions and functions.

[Clause 9](#) defines the interface parameters and registers. A recommended mapping for PHY parameters is provided along with the register map for PHY registers and setup and hold timing for register access.

[Clause 10](#) defines the frame formats for data exchanges over the interface.

[Clause 11](#) is the Theory of Operation for the complete interface covering the PHY states and transitions, reset and sleep protocols, frame timing references, preamble control and transmit and receive operations for both single frame and burst mode operation as well as receive error cases. The section is completed by definition of the CCA and Management interface protocols.

There are two annexes to this specification. Annex A provides an Electrical Interface and Annex B defines formats for two managed identifiers.

8 Interface Signal Description

The MAC-PHY signal interface is depicted in Figure 1. It consists of the Data Interface including an 8-bit data bus, the Control Interface, the CCA Interface and the Management Interface. The Data Interface, which is used to transfer data to and from the MAC, operates differently depending on the state of the PHY. The Control Interface is used by the MAC to control the operating state of the PHY and by the PHY to indicate TX/RX status to the MAC. The CCA Interface is used for Clear Channel Assessment status indication. The Management Interface is used to access the PHY registers.

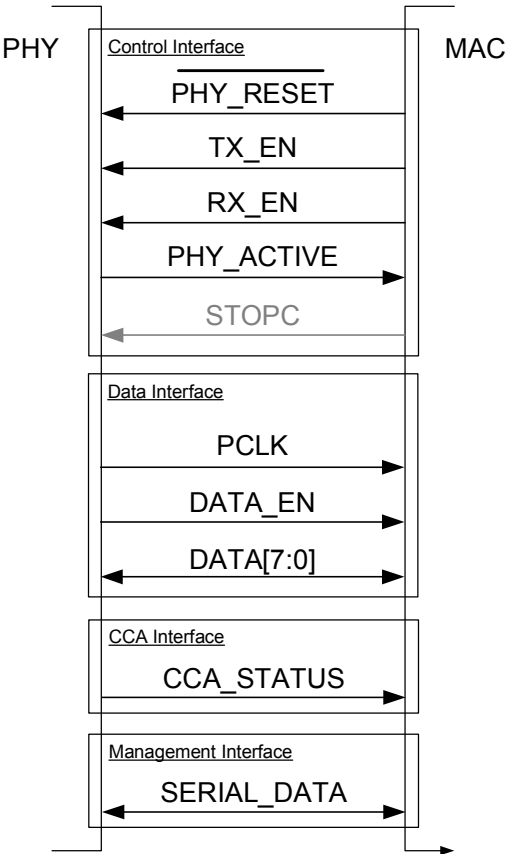


Figure 1 — PHY-MAC interface signals

Table 1 Table 2, Table 3 and Table 4 define the signals in the Control Interface, Data Interface, CCA Interface and Management Interface, respectively. The operational mode of the Data Interface in each PHY state is summarized in Table 5.

8.1 Interface Signal Definitions

8.1.1 Control Interface

Table 1 — Control Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
!PHY_RESET	1	MAC to PHY	!PHY_RESET is asserted for PHY specific interval PHYResetTime to clear all PHY variables and reset the PHY to its initial state. The PHY writes STANDBY to PMMODE and transitions to STANDBY state after !PHY_RESET is de-asserted and reset operations have completed. !PHY_RESET is asynchronous to PCLK. !PHY_RESET is ACTIVE LOW.
TX_EN	1	MAC to PHY	TX_EN is used to place the PHY in TRANSMIT State. [Its secondary use (with RX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.] TX_EN is synchronous to PCLK except in SLEEP state. TX_EN is ACTIVE HIGH.
RX_EN	1	MAC to PHY	RX_EN is used to place the PHY in RECEIVE State. [Its secondary use (with TX_EN) is to transition from SLEEP to STANDBY when the PHY clock source has been stopped for power saving.] RX_EN is synchronous to PCLK except in SLEEP state. RX_EN is ACTIVE HIGH.
PHY_ACTIVE	1	PHY to MAC	PHY_ACTIVE is used by the PHY to indicate that it is either transmitting or receiving a frame over the air. In TRANSMIT state, the rising edge of PHY_ACTIVE indicates the start of frame at the local antenna and the falling edge indicates that the entire frame has been transmitted over the air. In RECEIVE state, the rising edge of this signal indicates that the start of the preamble has been detected (SyncDelay + the preceding synchronization fields earlier) and the falling edge indicates that the entire frame has been received (PHYActiveDelay earlier) at the local antenna. PHY_ACTIVE is also used in the special cases of Exit from SLEEP and RESET. PHY_ACTIVE is synchronous to PCLK. PHY_ACTIVE is ACTIVE HIGH.
STOPC (optional)	1	MAC to PHY	On/Off signal for PCLK in STANDBY state. PCLK is active when STOPC is de-asserted and not active when STOPC is asserted. STOPC is asynchronous to PCLK. STOPC is ACTIVE HIGH.

8.1.2 Data Interface

Table 2 — Data Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
PCLK	1	PHY to MAC	Interface clock provided by the PHY. Interface signals are synchronous to the rising edge of PCLK (see Annex A). The nominal rate of PCLK is 66MHz.
DATA_EN	1	PHY to MAC	In TRANSMIT state, this signal is used by the PHY to request more data from the MAC. In RECEIVE state, it is used to indicate to the MAC that there is valid data on the DATA[7:0] bus. DATA_EN is synchronous to PCLK. DATA_EN is ACTIVE HIGH.
DATA[7:0]	8	Bi-directional	DATA[7:0] is an 8-bit wide data bus driven by the MAC in TRANSMIT state and by the PHY in all other states including SLEEP. DATA[7:0] is synchronous to PCLK whether driven by the PHY or the MAC. DATA[7:0] ONE is HIGH.

8.1.3 CCA Interface

Table 3 — CCA Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
CCA_STATUS	1	PHY to MAC	The PHY returns CCA_STATUS after a CCA request is initiated by the MAC writing to the CCRE register via SERIAL_DATA. CCA_STATUS is synchronous to PCLK. CCA_STATUS is ACTIVE HIGH.

8.1.4 Management Interface

Table 4 — Management Interface Signals

SIGNAL	Width (Bits)	DIR	DESCRIPTION
SERIAL_DATA	1	Bi-directional	The MAC writes control and address bits to SERIAL_DATA to initiate register access. SERIAL_DATA is driven by the MAC for Write operations. It is driven by the MAC for control and address parts of Read operations and by the PHY for the data part of Read operations. SERIAL_DATA is synchronous to PCLK. SERIAL_DATA ONE is HIGH.

8.2 PHY Operational State

Table 5 — PHY Readiness State

STATE	DESCRIPTION
RESET	Transitional state in which the configuration parameters are reset to default values. PCLK is undefined (see 11.11.1).
SLEEP	The radio is off. PCLK is off (see 11.11.2).
STANDBY	The radio is off. PCLK is on (unless STOPC is asserted). STANDBY is a higher activity state than SLEEP.
READY	Parts of the radio are on. PCLK is on.
TRANSMIT	The PHY Tx paths and the radio transmit path are active. PCLK is on.
RECEIVE	The PHY Rx paths and the radio receive path are active. PCLK is on.

9 Registers

In registers, bit positions that are defined as reserved shall be ignored on reading and set to ZERO on writing.

Two sets of parameters are defined to allow the MAC to control the operation of the PHY and permit information to be provided by the PHY to the MAC.

- **STATIC Parameters**

These parameters are fixed for a given instantiation of the MAC and PHY. They can be considered to be constants for the purposes of the definition of the MAC-PHY Interface and their values can be defined in a given PHY data sheet, stored as constants in the system implementation or provided by any other means. The static parameters are defined in Table 6.

- **DYNAMIC Parameters**

These parameters may be changed during operation of the system, and affect operation of the PHY. They shall be implemented within the PHY as registers and can be read and/or written (depending on the specific parameter) via the Serial Management Interface. The dynamic registers are defined in Table 7.

9.1 Bit Ordering and Interpretation

All data structures, except where explicitly stated, are defined with the bit order as shown in Figure 4.

Reserved bits shall be ignored on reading and set to ZERO on writing.

9.2 Register Address Spaces

The PHY has 256 addressable 8-bit registers (8-bit address, 8-bit data) divided into 3 regions:

Dynamic Register region defined by this specification: address 00(h)~1F(h)

Optional Static Parameter region defined by this specification: address 20(h)~7F(h)

Vendor Specific Register region for vendor defined registers: address 80(h)~FF(h)

9.3 Static Parameter Definitions

Table 6 — Description of Static Parameters

REGISTER	OCTETS	DEFINITION
SupportedRegDomains	2	Supported regulatory regions. Bit set to ONE if supported, ZERO otherwise First Octet Bit Domain [2:0] Reserved [3] European Region [4] United States of America [5] Canada [6] Japan [7] Korea Second Octet Bit Domain [7:0] Reserved
SupportedDataRates	2	Set of supported data rates. Bit set to ONE if supported, ZERO otherwise Bit Data Rate Supported [0] 53,33 Mbps [1] RESERVED [2] 80 Mbps [3] 106,7 Mbps [4] RESERVED [5] 160 Mbps [6] 200 Mbps [7] 320 Mbps [8] 400 Mbps [9] 480 Mbps [15:10] RESERVED
NumChannelsSupported	1	Number of supported channels

Table 6 — Description of Static Parameters (continued)

REGISTER	OCTETS	DEFINITION
SupportedDiversity	1	Number of additional antennas provided for diversity [1:0] Number of additional receive antennas [3:2] Reserved [5:4] Number of additional transmit antennas [7:6] Reserved
SupportedChannels	1	Supported Channels. Bit set to ONE if supported, ZERO otherwise Bit Channel Supported [0] TFC channels in band group 1 supported [1] TFC channels in band group 2 supported [2] TFC channels in band group 3 supported [3] TFC channels in band group 4 supported [4] TFC channels in band group 5 supported [7:5] RESERVED
TXPowerLevel	16	Array of transmit power levels. Each element from 0 to (NumTxPowerLevels-1) of the array holds a supported transmit power. The format of the power level datum is PHY vendor specific. The other elements shall be set to zero. Element 0 shall hold the maximum transmit power supported.
NumTxPowerLevels	1	Number of transmit power levels supported. Permitted range (0..15) with 0 meaning a single fixed power level only. [3:0] number of levels (permitted range 0..15) [7:4] RESERVED
SupportedPHYStates	1	Supported PHY States. Bit set to ONE if supported, ZERO otherwise. [0] SLEEP [1] STANDBY [2] READY [3] TRANSMIT [4] RECEIVE [7:5] RESERVED
PHYClockAccuracy	1	Accuracy of PHY clock. Units ppm.
PHYResetTime	1	Interval during which !PHY_RESET shall be held asserted for the PHY to perform the RESET operation. Units us.

Table 6 — Description of Static Parameters (continued)

REGISTER	OCTETS	DEFINITION
WakeUpDelay	2	Time to transition from SLEEP mode to STANDBY mode. Units 0,5 μ s.
TurnOnDelay	2	Radio turn-on time during transition from STANDBY mode to READY mode. Units 0,5 μ s.
TxDataDelay	1	Time period before the end of the preamble at the local antenna before which the PHY will not assert DATA_EN to request the first octet of header data. (See 11.4) Units μ s.
TxDelay	2	Delay from the rising edge of TX_EN to the time when the PHY feeds the leading edge of the preamble waveform to the antenna. Units ns.
RxDelay	2	Delay from the rising edge of RX_EN to the time when the PHY begins the preamble acquisition processing. Units ns.
Tx2RxDwellTime	2	Minimum interval between PHY_ACTIVE de-assertion (in TRANSMIT State) and RX_EN assertion. Units ns.
Rx2TxDwellTime	2	Minimum interval between RX_EN de-assertion and TX_EN assertion. Units ns.
SyncDelay	2	Delay from the end of the last symbol of the Frame Synchronization Sequence of the preamble waveform in the local antenna to the time when the PHY asserts PHY_ACTIVE. Note that since the preamble arrives asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be asserted assuming optimal alignment of the received preamble and PCLK. Units ns.
TxSetupTime	2	Minimum time between setting of transmit control registers and assertion of TX_EN. Units PCLK cycles.
RxSetupTime	2	Minimum time between setting of receive control registers and the assertion of RX_EN or de-assertion of PHY_ACTIVE. Units PCLK cycles.
TxHoldTime	2	Minimum time between the assertion of TX_EN and changing transmit control registers for the next frame. Units PCLK cycles.
RxHoldTime	2	Minimum time between the assertion of RX_EN or deassertion of PHY_ACTIVE and changing receive control registers for the next frame. Units PCLK cycles.
PHYID	2	PHY identifier to specify vendor, product and version. See Annex B for format and coding.

Table 6 — Description of Static Parameters (concluded)

REGISTER	OCTETS	DEFINITION
PHYVersion	1	Edition of the ISO/IEC 26907 PHY specification supported. See Annex B for format and coding.
PHYActiveDelay	2	Delay from the end of the last symbol of the frame received in the local antenna and PHY_ACTIVE de-assertion. Note that since received frames arrive asynchronously with respect to PCLK, PHY vendors should provide this value for the shortest amount of time before PHY_ACTIVE could be de-asserted assuming optimal alignment of the received frame and PCLK. Units ns.
CCAVlidTime	1	Interval following the MAC setting CCRE = ONE after which the PHY should respond with the CCA measurement result. Units 0,5 μs.
MinPTChangeLength	1	Minimum MAC Frame Payload length for the preamble type of the next frame to be different to the current frame. Fixed value = 1 octet
RangingSupported	1	Support of ranging [0] Set to ONE if supported, otherwise set to ZERO [1] Support for 528MHz precision (Mandatory) [2] Support for 1 056MHz precision [3] Support for 2 112MHz precision [4] Support for 4 224MHz precision [5] Support for RANGINGTIMER [23:16] [6] Support for RANGINGTIMER [31:24] [7] RESERVED
RANGING_TRANSMIT_DELAY	2	The time from the generation of the ranging reference signal (start of the Channel Estimation sequence of the preamble), triggering the RANGINGTIMER capture, to the time this signal reaches the device antenna. Units 1 / 4 224 MHz - same as RANGINGTIMER (see Table 7)
RANGING_RECEIVE_DELAY	2	The time from the arrival of the reference signal at the antenna to the time this signal is first detected in the PHY, triggering the RANGINGTIMER clock capture. Units 1 / 4 224 MHz - same as RANGINGTIMER (see Table 7)

9.4 Static Parameter Coding

If the values of the static parameters are stored in the PHY, they should be implemented as read only values using the addresses and formats shown in Figure 2 and Figure 3.

	bit-7		bit-4	bit-3		bit-0
7F(h)	Reserved					
7E(h)	Reserved					
6F(h)	Reserved					
6E(h)	TxPowerLevel15					
5F(h)	TxPowerLevel15[7:0]					
5E(h)	TxPowerLevel0					
50(h)	TxPowerLevel0[7:0]					
4F(h)	Reserved					
4E(h)	Reserved					
4D(h)	RxHoldTime[15:8]					
4C(h)	RxHoldTime[7:0]					
4B(h)	TxHoldTime[15:8]					
4A(h)	TxHoldTime[7:0]					
49(h)	RxSetupTime[15:8]					
48(h)	RxSetupTime[7:0]					
47(h)	TxSetupTime[15:8]					
46(h)	TxSetupTime[7:0]					
45(h)	SyncDelay[15:8]					
44(h)	SyncDelay[7:0]					
43(h)	RxDelay[15:8]					
42(h)	RxDelay[7:0]					
41(h)	TxDelay[15:8]					
40(h)	TxDelay[7:0]					

Figure 2 — Static Parameter Encoding 40(h) -7F(h)

	bit-7			bit-4	bit-3			bit-0
3F(h)				RANGING_RECEIVE_DELAY[15:8]				
				RANGING_RECEIVE_DELAY				
3E(h)				RANGING_RECEIVE_DELAY[7:0]				
3D(h)				RANGING_TRANSMIT_DELAY[15:8]				
				RANGING_TRANSMIT_DELAY				
3C(h)				RANGING_TRANSMIT_DELAY[7:0]				
3B(h)				Rx2TxDwellTime[15:8]				
				Rx2TxDwellTime				
3A(h)				Rx2TxDwellTime[7:0]				
39(h)				Tx2RxDwellTime[15:8]				
				Tx2RxDwellTime				
38(h)				Tx2RxDwellTime[7:0]				
37(h)				TurnOnDelay[15:8]				
				TurnOnDelay				
36(h)				TurnOnDelay[7:0]				
35(h)				WakeUpDelay[15:8]				
				WakeUpDelay				
34(h)				WakeUpDelay[7:0]				
33(h)				PHYActiveDelay[15:8]				
				PHYActiveDelay				
32(h)				PHYActiveDelay[7:0]				
				TxDataDelay				
31(h)				TxDataDelay[7:0]				
				MinPTChangeLength				
30(h)				MinPTChangeLength[7:0]				
				CCAValiTime				
2F(h)				CCAValiTime[7:0]				
				PHYResetTime				
2E(h)				PHYResetTime[7:0]				
				PHYClockAccuracy				
2D(h)				PHYClockAccuracy[7:0]				
				RangingSupported				
2C(h)	Reserved	32 Bit	24 Bit	4 224MHz	2 112MHz	1 056MHz	528MHz	Ranging Supported
				SupportedPHYStates				
2B(h)	Reserved			RECEIVE	TRANSMIT	READY	STANDBY	SLEEP
				NumTxPowerLevel				
2A(h)				NumTxPowerLevel[7:0]				
				SupportedChannels				
29(h)	Reserved			TFC BG5	TFC BG4	TFC BG3	TFC BG2	TFC BG1
				SupportedDiversity				
28(h)	Reserved			TxDiversity[5:4]	Reserved			RxDiversity[1:0]
				NumChannelsSupported				
27(h)				NumChannelsSupported[7:0]				
				SupportedDataRates2				
26(h)	Reserved						480Mb/s	400Mb/s
				SupportedDataRates1				
25(h)	320Mb/s	200Mb/s	160Mb/s	Reserved	106.67Mb/s	80Mb/s	Reserved	53.3Mb/s
				SupportedRegDomain2				
24(h)	Reserved			SupportedRegDomain1				
23(h)	MIC	ARIB	IC	FCC	ETSI	Reserved		
				PHYVersion				
22(h)				PHYVersion[7:0]				
21(h)				PHYID[15:8]				
				PHYID				
20(h)				PHYID[7:0]				

Figure 3 — Static Parameter Encoding 20(h) - 3F(h)