
**Telecommunications and information
exchange between systems —
Unmanned aircraft area network
(UAAN) —**

**Part 4:
Physical and data link protocols for
video communication**

*Télécommunications et échange d'information entre systèmes —
Réseau de zone de drones (Unmanned aircraft area network -
UAAN) —*

*Partie 4: Protocoles de liaison de données et physiques pour la
communication vidéo*



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Foreword

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A list of all parts in the ISO/IEC 4005 series can be found on the ISO and IEC websites.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html and www.iec.ch/national-committees.

Introduction

Unmanned aircrafts (UAs) operating at low altitudes will provide a variety of commercial services in the near future. UAs that provide these services are distributed in the airspace. In level II, many people operate their own UAs without the assignment of communication channels from a central control centre.

This document describes video communication, which is a wireless distributed communication. Video communication allows UAs distributed over the airspace to transmit video without serious interference to the relevant video receiver which is usually a controller. The channels used for video communication have a multi-channel structure, which enables UA and video receiver pairs to independently use the occupied communication link. A wireless distributed communication described by this document is intended to be used in licensed frequency bands.

The ISO/IEC 4005 series consists of the following four parts:

- ISO/IEC 4005-1: To support various services for UAs, it describes a wireless distributed communication model and the requirements that this model shall satisfy.
- ISO/IEC 4005-2: It describes communication in which all units involved in UA operation can broadcast or exchange information by sharing communication resources with each other.
- ISO/IEC 4005-3: It describes the control communication for the controller to control the UA.
- ISO/IEC 4005-4 (this document): It describes video communication for UAs to send video to a controller.

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Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) —

Part 4: Physical and data link protocols for video communication

1 Scope

This document specifies communication protocols for the physical and data link layer of video communication, which is a wireless distributed communication network for units related with unmanned aircrafts (UAs) in level II.

This document describes video communication, which is one-to-one communication that transmits video from a UA to a video receiver. For the specific use of video communication, video can be transmitted from a UA to multiple receivers.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 4005-1, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 1: Communication model and requirements*

ISO/IEC 4005-2, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 2: Physical and data link protocols for shared communication*

ISO/IEC 4005-3, *Telecommunications and information exchange between systems — Unmanned aircraft area network (UAAN) — Part 3: Physical and data link protocols for control communication*

ISO 21384-4, *Unmanned aircraft systems — Part 4: Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions defined in ISO/IEC 4005-1, ISO/IEC 4005-2, ISO/IEC 4005-3, ISO 21384-4 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at <https://www.iso.org/obp>
- IEC Electropedia: available at <https://www.electropedia.org/>

4 Abbreviated terms

CC	Control Communication
CB	Coding Block
CRC	Cyclic Redundancy Check

CSCH	Control Subchannel
DL	Data Link
DLL	Data Link Layer
DQPSK	Differential Quadrature Phase Shift Keying
DS	Dedicated Slot
FN	Frame Number
GF	Galois Field
PCCC	Parallel Concatenated Convolutional Code
PB	Parsing Block
PH	Parsing Header
PKH	Packet Header
PN	Pseudo Noise
SA	Source Address
SC	Shared Communication
SRRC	Square Root Raised Cosine
TSB	Tone Slot Block
UTC	Coordinated Universal Time
VC	Video Communication
VSCH	Video Subchannel

5 Physical layer

5.1 Channel and frame structure for data channel

5.1.1 The number of data channels and bandwidth

The number of data channels is L . L is greater than or equal to one. The bandwidth of one data channel is 5 MHz as shown in [Figure 1](#). The L is determined in the upper layer.

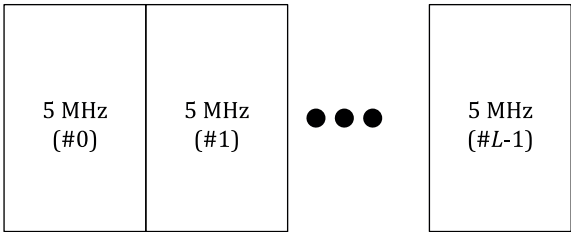
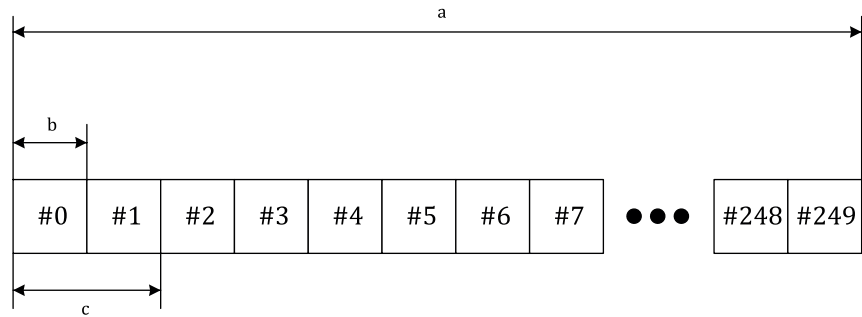


Figure 1 — Data channels in frequency region

5.1.2 Frame structure

The frame length of the data channel is 1 sec and consists of 250 slots. The one slot time T_s is 4 ms. A data slot block has 2 slots. Therefore, there are 125 data slot blocks in one frame, and the data slot block is 8 ms in length as shown in [Figure 2](#). The frame number, FN changes from 0 to 59 in a 1 min interval, and has the same value as the second of the current time.

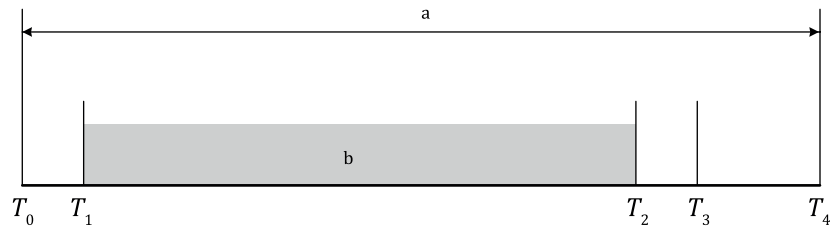


- a 1 frame, $T_f = 1 \text{ second} = 250 T_s$.
- b 1 slot, $T_s = 4 \text{ ms}$.
- c 1 slot block, $T_{sb} = 8 \text{ ms} = 2 T_s$.

Figure 2 — Data channel frame structure

5.1.3 Slot transmit time mask

The transmission time mask of a slot is as shown in [Figure 3](#).



- Key**
- T_0 0 μs
 - T_1, T_2, T_3, T_4 symbol offset from T_0
 - a 4 ms.
 - b Modulated signal.

Figure 3 — The transmission time mask of a slot

T_1, T_2, T_3, T_4 are symbol offsets from T_0 and symbol time is 1/2688000 sec. Each value is as follows: T_1 is 8, T_2 is 10380, T_3 is 10388, T_4 is 10752.

T_0 is 0 μs as the start time of the slot and the power amplifier is gated on and unmodulated fine signals begin to be transmitted. T_1 is an offset at which modulation signal transmission starts. T_2 is an offset at which the transmission of the modulated signal ends. T_3 is an offset at which the power amplifier is gated off, and transmission of unmodulated fine signals is stopped. The transmit power of T_0 to T_1 , T_2 to T_3 shall be at least 50 dB less than the modulation signal transmit power.

5.1.4 Sub channels

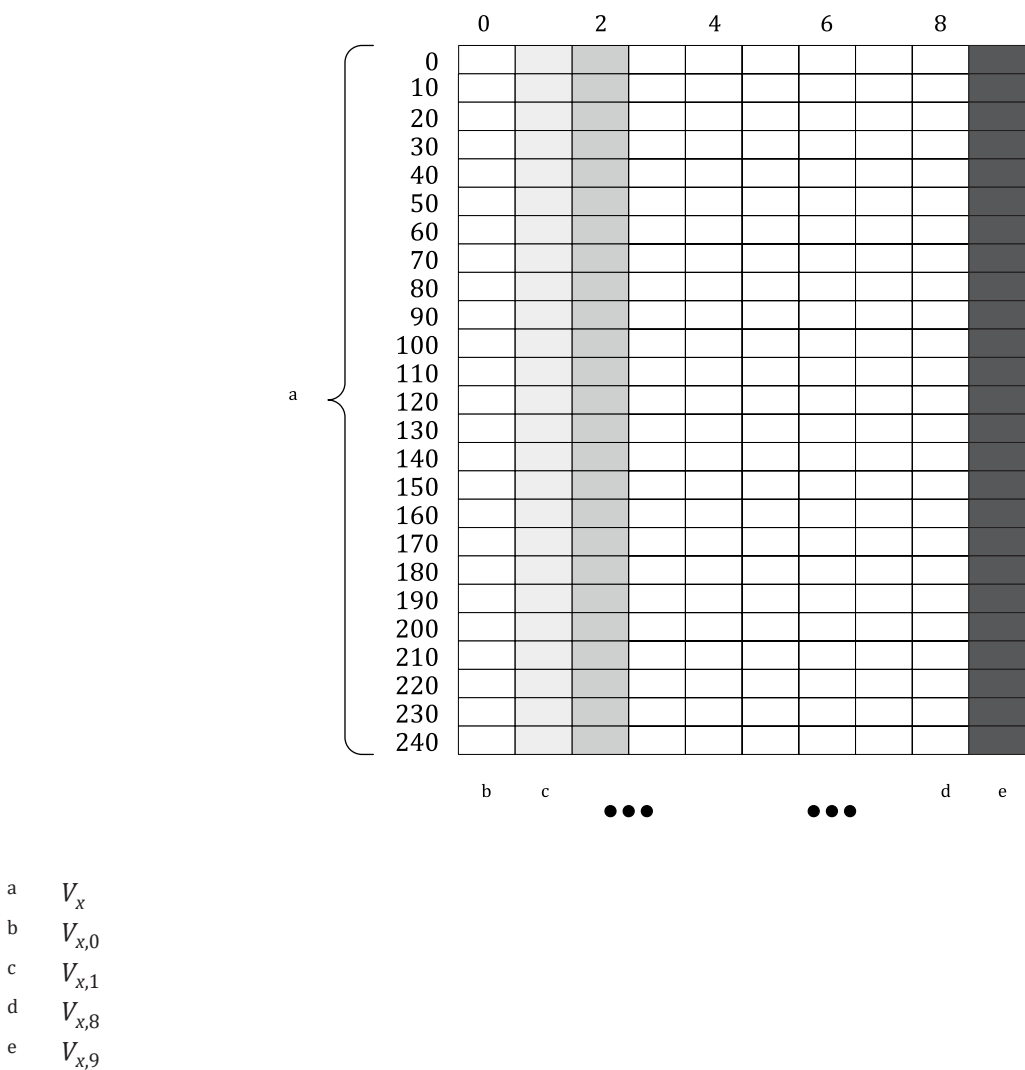


Figure 4 — Sub channel structure of video communication in even frame

One data channel consists of 10 subchannels as shown in [Figure 4](#). Subchannel y of video channel x is composed of the following slot set.

$$V_{x,y} = S_{x,z}, S_{x,z+10}, S_{x,z+20}, \dots, S_{x,z+240}$$
$$z = \begin{matrix} y, & \text{even frame} \\ y+1 - \lfloor (y \bmod 2) / 2 \rfloor \times 2, & \text{odd frame} \end{matrix} \tag{1}$$

where

- y is subchannel number, $y=0, 1, \dots, 9$;
- $S_{x,z}$ is slot z of video channel x .

The subchannel consists of 25 slots, the i -th slot resource of the subchannel y of the channel x is indicated by $SR_{x,y,i}$ and the subchannel y of frequency channel x is indicated by $V_{x,y}$. Therefore, $V_{x,y}$ is as follows:

$$V_{x,y} = SR_{x,y,0}, SR_{x,y,1}, \dots, SR_{x,y,24} \quad (2)$$

where $SR_{x,y,i}$ is i -th slot resource of subchannel y of channel x , $i=0, \dots, 24$.

All slots of video channel are downlink.

5.1.5 Dedicated subchannels

The upper layer can predetermine one or several subchannels as dedicated subchannels. In this case, the tone subslot set mapped with the dedicated subchannel is not used as a competition tone and can be used for other purposes.

Dedicated subchannel information is received from an upper layer through UPtoDL.InfoDedicatedChannel.

5.2 Channel and frame structure for tone channel

5.2.1 General

The tone channel of video communication means a competitive tone channel. The tone channel used for video communication resource allocation and the tone channel used for control communication resource allocation are the same channel (see ISO/IEC 4005-3).

5.2.2 Slot transmit power

The maximum transmission power $P_{\max TCH}$ of the tone slot mapped to the video subchannel (VSCH) is received as UPtoDL.InfoPowerParamVCH from the upper layer. The power of the tone subslot signal is determined by adding the PTX_VCHTCH_differ value to the transmission power of the mapped VSCH.

5.3 Encoding procedure

The encoding follows the following procedure. CRC encoding, turbo coding, rate matching, interleaving, modulation mapping, burst mapping, and pulse mapping are performed in this order as shown in [Figure 5](#).

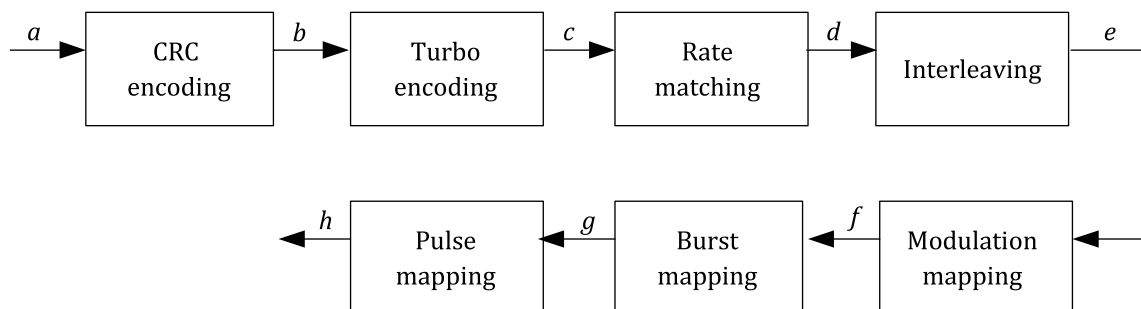


Figure 5 — Encoding procedure

The number of symbols according to each encoding stage is shown in [Table 1](#), where the encoding input consists of two code blocks, CB0 and CB1 as shown in [Figure 14](#). Each code block undergoes CRC encoding, turbo coding, rate matching, interleaving, and modulation mapping processes, respectively. The length of each code block in these processes is 4094, 4928, 9868, 9856, 9856, and 4928. The two code blocks are merged into one burst during burst mapping.

Table 1 — Number of symbols at each encoding stage

Stage	Number of symbols
<i>a</i>	4904 × 2 (binary)
<i>b</i>	4928 × 2 (binary)
<i>c</i>	9868 × 2 (binary)
<i>d</i>	9856 × 2 (binary)
<i>e</i>	9856 × 2 (binary)
<i>f</i>	4928 × 2 (complex)
<i>g</i>	10364 (complex)
<i>h</i>	10372 × OS (complex)

5.3.1 CRC encoding

The input bits are defined as $a_0, a_1, a_2, a_3, \dots, a_{A-1}$ and parity bits as $p_0, p_1, p_2, p_3, \dots, p_{23}$ where A represents the number of input sequences. Parity bits are generated through CRC generation polynomial as follows.

$$g_{\text{CRC}}(D) = D^{24} + D^{22} + D^6 + D^5 + D + 1 \quad (3)$$

The encoding performed through the cyclic generator polynomials has a systematic form as follows. The resulting polynomial has zero remainder when it is divided by $g_{\text{CRC}}(D)$ on GF(2).

$$a_0 D^{A+23} + a_1 D^{A+22} + \dots + a_{A-1} D^{24} + p_0 D^{23} + p_1 D^{22} + \dots + p_{22} D^1 + p_{23} \quad (4)$$

After CRC insertion, bits are represented by $b_0, b_1, b_2, b_3, \dots, b_{B-1}$ (where $B = A + 24$), and the relationship between a_k and b_k is as follows.

$$b_k = \begin{cases} a_k, & \text{for } k=0, 1, 2, \dots, A-1 \\ p_{k-A}, & \text{for } k=A, A+1, A+2, \dots, A+23 \end{cases} \quad (5)$$

5.3.2 Turbo encoding

The turbo encoder consists of Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one turbo coded internal interleaver. The coding rate of the turbo encoder is 1/2. The structure of the turbo encoder is shown in [Figure 6](#). The PCCC transfer function is as follows.

$$G(D) = [1, g_1(D)/g_0(D)] \quad (6)$$

where $g_0(D) = 1 + D^2 + D^3$, $g_1(D) = 1 + D + D^3$.

When the input bits of the turbo encoder are encoded, the initial values of the shift registers of the 8-state constituent encoder shall all be zero.

For $k = 0, 1, 2, \dots, B/2-1$, the output value of the turbo encoder is expressed as follows.

$$c_{4k} = x_{2k}$$

$$c_{4k+1} = z_{2k}$$

$$c_{4k+2} = x_{2k+1}$$

$$c_{4k+3} = z'_{2k+1} \quad (7)$$

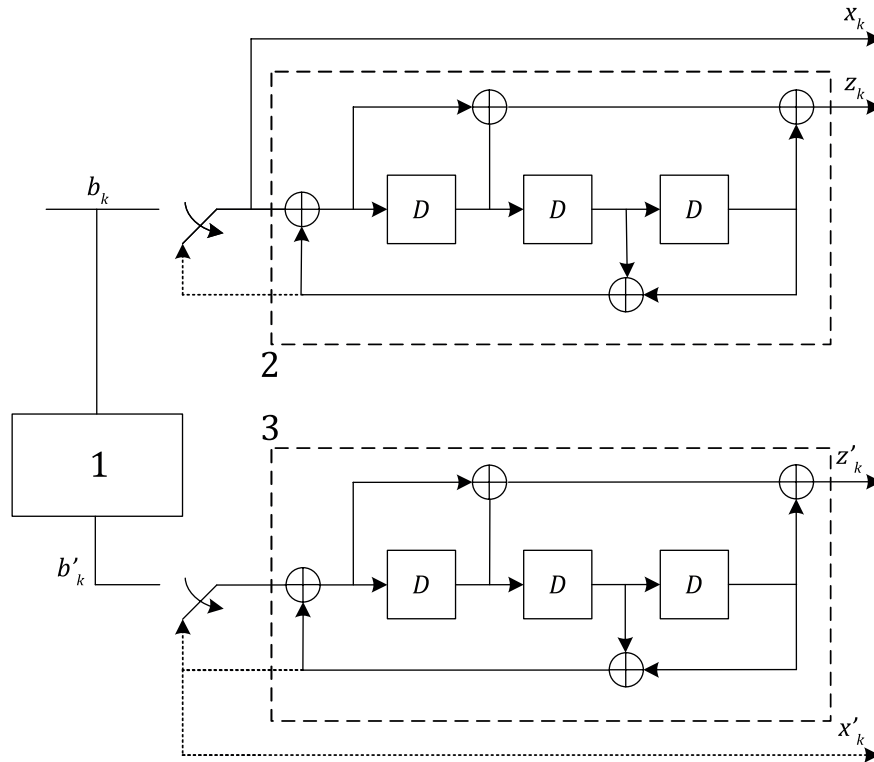
Output bits of the first and second 8-state constituent encoders for turbo encoder input bits $b_0, b_1, b_2, b_3, \dots, b_{B-1}$ are $z_0, z_1, z_2, z_3, \dots, z_{B-1}$ and $z'_0, z'_1, z'_2, z'_3, \dots, z'_{B-1}$, and the output bits through the turbo code internal interleaver that is described in [Annex A](#) are represented by $b'_0, b'_1, b'_2, b'_3, \dots, b'_{B-1}$. These output bits are used as inputs for the second 8-state constituent encoder.

Trellis termination is performed by taking tail bits from shift register feedback after all information bits have been encoded. The generated tail bits are added after encoding of the information bits.

The first three tail bits are used for the first constituent encoder termination and not the second constituent encoder. The remaining three tail bits are used for the termination of the second constituent encoder and not the first constituent encoder.

The bits transmitted for trellis termination are determined as follows.

$$\begin{aligned} c_{2B} &= x_B, c_{2B+3} = z_{B+1}, c_{2B+6} = x'_B, c_{2B+9} = z'_{B+1} \\ c_{2B+1} &= z_B, c_{2B+4} = x_{B+2}, c_{2B+7} = z'_B, c_{2B+10} = x'_{B+2} \\ c_{2B+2} &= x_{B+1}, c_{2B+5} = z_{B+2}, c_{2B+8} = x'_{B+1}, c_{2B+11} = z'_{B+2} \end{aligned} \quad (8)$$



Key

- 1 turbo code internal interleaver
- 2 first constituent encoder
- 3 second constituent encoder
- D register
- b_k a k -th bit of turbo encoder input
- b'_k a k -th bit of turbo code internal interleaver output
- x_k a k -th systematic bit of turbo encoder output
- z_k a k -th bit of first constituent encoder output
- x'_k a k -th bit of second constituent encoder output for trellis termination
- z'_k a k -th bit of second constituent encoder output

Figure 6 — Turbo encoder structure

Input bit sequence of turbo code internal interleaver, $b_0, b_1, b_2, b_3, \dots, b_{B-1}$ and output bit sequence generated from turbo code internal interleaver, $b'_0, b'_1, b'_2, b'_3, \dots, b'_{B-1}$ have the following relationship.

$$b'_i = b_j \quad (9)$$

where the mapping between the output bit index i and the input bit index j shall follow [Table A.1](#) of [Annex A](#) where j and i are as follows, and row and column numbers start at zero.

$$j = (\text{number shown in table}) - 1$$

$$i = (\text{row number in table}) \times 16 + (\text{column number in table}) \quad (10)$$

5.3.3 Rate matching

Rate matching outputs $d_0, d_1, d_2, d_3, \dots, d_{D-1}$ by puncturing the input bits $c_0, c_1, c_2, c_3, \dots, c_{C-1}$. The puncturing bit numbers are as follows.

— 821, 1643, 2461, 3283, 4101, 4923, 5741, 6563, 7381, 8203, 9021, 9843

5.3.4 Interleaving

The interleaver uses block interleaving with 77 rows and 128 columns.

$$e_m = d_n$$

$$m = (n \times 77) \% 9856 + \lfloor n/128 \rfloor \quad (11)$$

where $\lfloor x \rfloor$ means the largest integer among integers less than or equal to x and $0 \leq n \leq 9855$.

5.3.5 Modulation mapping

Modulation mapping generates a complex symbol f_n from the input bit e_m , $0 \leq n \leq 9855$, $0 \leq m \leq 4927$. Two input bits are mapped to one complex number as shown in [Table 2](#).

Table 2 — Modulation mapping

$e_{2n}e_{2n+1}$	00	01	10	11
f_n	$\exp(j/4\pi)$	$\exp(j \cdot 7/4\pi)$	$\exp(j \cdot 3/4\pi)$	$\exp(j \cdot 5/4\pi)$

5.3.6 Burst mapping

Output complex symbols $g_0, g_1, \dots, g_{4927}$ are generated from $f_0, f_1, \dots, f_{4927}$ of CB0 and $f_0, f_1, \dots, f_{4927}$ of CB1.

$$g_n = \prod_{k=0}^n c(k) \quad (12)$$

where $c(n)$ is shown in [Table 3](#).

Table 3 — $c(n)$

n	$c(n)$	Number of symbols
0, 1	$TSS(n)$	2
2, ..., 37	$PTS1(n-2)$	36
38, ..., 767	f_{n-38} of CB0	730
768, ..., 803	$PTS1(n-768)$	36
804, ..., 1533	f_{n-74} of CB0	730
1534, ..., 1569	$PTS1(n-1534)$	36
1570, ..., 2299	f_{n-110} of CB0	730
2300, ..., 2335	$PTS1(n-2300)$	36
2336, ..., 3065	f_{n-146} of CB0	730
3066, ..., 3101	$PTS1(n-3066)$	36
3102, ..., 3831	f_{n-182} of CB0	730
3832, ..., 3867	$PTS1(n-3832)$	36
3868, ..., 4597	f_{n-218} of CB0	730
4598, ..., 4633	$PTS1(n-4598)$	36

Table 3 (continued)

n	$c(n)$	Number of symbols
4634, ..., 5181	f_{n-254} of CB0	548
5182, ..., 5363	f_{n-5182} of CB1	182
5364, ..., 5399	$PTS1(n-5364)$	36
5400, ..., 6129	f_{n-5218} of CB1	730
6130, ..., 6165	$PTS1(n-6130)$	36
6166, ..., 6895	f_{n-5254} of CB1	730
6896, ..., 6931	$PTS1(n-6896)$	36
6932, ..., 7661	f_{n-5290} of CB1	730
7662, ..., 7697	$PTS1(n-7662)$	36
7698, ..., 8427	f_{n-5326} of CB1	730
8428, ..., 8463	$PTS1(n-8428)$	36
8464, ..., 9193	f_{n-5362} of CB1	730
9194, ..., 9229	$PTS1(n-9194)$	36
9230, ..., 9959	f_{n-5398} of CB1	730
9960, ..., 9995	$PTS1(n-9960)$	36
9996, ..., 10361	f_{n-5434} of CB1	366
10362, 10363	$TSS(n-10362)$	2

where $TSS(n)$ and $PTS1(n)$ are shown in [Table 4](#) and [Table 5](#) respectively.

Table 4 — $TSS(n)$

$TSS(0)$	$TSS(1)$
$\exp(j \cdot 3/4\pi)$	$\exp(j \cdot 7/4\pi)$

Table 5 — $PTS1(n)$

n	$PTS1(n)$	n	$PTS1(n)$	n	$PTS1(n)$
0	$\exp(j \cdot 5/4\pi)$	12	$\exp(j \cdot 5/4\pi)$	24	$\exp(j \cdot 7/4\pi)$
1	$\exp(j \cdot 7/4\pi)$	13	$\exp(j/4\pi)$	25	$\exp(j \cdot 5/4\pi)$
2	$\exp(j \cdot 7/4\pi)$	14	$\exp(j/4\pi)$	26	$\exp(j \cdot 7/4\pi)$
3	$\exp(j \cdot 5/4\pi)$	15	$\exp(j \cdot 5/4\pi)$	27	$\exp(j/4\pi)$
4	$\exp(j/4\pi)$	16	$\exp(j \cdot 7/4\pi)$	28	$\exp(j \cdot 5/4\pi)$
5	$\exp(j/4\pi)$	17	$\exp(j/4\pi)$	29	$\exp(j \cdot 3/4\pi)$
6	$\exp(j \cdot 3/4\pi)$	18	$\exp(j \cdot 5/4\pi)$	30	$\exp(j \cdot 3/4\pi)$
7	$\exp(j \cdot 5/4\pi)$	19	$\exp(j \cdot 3/4\pi)$	31	$\exp(j/4\pi)$
8	$\exp(j \cdot 3/4\pi)$	20	$\exp(j \cdot 7/4\pi)$	32	$\exp(j/4\pi)$
9	$\exp(j/4\pi)$	21	$\exp(j/4\pi)$	33	$\exp(j \cdot 5/4\pi)$
10	$\exp(j \cdot 5/4\pi)$	22	$\exp(j/4\pi)$	34	$\exp(j \cdot 3/4\pi)$
11	$\exp(j \cdot 5/4\pi)$	23	$\exp(j \cdot 3/4\pi)$	35	$\exp(j \cdot 7/4\pi)$

5.3.7 Pulse mapping

The complex symbol g_m is converted into a complex signal h_n , where the oversampling ratio of the filter is OS times and depends on implementation. For $0 \leq n < 10372 \times OS$, the complex signal is defined as follows.

$$h_n = w\left(\frac{nT_s}{OS}\right) \sum_{m=0}^{10363} p\left(\left(\frac{n}{OS} - m - 4\right)T_s\right) g_m \quad (13)$$

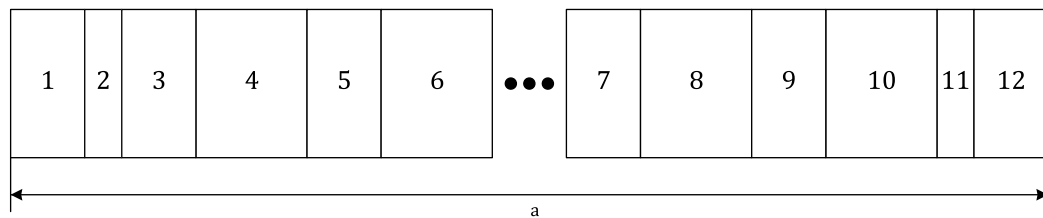
where symbol duration T_s is the $1/2688000$ second and pulse shape $p(t)$ is defined as SRRC function of roll-off factor 0,35 as follows.

$$p(t) = \frac{1}{1 + \frac{(1-\alpha)\pi}{4\alpha}} \cdot \frac{\cos\left(\frac{(1+\alpha)\pi t}{T_s}\right) + \frac{\sin((1-\alpha)\pi t / T_s)}{4\alpha t / T_s}}{1 - (4\alpha t / T_s)^2} \quad (14)$$

The window function $w(t)$ is defined as follows.

$$w(t) = \begin{cases} (1/2)(1 - \cos(\pi t / 2T_s)), & 0 \leq t < 2T_s \\ 1, & 2T_s \leq t < 10370T_s \\ (1/2)(1 - \cos\left(\frac{\pi}{2T_s}(t - 10372T_s)\right)), & 10370T_s \leq t < 10372T_s \\ 0, & \text{otherwise} \end{cases} \quad (15)$$

The modulated signal is shown in [Figure 7](#). Timing of modulated signal transmission is as described in [5.1.3](#), i.e. the modulated signals are transmitted in the time intervals of T_1 to T_2 as shown in [Figure 3](#).



Key

- 1 filter ripple (4 symbols)
- 2 TSS (2 symbols)
- 3 PTS1 (36 symbols)
- 4 data (730 symbols)
- 5 PTS1 (36 symbols)
- 6 data (730 symbols)
- 7 PTS1 (36 symbols)
- 8 data (730 symbols)
- 9 PTS1 (36 symbols)
- 10 data (336 symbols)
- 11 TSS (2 symbols)
- 12 filter ripple (4 symbols)

^a Modulated signal (10372 DQPSK symbol).

Figure 7 — Modulated signal structure

5.4 Physical layer procedure

5.4.1 Synchronization

All messages shall be transmitted based on UTC time. All times are measured based on UTC.

The synchronization mode of the unit includes 'A sync', 'B sync' and 'C sync'.

- A sync is synchronization obtained from UTC.
- B sync is secondary synchronization acquired from the synchronization signal of the A sync unit.
- C sync is sync status within 20 seconds after sudden loss of sync in A or B sync mode.

A sync unit shall know the date, hour, minute, second, slot number.

The time error of A sync shall be within $\pm 0,4 \mu\text{s}$. The time error of B sync shall be within $\pm 4 \mu\text{s}$. The time error of C sync shall be within $\pm 5 \mu\text{s}$.

The frequency error of A sync shall be within $\pm 0,1 \text{ ppm}$. The frequency error of the B sync shall be within $\pm 0,2 \text{ ppm}$. The frequency error of the C sync shall be within $\pm 0,3 \text{ ppm}$.

5.4.2 Subchannel power

The maximum power P_{maxVCH} of the VSCH is received as $\text{UPtoDL.InfoPowerParamVCH}$ from an upper layer. The maximum transmission power and minimum transmission power of each VSCH are received as $\text{UPtoDL.InfoPowerParamVCHsub}$ from the upper layer. The power control of each VSCH is described in the resource allocation procedure.

5.4.3 Measurements

The physical layer shall have the ability to measure the following parameters. The received signal power of a tone subslot, the received signal power of a data slot, and propagation delay time of the received data signal shall be measured. The receiving power determination point shall be the receiving antenna connector.

5.4.4 Coexistence operation

If the hardware of shared communication described in ISO/IEC 4005-2 and the hardware of control communication described in ISO/IEC 4005-3 and the hardware of video communication described in this document are completely physically isolated and do not affect each other at all, it is possible that coexistence operation is not performed, which is implementation dependent. In general, the three communications affect each other, and in this case, the following coexistence operation shall be performed.

The TX operation of a shared slot includes the TX of the corresponding shared slot and the TX operation in the mapped tone subslot set. The TX operation of a control communication includes TX of the mapped tone subslot set and TX in the subchannel for transmitting control data. The TX operation of video communication includes TX of a mapped tone subslot set and TX in a subchannel for transmitting video data.

When a UA periodically broadcasts its information to a shared slot of a shared channel, a shared slot and a set of tone subslots mapped to the shared slot generally require 1 slot and 4 slots, respectively, for TX operation. If the TX operation of the shared slot used for mandatory periodic broadcasting and the TX operation of the video channel overlap, the TX operation of the shared slot shall be performed.

A control subchannel (CSCH) and a VSCH shall be allocated so that they do not overlap in time.

The TX time of the tone subslot set mapped with mandatory periodically broadcasted shared slot, the TX time of the tone subslot set mapped with the CSCH, and the TX time of the tone subslot set mapped

with the VSCH shall not overlap each other. If the video tone slot block type is TSBtype0, the video tone subslot set and the shared tone subslot set can be located in the same TSB. In this case, the two tone subslot set numbers shall be different. If the video TSB type is not TSBtype0, the video tone subslot set and the shared tone subslot set cannot be located in the same TSB.

The TX operation time of the tone subslot set mapped with a CSCH may overlap the TX time of a VSCH, and in this case, the corresponding video slot cannot be transmitted. The TX operation time of the tone subslot set mapped with a VSCH may overlap with the slot TX time of a CSCH, and in this case, the corresponding control slot cannot be transmitted.

6 Data link layer

6.1 General

The data link layer allocates subchannels consisting of 25 slots to controllers and UAs. The controller can use this subchannel to receive video from the UA. In this case, the controller shall include a video channel receiver. The representative application service of video communication is that the controller receives video from the UA, but it is possible to provide other services through the formed video link. This is determined at the upper layer.

The process of using the VSCH is almost the same as the process of using the CSCH and shown in [Figure 8](#).

- negotiation of subchannel number to be allocated;
- competition for allocation and generated link confirmation;
- occupation and management of subchannels;
- subchannel return or reallocation.

Firstly, the UA and the controller each generate a map of the available subchannels. The controller selects one of the subchannels available together and the controller transfers the selected subchannel number to the UA where the subchannel negotiation is performed by the SC DLL or the CC DLL.

After that, the UA and the controller attempt to allocate subchannel at the same time. Subchannel can be allocated only when the UA and the controller succeed in allocation at the same time. The controller shall confirm whether a link is generated.

If the subchannel allocation is successful, the UA and the controller simultaneously perform slot clearing to occupy the subchannel. While occupying a subchannel, the UA and the controller constantly check for collisions of subchannel resources. They also calculate the amount of interference from neighboring channels.

If collision of subchannel resources or interference with neighboring channels exceeding the threshold is detected, the UA and the controller reallocate the subchannel. To do this, the UA and the controller decide which subchannels to reallocate and perform allocation competition on that subchannel.

The UA and the controller return the subchannel when they can no longer maintain or need to maintain them.

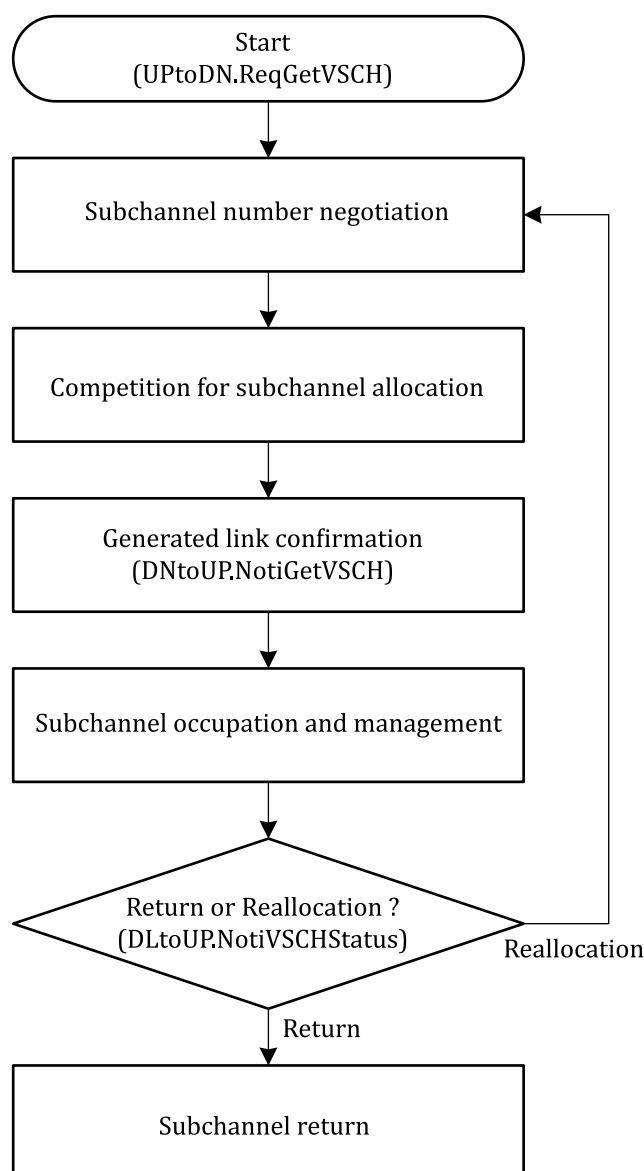


Figure 8 — Subchannel use procedure

6.2 Channel mapping and measurements

6.2.1 General

Allocating subchannel resources is performed by tone channel. One subslot set in a tone channel and one subchannel have a mapping relationship. When one tone subslot set is allocated, a subchannel mapped thereto is allocated.

In order for the UA and the controller to allocate a subchannel, the UA and the controller shall find subchannels that can be allocated at the same time. To this end, the UA and the controller determine the allocable subchannels by calculating the interference power for each subchannel.

6.2.2 Mapping of communication resources and subslot sets

The competition for allocating a subchannel is performed in the subslot set mapped thereto. Subslot sets are mapped to subchannels.