
**Telecommunications and exchange
between information technology
systems — Requirements for local and
metropolitan area networks —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 3: Media access control
parameters for 50 Gb/s and physical
layers and management parameters
for 50 Gb/s, 100 Gb/s, and 200 Gb/s
operation**

*Télécommunications et échange entre systèmes informatiques —
Exigences pour les réseaux locaux et métropolitains —*

Partie 3: Norme pour Ethernet

*AMENDEMENT 3: Paramètres de commande d'accès media pour
50 Gb/s et couches physiques et paramètres de gestion pour
fonctionnement à 50 Gb/s, 100 Gb/s et 200 Gb/s*



Reference number
ISO/IEC/IEEE 8802-3:2021/Amd.3:2021(E)

Documents
Document Sharing Hub
© IEEE 2019



COPYRIGHT PROTECTED DOCUMENT

© IEEE 2019

All rights reserved. Unless otherwise specified, or required in the context of its implementation, no part of this publication may be reproduced or utilized otherwise in any form or by any means, electronic or mechanical, including photocopying, or posting on the internet or an intranet, without prior written permission. Permission can be requested from IEEE at the address below.

Institute of Electrical and Electronics Engineers, Inc
3 Park Avenue, New York
NY 10016-5997, USA

Email: stds.ipr@ieee.org
Website: www.ieee.org

Published in Switzerland

Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO/IEC documents should be noted.

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards.

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. ISO and IEC shall not be held responsible for identifying any or all such patent rights. Details of any patent rights identified during the development of the document will be in the Introduction and/or on the ISO list of patent declarations received (see www.iso.org/patents) or the IEC list of patent declarations received (see patents.iec.ch).

Any trade name used in this document is information given for the convenience of users and does not constitute an endorsement.

For an explanation of the voluntary nature of standards, the meaning of ISO specific terms and expressions related to conformity assessment, as well as information about ISO's adherence to the World Trade Organization (WTO) principles in the Technical Barriers to Trade (TBT), see www.iso.org/iso/foreword.html. In the IEC, see www.iec.ch/understanding-standards.

ISO/IEC/IEEE 8802-3:2021/Amd.3 was prepared by the LAN/MAN of the IEEE Computer Society (as IEEE Std 802.3cd-2018) and drafted in accordance with its editorial rules. It was adopted, under the “fast-track procedure” defined in the Partner Standards Development Organization cooperation agreement between ISO and IEEE, by Joint Technical Committee ISO/IEC JTC 1, *Information technology*, Subcommittee SC 6, *Telecommunications and information exchange between systems*.

A list of all parts in the ISO/IEC/IEEE 8802 series can be found on the ISO and IEC websites.

Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html and www.iec.ch/national-committees.

IEEE Std 802.3cd™-2018
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018
and IEEE Std 802.3bt™-2018)

IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

Sponsor
LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 5 December 2018
IEEE-SA Standards Board

Abstract: Clause 131 through Clause 140 and Annex 135A through Annex 136D are added to IEEE Std 802.3-2018 by this amendment to specify IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

Keywords: 50GAUI-1, 50GAUI-2, 50GBASE-CR, 50GBASE-FR, 50GBASE-KR, 50GBASE-LR, 50GBASE-SR, 50 Gigabit Ethernet, 50GMII, 100GAUI-2, 100GAUI-4, 100GBASE-CR2, 100GBASE-DR, 100GBASE-KR2, 100GBASE-SR2, 100 Gigabit Ethernet, 200GBASE-CR4, 200GBASE-KR4, 200GBASE-SR4, 200 Gigabit Ethernet, amendment, EEE, Energy-Efficient Ethernet, Ethernet, FEC, forward error correction, IEEE 802.3™, IEEE 802.3cd™, LAUI-2, MMF, SMF

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2019 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 15 February 2019. Printed in the United States of America.

IEEE and 802 are registered trademarks in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

PDF: ISBN 978-1-5044-5357-8 STD23441
Print: ISBN 978-1-5044-5358-5 STDPD23441

IEEE prohibits discrimination, harassment and bullying.

For more information, visit <http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html>.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page, appear in all standards and may be found under the heading “Important Notices and Disclaimers Concerning IEEE Standards Documents.” They can also be obtained on request from IEEE or viewed at <http://standards.ieee.org/ipr/disclaimers.html>.

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents (standards, recommended practices, and guides), both full-use and trial-use, are developed within IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (“IEEE-SA”) Standards Board. IEEE (“the Institute”) develops its standards through a consensus development process, approved by the American National Standards Institute (“ANSI”), which brings together volunteers representing varied viewpoints and interests to achieve the final product. IEEE Standards are documents developed through scientific, academic, and industry-based technical working groups. Volunteers in IEEE working groups are not necessarily members of the Institute and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE Standards do not guarantee or ensure safety, security, health, or environmental protection, or ensure against interference with or from other devices or networks. Implementers and users of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.

IEEE does not warrant or represent the accuracy or content of the material contained in its standards, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, effectiveness, currency, or completeness of material. In addition, IEEE disclaims any and all conditions relating to: results; and workmanlike effort. IEEE standards documents are supplied “AS IS” and “WITH ALL FAULTS.”

Use of an IEEE standard is wholly voluntary. The existence of an IEEE standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE should be considered the approved IEEE standard.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE-SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, or be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that his or her views should be considered the personal views of that individual rather than the formal position of IEEE.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party, regardless of membership affiliation with IEEE. However, IEEE does not provide consulting information or advice pertaining to IEEE Standards documents. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to comments or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in revisions to an IEEE standard is welcome to join the relevant IEEE working group.

Comments on standards should be submitted to the following address:

Secretary, IEEE-SA Standards Board
445 Hoes Lane
Piscataway, NJ 08854 USA

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not imply compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under U.S. and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, IEEE does not waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate fee, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every ten years. When a document is more than ten years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit the IEEE-SA Website at <http://ieeexplore.ieee.org> or contact IEEE at the address listed previously. For more information about the IEEE SA or IEEE's standards development process, visit the IEEE-SA Website at <http://standards.ieee.org>.

Errata

Errata, if any, for all IEEE standards can be accessed on the IEEE-SA Website at the following URL: <http://standards.ieee.org/findstds/errata/index.html>. Users are encouraged to check this URL for errata periodically.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE-SA Website at <http://standards.ieee.org/about/sasb/patcom/patents.html>. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

Participants

The following individuals were officers and members of the IEEE 802.3 Working Group at the beginning of the IEEE P802.3cd Working Group ballot.

David J. Law, *IEEE 802.3 Working Group Chair*
Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

Mark Nowell, *IEEE P802.3cd Task Force Chair*
Matt Brown, *IEEE P802.3cd Task Force Editor-in-Chief*
Arthur Marris, *IEEE P802.3cd Task Force Editor*
Gary Nicholl, *IEEE P802.3cd Task Force Editor*
Adee Ran, *IEEE P802.3cd Task Force Editor*
Jonathan King,¹ *IEEE P802.3cd Task Force Editor*
Peter Stassar, *IEEE P802.3cd Task Force Editor*

Justin Abbott
David Abramson
Dale Amason
Eric Baden
Amrik Bains
Thananya Baldwin
Denis Beaudoin
Christian Beia
Vipul Bhatt
William Bliss
Mark Bohm
Brad Booth
Martin Bouda
David Brandt
Ralf-Peter Braun
Theodore Brillhart
Paul Brooks
Phillip Brownlee
Chris Bullock
Jairo Bustos Heredia
Adrian Butter
Anthony Calbone
Clark Carty
Craig Chabot
Mandeep Chadha
David Chalupsky
Jacky Chang
Xin Chang
Chan Chen
Weiyang Cheng
Golam Choudhury
Keng Hua Chuang
Christopher R. Cole
John D'Ambrosia
Piers J. G. Dawe
Fred Dawson

Eric DiBiaso
John Dillard
Chris Diminico
Curtis Donahue
Michael Dudek
Frank Effenberger
John Ewen
Ramin Farjad
Shahar Feldman
Matthias Fritsche
Richard Frosch
Andrew Gardner
Ali Ghiasi
Steven Gorshe
Steffen Graber
Olaf Grau
Robert M. Grow
Yong Guo
Mark Gustlin
Marek Hajduczenia
Tomohiro Hashimoto
Akinori Hayakawa
Rajmohan Hegde
David Hess
Yasuo Hidaka
David Hoglund
Rita Horner
Bernd Hormmeyer
Xi Huang
Xingang Huang
Yasuhiro Hyakutake
Jonathan Ingham
Kazuhiko Ishibe
Hideki Isono
Tom Issenhuth
Kenneth Jackson

Andrew Jimenez
John Johnson
Chad Jones
Peter Jones
Upen Kareti
Yasuaki Kawatsu
Yongbum Kim
Mark Kimber
Scott Kipp
Michael Klempa
Curtis Knittle
Shigeru Kobayashi
Paul Kolesar
Toshihiko Kusano
Hans Lackner
Jeffrey Lapak
Mark Laubach
Greg Le Cheminant
Hanan Leizerovich
David Lewis
Jon Lewis
Mike Peng Li
Robert Lingle
Hai-Feng Liu
Zhenyu Liu
Moiz Lokhandwala
Miklos Lukacs
Kent Lusted
Zahy Madgar
Jeffery Maki
David Malicoat
Takeo Masuda
Kirsten Matheus
Erdem Matoglu

¹Not a member of the IEEE 802.3 working group at the beginning of the working group ballot.

Mick McCarthy	Alon Regev	Yoshihiro Tsukamoto
Brett McClellan	Duane Remein	Ed Ulrichs
Thomas McDermott	Salvatore Rotolo	Alexander Umnov
John McDonough	Sam Sambasivan	Sterling A. Vaden
Larry McMillan	Edward Sayre	Stefano Valle
Greg McSorley	Fred Schindler	Paul Vanderlaan
Marcel Medina	Masood Shariff	Dylan Walker
Richard Mei	Kapil Shrikhande	Roy Wang
Richard Mellitz	Jeff Slavick	Tongtong Wang
Phil Miguelez	Daniel Smith	Xinyuan Wang
Paul Mooney	Scott Sommers	Matthias Wendt
Ron Muir Dale Murray	Yoshiaki Sone	Oded Wertheim
Henry Muyschondt	Bryan Sparrowhawk	Natalie Wienckowski
Edward Nakamoto	Atul Srivastava	Ludwig Winkel
Kevin Noll	Heath Stewart	Peter Wu
David Ofelt	David Stover	Dayin Xu
Thomas Palkert	Ken-Ichi Suzuki	Yu Xu
Sujan Pandey	Steve Swanson	Lennart Yseboodt
Sesha Panguluri	Andre Szczepanek	Hayato Yuki
Earl Parsons	William Szeto	Andrew Zambell
Wanquan Peng	Bharat Tailor	Huanlin Zhang
Ruben Perez De Aranda Alonso	Takayuki Tajima	Qiwen Zhong
Michael Peters	Tomoo Takahara	Yan Zhuang
Jean Picard	Kohichi Tamura	George Zimmerman
David Piehler	Nathan Tracy	Helge Zinner
Rick Pimpinella	Matthew Traverso	Pavel Zivny
William Powell	David Tremblay	
Rick Rabinovich	Stephen Trowbridge	

The following members of the individual balloting committee voted on this amendment. Balloters may have voted for approval, disapproval, or abstention.

Thomas Alexander	Brian Franchuk	Hyeong Ho Lee
Richard Alfvén	Avraham Freedman	Hanan Leizerovich
Arne Alping	Yukihiro Fujimoto	David Lewis
Pete Anslow	Zhigang Gong	Jon Lewis
Butch Anton	Eric W. Gray	Robert Lingle
Eric Baden	Randall Groves	Hai-Feng Liu
John Ballingall	Mark Gustlin	Kent Lusted
Ralf-Peter Braun	Adam Healey	Michael Lynch
Nancy Bravin	Marco Hernandez	Elvis Maculuba
Theodore Brillhart	David Hess	Valerie Maguire
Matt Brown	Yasuo Hidaka	Jeffery Maki
Demetrio Bucaneg	Werner Hoelzl	Arthur Marris
Gary Burrell	Rita Horner	Michael Maytum
Jairo Bustos Heredia	Noriyuki Ikeuchi	Mick McCarthy
William Byrd	Sergiu Iordanescu	Brett McClellan
John Calvin	Osamu Ishida	Thomas McDermott
Steven B. Carlson	Atsushi Ito	Richard Mellitz
Juan Carreon	Raj Jain	Tremont Miao
Clark Carty	SangKwon Jeong	Charles Moorwood
Chan Chen	Peter Jones	Rick Murphy
Keith Chow	Manabu Kagami	Michael Newman
Keng Hua Chuang	Piotr Karocki	Charles Ngethe
Charles Cook	Stuart Kerry	Gary Nicholl
Piers J. G. Dawe	Yongbum Kim	Nick S. A. Nikjoo
Stephen Didde	Jonathan King	Mark Nowell
Michael Dudek	Paul Kolesar	Satoshi Obara
Sourav Dutta	Mark Laubach	Thomas Palkert
Jason Ellison	David J. Law	Bansi Patel

Arumugam Paventhan
Michael Peters
David Piehler
Rick Pimpinella
Adee Ran
R. K. Rannow
Alon Regev
Maximilian Riegel
Robert Robinson
Alexander Rysin
Toshiaki Sakai
Kapil Shrikhande
Jason Shriver
Jeff Slavick
Daniel Smith
Thomas Starai

Peter Stassar
Robert Stone
Walter Struppler
Mitsutoshi Sugawara
Junqing Sun
Patrik Sundstrom
Andre Szczepanek
Kohichi Tamura
David Thompson
Geoffrey Thompson
Michael Thompson
David Tremblay
Stephen Trowbridge
Mark-Rene Uchida
Alexander Umnov
Paul Vanderlaan

Dmitri Varsanofiev
George Vlantis
Khurram Waheed
Lisa Ward
Keith Waters
Oded Wertheim
Andreas Wolf
Chun Yu Charles Wong
Peter Wu
Xin Wu
Jun Xu
Adrian Young
Oren Yuen
Andrew Zambell
Zhen Zhou
Pavel Zivny

When the IEEE-SA Standards Board approved this amendment on 5 December 2018, it had the following membership:

Jean-Philippe Faure, *Chair*
Gary Hoffman, *Vice Chair*
John D. Kulick, *Past Chair*
Konstantinos Karachalios, *Secretary*

Ted Burse
Guido R. Hiertz
Christel Hunter
Joseph L. Koepfinger*
Thomas Koshy
Hung Ling
Dong Liu

Xiaohui Liu
Kevin Lu
Daleep Mohla
Andrew Myles
Paul Nikolich
Ronald C. Petersen
Annette D. Reilly

Robby Robson
Dorothy Stanley
Mehmet Ulema
Phil Wennblom
Philip Winston
Howard Wolfman
Jingyi Zhou

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 802.3cd-2018, IEEE Standard for Ethernet. Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3cd-2018, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, Annex 128C, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

A companion document, IEEE Std 802.3.1, describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

1. Introduction.....	35
1.1 Overview.....	35
1.1.3 Architectural perspectives.....	35
1.1.3.2 Compatibility interfaces.....	35
1.3 Normative references.....	35
1.4 Definitions.....	36
1.5 Abbreviations.....	37
4. Media Access Control.....	38
4.4 Specific implementations.....	38
4.4.2 MAC parameters.....	38
30. Management.....	39
30.3 Layer management for DTEs.....	39
30.3.2 PHY device managed object class.....	39
30.3.2.1 PHY device attributes.....	39
30.3.2.1.2 aPhyType.....	39
30.3.2.1.3 aPhyTypeList.....	39
30.3.2.1.5 aSymbolErrorDuringCarrier.....	39
30.5 Layer management for medium attachment units (MAUs).....	39
30.5.1 MAU managed object class.....	39
30.5.1.1 MAU attributes.....	39
30.5.1.1.2 aMAUType.....	39
30.5.1.1.4 aMediaAvailable.....	40
30.5.1.1.11 aBIPErrCount.....	41
30.5.1.1.12 aLaneMapping.....	41
30.5.1.1.17 aFECCorrectedBlocks.....	41
30.5.1.1.18 aFECUncorrectableBlocks.....	41
30.5.1.1.26 aRSFECBIPErrCount.....	42
30.5.1.1.27 aRSFECLaneMapping.....	42
30.5.1.1.29 aRSFECBypassIndicationAbility.....	42
30.5.1.1.31 aRSFECBypassIndicationEnable.....	42
30.6 Management for link Auto-Negotiation.....	43
30.6.1 Auto-Negotiation managed object class.....	43
30.6.1.1 Auto-Negotiation attributes.....	43
30.6.1.1.5 aAutoNegLocalTechnologyAbility.....	43
45. Management Data Input/Output (MDIO) Interface.....	44
45.2 MDIO Interface Registers.....	44
45.2.1 PMA/PMD registers.....	44
45.2.1.1 PMA/PMD control 1 register (Register 1.0).....	46
45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2).....	46
45.2.1.2 PMA/PMD status 1 register (Register 1.1).....	46
45.2.1.2.3 Fault (1.1.7).....	46
45.2.1.4 PMA/PMD speed ability (Register 1.4).....	47
45.2.1.4.12a 50G capable (1.4.3).....	47
45.2.1.6 PMA/PMD control 2 register (Register 1.7).....	47
45.2.1.6.3 PMA/PMD type selection (1.7.6:0).....	48

45.2.1.7 PMA/PMD status 2 register (Register 1.8).....	48
45.2.1.7.4 Transmit fault (1.8.11).....	48
45.2.1.7.5 Receive fault (1.8.10).....	49
45.2.1.8 PMD transmit disable register (Register 1.9).....	49
45.2.1.17a 50G PMA/PMD extended ability (Register 1.20).....	50
45.2.1.17a.1 50G PMA remote loopback ability (1.20.15).....	50
45.2.1.17a.2 50GBASE-LR ability (1.20.4).....	50
45.2.1.17a.3 50GBASE-FR ability (1.20.3).....	51
45.2.1.17a.4 50GBASE-SR ability (1.20.2).....	51
45.2.1.17a.5 50GBASE-CR ability (1.20.1).....	51
45.2.1.17a.6 50GBASE-KR ability (1.20.0).....	51
45.2.1.21a PMA/PMD extended ability 2 (Register 1.25).....	51
45.2.1.21a.1 50G extended abilities (1.25.0).....	51
45.2.1.89 BASE-R PMD control register (Register 1.150).....	52
45.2.1.90 BASE-R PMD status register (Register 1.151).....	52
45.2.1.90.1 Receiver status 0 (1.151.0).....	52
45.2.1.90.2 Frame lock 0 (1.151.1).....	52
45.2.1.90.3 Start-up protocol status 0 (1.151.2).....	52
45.2.1.90.4 Training failure 0 (1.151.3).....	52
45.2.1.110 RS-FEC control register (Register 1.200).....	53
45.2.1.110.a FEC degraded SER enable (1.200.4).....	53
45.2.1.110.b Four-lane PMD (1.200.3).....	53
45.2.1.110.2 FEC bypass indication enable (1.200.1).....	54
45.2.1.111 RS-FEC status register (Register 1.201).....	54
45.2.1.111.1 PCS align status (1.201.15).....	54
45.2.1.111.2 RS-FEC align status (1.201.14).....	54
45.2.1.111.5 FEC AM lock 1 (1.201.9).....	55
45.2.1.111.6 FEC AM lock 0 (1.201.8).....	55
45.2.1.111.7a FEC degraded SER (1.201.4).....	55
45.2.1.111.7b FEC degraded SER ability (1.201.3).....	55
45.2.1.111.8 RS-FEC high SER (1.201.2).....	55
45.2.1.111.9 FEC bypass indication ability (1.201.1).....	55
45.2.1.117 RS-FEC BIP error counter lane 0 (Register 1.230).....	55
45.2.1.129 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 register (Register 1.500).....	56
45.2.1.129.1 Request flag (1.500.15).....	57
45.2.1.129.2 Post-cursor request (1.500.14:12).....	57
45.2.1.129.3 Pre-cursor request (1.500.11:10).....	57
45.2.1.129.4 Post-cursor remote setting (1.500.9:7).....	57
45.2.1.129.5 Pre-cursor remote setting (1.500.6:5).....	58
45.2.1.129.6 Post-cursor local setting (1.500.4:2).....	58
45.2.1.129.7 Pre-cursor local setting (1.500.1:0).....	58
45.2.1.130 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 1 through lane 15 registers (Registers 1.501 through 1.515).....	58
45.2.1.131 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 register (Register 1.516).....	58
45.2.1.131.1 Request flag (1.516.15).....	60
45.2.1.131.2 Post-cursor request (1.516.14:12).....	60
45.2.1.131.3 Pre-cursor request (1.516.11:10).....	60
45.2.1.131.4 Post-cursor remote setting (1.516.9:7).....	60
45.2.1.131.5 Pre-cursor remote setting (1.516.6:5).....	60
45.2.1.131.6 Post-cursor local setting (1.516.4:2).....	60
45.2.1.131.7 Pre-cursor local setting (1.516.1:0).....	61

45.2.1.132 50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 1 through lane 15 registers (Registers 1.517 through 1.531).....	61
45.2.1.132a PMA precoder control Tx output (Register 1.600).....	61
45.2.1.132a.1 Lane 3 Tx output precoder enable (1.600.3).....	61
45.2.1.132a.2 Lane 2 Tx output precoder enable (1.600.2).....	61
45.2.1.132a.3 Lane 1 Tx output precoder enable (1.600.1).....	62
45.2.1.132a.4 Lane 0 Tx output precoder enable (1.600.0).....	62
45.2.1.132b PMA precoder control Rx input (Register 1.601).....	62
45.2.1.132b.1 Lane 3 Rx input precoder enable (1.601.3).....	62
45.2.1.132b.2 Lane 2 Rx input precoder enable (1.601.2).....	62
45.2.1.132b.3 Lane 1 Rx input precoder enable (1.601.1).....	62
45.2.1.132b.4 Lane 0 Rx input precoder enable (1.601.0).....	62
45.2.1.132c PMA precoder control Rx output (Register 1.602).....	63
45.2.1.132c.1 Lane 1 Rx output precoder enable (1.602.1).....	63
45.2.1.132c.2 Lane 0 Rx output precoder enable (1.602.0).....	63
45.2.1.132d PMA precoder control Tx input (Register 1.603).....	63
45.2.1.132d.1 Lane 1 Tx input precoder enable (1.603.1).....	63
45.2.1.132d.2 Lane 0 Tx input precoder enable (1.603.0).....	63
45.2.1.132e PMA precoder request flag (Register 1.604).....	64
45.2.1.132e.1 Tx input precoder request flag (1.604.1).....	64
45.2.1.132e.2 Rx input precoder request flag (1.604.0).....	64
45.2.1.132f PMA precoder request Rx input status (Register 1.605).....	64
45.2.1.132f.1 Lane 1 Rx input precoder request status (1.605.1).....	64
45.2.1.132f.2 Lane 0 Rx input precoder request status (1.605.0).....	64
45.2.1.132g PMA precoder request Tx input status (Register 1.606).....	65
45.2.1.132g.1 Lane 1 Tx input precoder request status(1.606.1).....	65
45.2.1.132g.2 Lane 0 Tx input precoder request status (1.606.0).....	65
45.2.1.132h RS-FEC degraded SER activate threshold register (Register 1.650, 1.651).....	65
45.2.1.132i RS-FEC degraded SER deactivate threshold register (Register 1.652, 1.653).....	66
45.2.1.132j RS-FEC degraded SER interval register (Register 1.654, 1.655).....	66
45.2.1.135a BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers (Register 1.1120 through 1.1123).....	67
45.2.1.136a BASE-R PAM4 PMD training LP status, lane 0 through lane 3 registers (Register 1.1220 through 1.1223).....	68
45.2.1.137a BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers (Register 1.1320 through 1.1323).....	69
45.2.1.138a BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers (Register 1.1420 through 1.1423).....	70
45.2.1.139 PMD training pattern lanes 0 through 3 (Register 1.1450 through 1.1453).....	71
45.2.1.141 PRBS pattern testing control (Register 1.1501).....	71
45.2.3 PCS registers.....	72
45.2.3.1 PCS control 1 register (Register 3.0).....	72
45.2.3.2 PCS status 1 register (Register 3.1).....	72
45.2.3.2.7 PCS receive link status (3.1.2).....	72
45.2.3.4 PCS speed ability (Register 3.4).....	73
45.2.3.4.5a 50G capable (3.4.5).....	73
45.2.3.6 PCS control 2 register (Register 3.7).....	73
45.2.3.7 PCS status 2 register (Register 3.8).....	74
45.2.3.7.6a 50GBASE-R capable (3.8.8).....	74
45.2.3.10 EEE control and capability 1 (Register 3.20).....	74
45.2.3.10.a 50GBASE-R EEE fast wake supported (3.20.14).....	74
45.2.3.15 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32).....	75
45.2.3.15.1 BASE-R and MultiGBASE-T receive link status (3.32.12).....	75

45.2.3.15.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)	75
45.2.3.15.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)	75
45.2.3.16 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)	75
45.2.3.16.1 Latched block lock (3.33.15)	75
45.2.3.16.2 Latched high BER (3.33.14)	75
45.2.3.16.3 BER (3.33.13:8)	76
45.2.3.16.4 Errored blocks (3.33.7:0)	76
45.2.3.19 BASE-R PCS test-pattern control register (Register 3.42)	76
45.2.7 Auto-Negotiation registers	76
45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)	76
45.2.7.12.3 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15, 7.49.0, 7.49.1, 7.49.2)	76
45.2.7.12a Backplane Ethernet, BASE-R copper status 2 (Register 7.49)	77
45.2.7.12a.1 Negotiated Port Type	77
69. Introduction to Ethernet operation over electrical backplanes	78
69.1 Overview	78
69.1.1 Scope	78
69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model	78
69.2 Summary of Backplane Ethernet Sublayers	80
69.2.1 Reconciliation sublayer and media independent interfaces	80
69.2.3 Physical Layer signaling systems	80
69.3 Delay constraints	82
69.5 Protocol implementation conformance statement (PICS) proforma	82
73. Auto-Negotiation for backplane and copper cable assembly	83
73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model	83
73.5 DME transmission	83
73.5.1 DME electrical specifications	83
73.6 Link codeword encoding	84
73.6.4 Technology Ability Field	84
73.7 Receive function requirements	85
73.7.6 Priority Resolution function	85
73.10 State diagrams and variable definitions	86
73.10.1 State diagram variables	86
73.10.2 State diagram timers	87
78. Energy-Efficient Ethernet (EEE)	88
78.1 Overview	88
78.1.4 PHY types optionally supporting EEE	88
78.5 Communication link access latency	89
80. Introduction to 40 Gb/s and 100 Gb/s networks	90
80.1 Overview	90
80.1.3 Relationship of 40 Gigabit and 100 Gigabit Ethernet to the ISO OSI reference model	90
80.1.4 Nomenclature	91
80.1.5 Physical Layer signaling systems	92
80.2 Summary of 40 Gigabit and 100 Gigabit Ethernet sublayers	93
80.2.2 Physical Coding Sublayer (PCS)	93

80.2.3 Forward Error Correction (FEC) sublayers	93
80.2.4 Physical Medium Attachment (PMA) sublayer.....	94
80.2.5 Physical Medium Dependent (PMD) sublayer	94
80.2.6 Auto-Negotiation	94
80.4 Delay constraints.....	95
80.5 Skew constraints	96
80.7 Protocol implementation conformance statement (PICS) proforma.....	99
82. Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R	100
82.6 Auto-Negotiation	100
82.7 Protocol implementation conformance statement (PICS) proforma for Clause 82, Physical Coding Sublayer (PCS) for 64B/66B, type 40GBASE-R and 100GBASE-R.....	100
82.7.4 PICS proforma tables for PCS, type 40GBASE-R and 100GBASE-R	100
82.7.4.11 Auto-Negotiation for Backplane Ethernet functions	100
90. Ethernet support for time synchronization protocols.....	101
90.1 Introduction.....	101
91. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs	102
91.3 PMA compatibility	102
91.5 Functions within the RS-FEC sublayer	102
91.5.2 Transmit function.....	102
91.5.2.6 Alignment marker mapping and insertion	102
91.5.2.7 Reed-Solomon encoder.....	102
91.5.3 Receive function	103
91.5.3.3 Reed-Solomon decoder.....	103
91.5.3.3.1 FEC Degraded SER (optional)	103
91.6 RS-FEC MDIO function mapping	104
91.6.2a four_lane_pmd	104
91.6.2b FEC_degraded_SER_enable.....	104
91.6.2c FEC_degraded_SER_activate_threshold	105
91.6.2d FEC_degraded_SER_deactivate_threshold	105
91.6.2e FEC_degraded_SER_interval	105
91.6.5a FEC_degraded_SER_ability	105
91.6.5b FEC_degraded_SER	105
91.7 Protocol implementation conformance statement (PICS) proforma for Clause 91, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs.....	105
91.7.3 Major capabilities/options.....	105
91.7.4 PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 100GBASE-R PHYs	106
91.7.4.1 Transmit function.....	106
91.7.4.2 Receive function	106
116. Introduction to 200 Gb/s and 400 Gb/s networks	108
116.1 Overview.....	108
116.1.2 Relationship of 200 Gigabit and 400 Gigabit Ethernet to the ISO OSI reference model	108
116.1.3 Nomenclature.....	108
116.1.4 Physical Layer signaling systems	108
116.2 Summary of 200 Gigabit and 400 Gigabit Ethernet sublayers	110

116.2.5 Physical Medium Dependent (PMD) sublayer	110
116.4 Delay constraints.....	110
119. Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R	111
119.5a Auto-Negotiation	111
119.6 Protocol implementation conformance statement (PICS) proforma for Clause 119, Physical Coding Sublayer (PCS) for 64B/66B, type 200GBASE-R and 400GBASE-R.....	111
119.6.4 PICS proforma tables for Physical Coding Sublayer (PCS) 64B/66B, type 200GBASE-R and 400GBASE-R	111
119.6.4.12 Auto-Negotiation for Backplane Ethernet functions	111
120. Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R.....	112
120.5 Functions within the PMA	112
120.5.7 PAM4 Encoding Gray mapping for PAM4 encoded lanes.....	112
120.5.7.1 Gray mapping for PAM4 encoded lanes.....	112
120.5.7.2 Precoding for PAM4 encoded lanes	112
120.6 PMA MDIO function mapping.....	112
120.7 Protocol implementation conformance statement (PICS) proforma for Clause 120, Physical Medium Attachment (PMA) sublayer, type 200GBASE-R and 400GBASE-R	113
120.7.7 Encoding	113
131. Introduction to 50 Gb/s networks	114
131.1 Overview.....	114
131.1.1 Scope.....	114
131.1.2 Relationship of 50 Gigabit Ethernet to the ISO OSI reference model.....	114
131.1.3 Nomenclature.....	114
131.1.4 Physical Layer signaling systems	116
131.2 Summary of 50 Gigabit Ethernet sublayers	117
131.2.1 Reconciliation Sublayer (RS) and Media Independent Interface (50GMII).....	117
131.2.2 Physical Coding Sublayer (PCS)	117
131.2.3 Forward Error Correction (FEC) sublayer.....	117
131.2.4 Physical Medium Attachment (PMA) sublayer.....	117
131.2.5 Physical Medium Dependent (PMD) sublayer	117
131.2.6 Management interface (MDIO/MDC)	117
131.2.7 Management.....	118
131.3 Service interface specification method and notation	118
131.3.1 Inter-sublayer service interface.....	118
131.3.2 Instances of the Inter-sublayer service interface.....	118
131.3.3 Semantics of inter-sublayer service interface primitives	118
131.4 Delay constraints.....	120
131.5 Skew constraints	120
131.6 State diagrams	123
131.7 Protocol implementation conformance statement (PICS) proforma.....	123
132. Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation ...	124
132.1 Overview.....	124
132.1.1 Summary of major concepts	124
132.1.2 Application.....	124
132.1.3 Rate of operation.....	124
132.1.4 Delay constraints.....	125

132.1.5 Allocation of functions	126
132.1.6 50GMII structure	126
132.1.7 Mapping of 50GMII signals to PLS service primitives	126
132.2 50GMII data stream	126
132.3 50GMII functional specifications	126
132.4 LPI assertion and detection	126
132.5 Protocol implementation conformance statement (PICS) proforma for Clause 132, Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation	127
132.5.1 Introduction	127
132.5.2 Identification	127
132.5.2.1 Implementation identification	127
132.5.2.2 Protocol summary	127
132.5.2.3 Major capabilities/options	128
132.5.3 PICS proforma tables for Reconciliation Sublayer (RS) and Media Independent Interface (50GMII) for 50 Gb/s operation	128
132.5.3.1 General	128
132.5.3.2 Mapping of PLS service primitives	128
133. Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R	129
133.1 Overview	129
133.1.1 Scope	129
133.1.2 Relationship of 50GBASE-R to other standards	129
133.1.3 Summary of 50GBASE-R sublayers	129
133.1.3.1 Physical Coding Sublayer (PCS)	129
133.1.4 Inter-sublayer interfaces	129
133.1.4.1 PCS service interface (50GMII)	129
133.1.4.2 Forward Error Correction (FEC) or Physical Medium Attachment (PMA) service interface	130
133.1.5 Functional block diagram	131
133.2 Physical Coding Sublayer (PCS)	132
133.2.1 Functions within the PCS	132
133.2.2 Alignment marker insertion	132
133.2.3 PCS lane deskew	133
133.2.4 Detailed functions and state diagrams	133
133.3 Delay constraints	133
133.4 Auto-Negotiation	133
133.5 Protocol implementation conformance statement (PICS) proforma for Clause 133, Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R	134
133.5.1 Introduction	134
133.5.2 Identification	134
133.5.2.1 Implementation identification	134
133.5.2.2 Protocol summary	134
133.5.3 Major capabilities/options	135
133.5.4 PICS proforma tables for Physical Coding Sublayer (PCS) for 64B/66B, type 50GBASE-R	135
133.5.4.1 Coding rules	135
133.5.4.2 Scrambler and Descrambler	136
133.5.4.3 Deskew and Reordering	136
133.5.4.4 Alignment Markers	136
133.5.4.5 Test-pattern modes	136
133.5.4.6 Bit order	137
133.5.4.7 Management	137

133.5.4.8 State diagrams.....	137
133.5.4.9 Loopback	138
133.5.4.10 Delay constraints.....	138
133.5.4.11 Auto-Negotiation for Backplane Ethernet functions	138
134. Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs	139
134.1 Overview.....	139
134.1.1 Scope.....	139
134.1.2 Position of RS-FEC in the 50GBASE-R sublayers	139
134.2 FEC service interface.....	139
134.3 PMA compatibility	140
134.4 Delay constraints.....	141
134.5 Functions within the RS-FEC sublayer	141
134.5.1 Functional block diagram	141
134.5.2 Transmit function.....	141
134.5.2.1 PCS Lane block synchronization.....	141
134.5.2.2 PCS Alignment lock and deskew.....	141
134.5.2.3 PCS Lane reorder.....	141
134.5.2.4 Alignment marker removal.....	141
134.5.2.5 64B/66B to 256B/257B transcoder.....	142
134.5.2.6 Alignment marker mapping and insertion	143
134.5.2.7 Reed-Solomon encoder.....	144
134.5.2.8 Symbol distribution.....	144
134.5.2.9 Transmit bit ordering	144
134.5.3 Receive function	144
134.5.3.1 Alignment lock and deskew	144
134.5.3.2 FEC Lane reorder.....	146
134.5.3.3 Reed-Solomon decoder.....	146
134.5.3.3.1 FEC Error indication bypass (optional)	146
134.5.3.3.2 FEC Degraded SER (optional)	147
134.5.3.4 Alignment marker removal.....	147
134.5.3.5 256B/257B to 64B/66B transcoder.....	147
134.5.3.6 Block distribution	147
134.5.3.7 Alignment marker mapping and insertion	147
134.5.3.8 Receive bit ordering.....	148
134.5.4 Detailed functions and state diagrams	148
134.5.4.1 State diagram conventions	148
134.5.4.2 State variables	150
134.5.4.2.1 Variables	150
134.5.4.2.2 Functions.....	150
134.5.4.2.3 Counters	150
134.5.4.3 State diagrams.....	150
134.6 RS-FEC MDIO function mapping.....	151
134.6.1 FEC_bypass_indication_enable.....	152
134.6.2 FEC_degraded_SER_enable.....	152
134.6.3 FEC_degraded_SER_activate_threshold.....	152
134.6.4 FEC_degraded_SER_deactivate_threshold.....	152
134.6.5 FEC_degraded_SER_interval.....	152
134.6.6 FEC_bypass_indication_ability.....	152
134.6.7 hi_ser.....	153
134.6.8 FEC_degraded_SER_ability.....	153
134.6.9 FEC_degraded_SER.....	153
134.6.10 fec_optional_states.....	153

134.6.11	amps_lock<x>	153
134.6.12	fec_align_status	153
134.6.13	FEC_corrected_cw_counter	153
134.6.14	FEC_uncorrected_cw_counter	153
134.6.15	FEC_lane_mapping<x>	154
134.6.16	FEC_symbol_error_counter_i	154
134.6.17	align_status	154
134.6.18	BIP_error_counter_i	154
134.6.19	lane_mapping<x>	154
134.6.20	block_lock<x>	154
134.6.21	am_lock<x>	154
134.7	Protocol implementation conformance statement (PICS) proforma for Clause 134, Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs	155
134.7.1	Introduction	155
134.7.2	Identification	155
134.7.2.1	Implementation identification	155
134.7.2.2	Protocol summary	155
134.7.3	Major capabilities/options	156
134.7.4	PICS proforma tables for Reed-Solomon Forward Error Correction (RS-FEC) sublayer for 50GBASE-R PHYs	156
134.7.4.1	Transmit function	156
134.7.4.2	Receive function	157
134.7.4.3	State diagrams	158
134.7.4.4	Delay Constraints	158
135.	Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P	159
135.1	Overview	159
135.1.1	Scope	159
135.1.2	Position of the PMA in the 50GBASE-R and 100GBASE-P sublayers	159
135.1.3	Summary of functions	159
135.1.4	PMA sublayer positioning	160
135.2	PMA interfaces	162
135.3	PMA service interface	163
135.4	Service interface below PMA	164
135.5	Functions within the PMA	165
135.5.1	Per input-lane clock and data recovery	166
135.5.2	Bit-level multiplexing	167
135.5.3	Skew and Skew Variation	167
135.5.3.1	Skew generation toward SP0	168
135.5.3.2	Skew tolerance at SP0	168
135.5.3.3	Skew generation toward SP1	168
135.5.3.4	Skew tolerance at SP1	169
135.5.3.5	Skew generation toward SP2	169
135.5.3.6	Skew tolerance at SP5	169
135.5.3.7	Skew generation at SP6	169
135.5.3.8	Skew tolerance at SP6	169
135.5.3.9	Skew generation at SP7	169
135.5.3.10	Skew tolerance at SP7	169
135.5.4	Delay constraints	170
135.5.5	Clocking architecture	170
135.5.6	Signal drivers	170
135.5.7	PAM4 encoding	171
135.5.7.1	Gray mapping for PAM4 encoded lanes	171

135.5.7.2 Precoding for PAM4 encoded lanes	171
135.5.8 PMA local loopback mode (optional).....	172
135.5.9 PMA remote loopback mode (optional)	173
135.5.10 PMA test patterns (optional).....	173
135.5.10.1 Test patterns for NRZ encoded signals.....	173
135.5.10.1.1 PRBS31 test pattern.....	173
135.5.10.1.2 PRBS9 test pattern.....	173
135.5.10.1.3 Square-wave test pattern.....	173
135.5.10.2 Test patterns for PAM4 encoded signals	174
135.5.10.2.1 PRBS13Q test pattern.....	174
135.5.10.2.2 PRBS31Q test pattern.....	174
135.5.10.2.3 SSPRQ test pattern.....	174
135.5.10.2.4 Square wave (quaternary) test pattern	174
135.6 PMA MDIO function mapping.....	174
135.7 Protocol implementation conformance statement (PICS) proforma for Clause 135, Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P	178
135.7.1 Introduction.....	178
135.7.2 Identification	178
135.7.2.1 Implementation identification.....	178
135.7.2.2 Protocol summary	178
135.7.3 Major capabilities/options.....	179
135.7.4 PICS proforma tables for Physical Medium Attachment (PMA) sublayer, type 50GBASE-R and 100GBASE-P	180
135.7.4.1 Functions.....	180
135.7.4.2 Timing.....	180
135.7.4.3 Electrical	181
135.7.4.4 Diagnostics.....	182
135.7.7 Encoding	184
136. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	185
136.1 Overview.....	185
136.2 Conventions	187
136.3 PMD service interfaces.....	187
136.4 PCS requirements for Auto-Negotiation (AN) service interface.....	189
136.5 Delay constraints.....	189
136.6 Skew constraints	190
136.6.1 Skew Constraints for 50GBASE-CR.....	190
136.6.2 Skew Constraints for 100GBASE-CR2 and 200GBASE-CR4	190
136.7 PMD MDIO function mapping.....	190
136.8 PMD functional specifications.....	194
136.8.1 Link block diagram	194
136.8.2 PMD transmit function	195
136.8.3 PMD receive function.....	196
136.8.4 PMD global signal detect function	196
136.8.5 PMD lane-by-lane signal detect function	196
136.8.6 PMD global transmit disable function (optional)	196
136.8.7 PMD lane-by-lane transmit disable function (optional)	197
136.8.8 PMD fault function	197
136.8.9 PMD transmit fault function (optional)	197
136.8.10 PMD receive fault function (optional).....	197
136.8.11 PMD control function	197
136.8.11.1 Training frame structure	197

136.8.11.1.1	Frame marker	198
136.8.11.1.2	Control and status fields	198
136.8.11.1.3	Training pattern	199
136.8.11.1.4	Zero pad	200
136.8.11.2	Control field structure	200
136.8.11.2.1	Initial condition request	201
136.8.11.2.2	Modulation and precoding request	201
136.8.11.2.3	Coefficient select	201
136.8.11.2.4	Coefficient request	201
136.8.11.3	Status field structure	202
136.8.11.3.1	Receiver ready	202
136.8.11.3.2	Modulation and precoding status	202
136.8.11.3.3	Receiver frame lock	202
136.8.11.3.4	Initial condition status	203
136.8.11.3.5	Parity bit	203
136.8.11.3.6	Coefficient select echo	203
136.8.11.3.7	Coefficient status	203
136.8.11.4	Equalization control	203
136.8.11.4.1	Initial condition setting request process	203
136.8.11.4.2	Initial condition setting response process	203
136.8.11.4.3	Coefficient update request process	204
136.8.11.4.4	Coefficient update response process	204
136.8.11.5	Modulation and precoding setting	205
136.8.11.6	Handshake timing	206
136.8.11.7	Variables, functions, timers, counters, and state diagrams	206
136.8.11.7.1	Variables	206
136.8.11.7.2	Functions	208
136.8.11.7.3	Timers	209
136.8.11.7.4	Counters	209
136.8.11.7.5	State diagrams	209
136.9	PMD electrical characteristics	213
136.9.1	AC-coupling	213
136.9.2	Signal paths	213
136.9.3	Transmitter characteristics	213
136.9.3.1	Transmitter output waveform	214
136.9.3.1.1	Linear fit to the measured waveform	214
136.9.3.1.2	Steady-state voltage and linear fit pulse peak	216
136.9.3.1.3	Coefficient initialization	216
136.9.3.1.4	Coefficient step size	216
136.9.3.1.5	Coefficient range	217
136.9.3.2	Insertion loss, TP0 to TP2 or TP3 to TP5	217
136.9.3.3	J3u jitter	217
136.9.3.4	Transmitter effective return loss (ERL)	217
136.9.4	Receiver characteristics	218
136.9.4.1	Receiver input amplitude tolerance	218
136.9.4.2	Receiver interference tolerance	219
136.9.4.2.1	Test setup	219
136.9.4.2.2	Test channel	219
136.9.4.2.3	Test channel calibration	219
136.9.4.2.4	Pattern generator and noise injection	220
136.9.4.2.5	Test procedure	221
136.9.4.3	Receiver jitter tolerance	221
136.9.4.3.1	Test setup	221
136.9.4.3.2	Test procedure	221

136.9.4.4 Signaling rate range	222
136.9.4.5 Receiver ERL	222
136.10 Channel characteristics	222
136.11 Cable assembly characteristics	222
136.11.1 Characteristic impedance and reference impedance	223
136.11.2 Cable assembly insertion loss	223
136.11.3 Cable assembly ERL	223
136.11.4 Differential to common-mode return loss	224
136.11.5 Differential to common-mode conversion loss	224
136.11.6 Common-mode to common-mode return loss	224
136.11.7 Cable assembly Channel Operating Margin	224
136.11.7.1 Channel signal and crosstalk path calculations	226
136.11.7.1.1 Channel signal path	226
136.11.7.1.2 Channel crosstalk paths	226
136.11.7.2 Signal and crosstalk paths used in calculation of COM	227
136.12 MDI specifications	228
136.13 Environmental specifications	228
136.14 Protocol implementation conformance statement (PICS) proforma for Clause 136, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	229
136.14.1 Introduction	229
136.14.2 Identification	229
136.14.2.1 Implementation identification	229
136.14.2.2 Protocol summary	229
136.14.3 Major capabilities/options	230
136.14.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	231
136.14.4.1 PMD functional specifications	231
136.14.4.2 PMD control function	232
136.14.4.3 Transmitter specifications	232
136.14.4.4 Receiver specifications	233
136.14.4.5 Cable assembly specifications	233
136.14.4.6 Environmental specifications	234
137. Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	235
137.1 Overview	235
137.2 Conventions	238
137.3 PMD service interfaces	238
137.4 PCS requirements for Auto-Negotiation (AN) service interface	238
137.5 Delay constraints	238
137.6 Skew constraints	239
137.6.1 Skew Constraints for 50GBASE-KR	239
137.6.2 Skew Constraints for 100GBASE-KR2 and 200GBASE-KR4	239
137.7 PMD MDIO function mapping	239
137.8 PMD functional specifications	240
137.8.1 Link block diagram	240
137.8.2 PMD transmit function	240
137.8.3 PMD receive function	240
137.8.4 PMD global signal detect function	240
137.8.5 PMD lane-by-lane signal detect function	240
137.8.6 PMD global transmit disable function (optional)	240
137.8.7 PMD lane-by-lane transmit disable function (optional)	240

137.8.8 PMD fault function	241
137.8.9 PMD transmit fault function (optional)	241
137.8.10 PMD receive fault function (optional)	241
137.8.11 PMD control function	241
137.9 Electrical characteristics	241
137.9.1 MDI	241
137.9.2 Transmitter characteristics	241
137.9.2.1 Transmitter ERL	241
137.9.3 Receiver characteristics	242
137.9.3.1 Receiver ERL	242
137.10 Channel characteristics	242
137.10.1 Channel insertion loss	244
137.10.2 Channel ERL	245
137.11 Environmental specifications	245
137.12 Protocol implementation conformance statement (PICS) proforma for Clause 137, Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	246
137.12.1 Introduction	246
137.12.2 Identification	246
137.12.2.1 Implementation identification	246
137.12.2.2 Protocol summary	246
137.12.3 Major capabilities/options	247
137.12.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and baseband medium, type 50GBASE-KR, 100GBASE-KR2, and 200GBASE-KR4	248
137.12.4.1 Functional specifications	248
137.12.4.2 PMD control function	249
137.12.4.3 Transmitter characteristics	249
137.12.4.4 Receiver characteristics	250
137.12.4.5 Channel characteristics	250
137.12.4.6 Environmental specifications	250
138. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4	251
138.1 Overview	251
138.1.1 Bit error ratio	253
138.2 Physical Medium Dependent (PMD) service interface	254
138.3 Delay and Skew	255
138.3.1 Delay constraints	255
138.3.2 Skew constraints	255
138.3.2.1 Skew Constraints for 50GBASE-SR	255
138.3.2.2 Skew Constraints for 100GBASE-SR2 and 200GBASE-SR4	256
138.4 PMD MDIO function mapping	256
138.5 PMD functional specifications	257
138.5.1 PMD block diagram	257
138.5.2 PMD transmit function	257
138.5.3 PMD receive function	258
138.5.4 PMD global signal detect function	258
138.5.5 PMD lane-by-lane signal detect function	259
138.5.6 PMD reset function	259
138.5.7 PMD global transmit disable function (optional)	259
138.5.8 PMD lane-by-lane transmit disable function (optional)	259
138.5.9 PMD fault function (optional)	260
138.5.10 PMD transmit fault function (optional)	260

138.5.11 PMD receive fault function (optional).....	260
138.6 Lane assignments.....	260
138.7 PMD to MDI optical specifications for 50GBASE-SR, 100GBASE-SR2, and 200GBASE-SR4.....	260
138.7.1 Transmitter optical specifications.....	261
138.7.2 Receiver optical specifications.....	261
138.7.3 Illustrative link power budget.....	262
138.8 Definition of optical parameters and measurement methods.....	263
138.8.1 Test patterns for optical parameters.....	263
138.8.1.1 Multi-lane testing considerations.....	264
138.8.2 Center wavelength and spectral width.....	264
138.8.3 Average optical power.....	264
138.8.4 Outer Optical Modulation Amplitude (OMA _{outer}).....	264
138.8.5 Transmitter and dispersion eye closure for PAM4 (TDECQ).....	264
138.8.5.1 TDECQ reference equalizer.....	265
138.8.6 Extinction ratio.....	265
138.8.7 Transmitter transition time.....	265
138.8.8 Relative intensity noise (RIN _{12OMA}).....	265
138.8.9 Receiver sensitivity.....	266
138.8.10 Stressed receiver sensitivity.....	266
138.8.10.1 Sinusoidal jitter for receiver conformance test.....	267
138.9 Safety, installation, environment, and labeling.....	267
138.9.1 General safety.....	267
138.9.2 Laser safety.....	267
138.9.3 Installation.....	268
138.9.4 Environment.....	268
138.9.5 Electromagnetic emission.....	268
138.9.6 Temperature, humidity, and handling.....	268
138.9.7 PMD labeling requirements.....	268
138.10 Fiber optic cabling model.....	268
138.10.1 Fiber optic cabling model.....	269
138.10.2 Characteristics of the fiber optic cabling (channel).....	270
138.10.2.1 Optical fiber cable.....	270
138.10.2.2 Optical fiber connection.....	270
138.10.2.2.1 Connection insertion loss.....	270
138.10.2.2.2 Maximum discrete reflectance.....	270
138.10.3 Medium Dependent Interface (MDI).....	271
138.10.3.1 Optical lane assignments for 100GBASE-SR2 and 200GBASE-SR4.....	271
138.10.3.2 MDI requirements for 50GBASE-SR.....	271
138.10.3.3 MDI requirements for 100GBASE-SR2 and 200GBASE-SR4.....	272
138.11 Protocol implementation conformance statement (PICS) proforma for Clause 138, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4.....	273
138.11.1 Introduction.....	273
138.11.2 Identification.....	273
138.11.2.1 Implementation identification.....	273
138.11.2.2 Protocol summary.....	273
138.11.3 Major capabilities/options.....	274
138.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-SR, 100GBASE-SR2, 200GBASE-SR4.....	274
138.11.4.1 PMD functional specifications.....	274
138.11.4.2 Management functions.....	275
138.11.4.3 PMD to MDI optical specifications.....	276
138.11.4.4 Optical measurement methods.....	276

138.11.4.5 Environmental specifications.....	277
138.11.4.6 Characteristics of the fiber optic cabling and MDI.....	277
139. Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR.....	278
139.1 Overview.....	278
139.1.1 Bit error ratio	279
139.2 Physical Medium Dependent (PMD) service interface	279
139.3 Delay and Skew	280
139.3.1 Delay constraints.....	280
139.3.2 Skew constraints	280
139.4 PMD MDIO function mapping.....	281
139.5 PMD functional specifications.....	281
139.5.1 PMD block diagram.....	281
139.5.2 PMD transmit function	282
139.5.3 PMD receive function.....	282
139.5.4 PMD global signal detect function	282
139.5.5 PMD reset function	283
139.5.6 PMD global transmit disable function (optional)	283
139.5.7 PMD fault function (optional)	283
139.5.8 PMD transmit fault function (optional)	283
139.5.9 PMD receive fault function (optional).....	283
139.6 PMD to MDI optical specifications for 50GBASE-FR and 50GBASE-LR.....	284
139.6.1 50GBASE-FR and 50GBASE-LR transmitter optical specifications.....	284
139.6.2 50GBASE-FR and 50GBASE-LR receive optical specifications	285
139.6.3 50GBASE-FR and 50GBASE-LR illustrative link power budgets.....	286
139.7 Definition of optical parameters and measurement methods.....	286
139.7.1 Test patterns for optical parameters.....	286
139.7.2 Wavelength and side-mode suppression ratio (SMSR)	287
139.7.3 Average optical power	287
139.7.4 Outer Optical Modulation Amplitude (OMA _{outer}).....	287
139.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)	288
139.7.5.1 TDECQ conformance test setup	288
139.7.5.2 Channel requirements	289
139.7.5.3 TDECQ measurement method.....	289
139.7.5.4 TDECQ reference equalizer.....	290
139.7.6 Extinction ratio	290
139.7.7 Transmitter transition time.....	290
139.7.8 Relative intensity noise (RIN _{17,1} OMA and RIN _{15,6} OMA).....	290
139.7.9 Receiver sensitivity.....	291
139.7.10 Stressed receiver sensitivity.....	291
139.7.10.1 Stressed receiver conformance test block diagram.....	292
139.7.10.2 Stressed receiver conformance test signal characteristics and calibration.....	293
139.7.10.3 Stressed receiver conformance test signal verification.....	293
139.8 Safety, installation, environment, and labeling.....	293
139.8.1 General safety	293
139.8.2 Laser safety	293
139.8.3 Installation	294
139.8.4 Environment.....	294
139.8.5 Electromagnetic emission	294
139.8.6 Temperature, humidity, and handling.....	294
139.8.7 PMD labeling requirements	294
139.9 Fiber optic cabling model	295

139.10 Characteristics of the fiber optic cabling (channel)	295
139.10.1 Optical fiber cable	295
139.10.2 Optical fiber connection	296
139.10.2.1 Connection insertion loss	296
139.10.2.2 Maximum discrete reflectance	296
139.10.3 Medium Dependent Interface (MDI) requirements	297
139.11 Protocol implementation conformance statement (PICS) proforma for Clause 139, Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR	298
139.11.1 Introduction	298
139.11.2 Identification	298
139.11.2.1 Implementation identification	298
139.11.2.2 Protocol summary	298
139.11.3 Major capabilities/options	299
139.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 50GBASE-FR and 50GBASE-LR	299
139.11.4.1 PMD functional specifications	299
139.11.4.2 Management functions	300
139.11.4.3 PMD to MDI optical specifications for 50GBASE-FR	300
139.11.4.4 PMD to MDI optical specifications for 50GBASE-LR	301
139.11.4.5 Optical measurement methods	301
139.11.4.6 Environmental specifications	301
139.11.4.7 Characteristics of the fiber optic cabling and MD	302
140. Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR	303
140.1 Overview	303
140.1.1 Bit error ratio	304
140.2 Physical Medium Dependent (PMD) service interface	304
140.3 Delay and Skew	305
140.3.1 Delay constraints	305
140.3.2 Skew constraints	305
140.4 PMD MDIO function mapping	306
140.5 PMD functional specifications	306
140.5.1 PMD block diagram	306
140.5.2 PMD transmit function	307
140.5.3 PMD receive function	307
140.5.4 PMD global signal detect function	307
140.5.5 PMD reset function	308
140.5.6 PMD global transmit disable function (optional)	308
140.5.7 PMD fault function (optional)	308
140.5.8 PMD transmit fault function (optional)	308
140.5.9 PMD receive fault function (optional)	308
140.6 PMD to MDI optical specifications for 100GBASE-DR	309
140.6.1 100GBASE-DR transmitter optical specifications	309
140.6.2 100GBASE-DR receive optical specifications	310
140.6.3 100GBASE-DR illustrative link power budget	311
140.7 Definition of optical parameters and measurement methods	311
140.7.1 Test patterns for optical parameters	311
140.7.2 Wavelength and side-mode suppression ratio (SMSR)	312
140.7.3 Average optical power	312
140.7.4 Outer Optical Modulation Amplitude (OMA _{outer})	313
140.7.5 Transmitter and dispersion eye closure for PAM4 (TDECQ)	313
140.7.5.1 TDECQ reference equalizer	313

140.7.6 Extinction ratio	314
140.7.7 Transmitter transition time.....	314
140.7.8 Relative intensity noise (RIN15.5OMA).....	314
140.7.9 Receiver sensitivity.....	314
140.7.10 Stressed receiver sensitivity.....	315
140.8 Safety, installation, environment, and labeling.....	315
140.8.1 General safety	315
140.8.2 Laser safety	316
140.8.3 Installation	316
140.8.4 Environment.....	316
140.8.5 Electromagnetic emission	316
140.8.6 Temperature, humidity, and handling.....	316
140.8.7 PMD labeling requirements	316
140.9 Fiber optic cabling model	317
140.10 Characteristics of the fiber optic cabling (channel)	318
140.10.1 Optical fiber cable.....	318
140.10.2 Optical fiber connection.....	319
140.10.2.1 Connection insertion loss.....	319
140.10.2.2 Maximum discrete reflectance.....	319
140.10.3 Medium Dependent Interface (MDI).....	319
140.11 Protocol implementation conformance statement (PICS) proforma for Clause 140, Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR	320
140.11.1 Introduction.....	320
140.11.2 Identification.....	320
140.11.2.1 Implementation identification.....	320
140.11.2.2 Protocol summary	320
140.11.3 Major capabilities/options.....	321
140.11.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium, type 100GBASE-DR	321
140.11.4.1 PMD functional specifications.....	321
140.11.4.2 Management functions.....	322
140.11.4.3 PMD to MDI optical specifications for 100GBASE-DR	322
140.11.4.4 Optical measurement methods.....	323
140.11.4.5 Environmental specifications.....	323
140.11.4.6 Characteristics of the fiber optic cabling and MD.....	323
Annex 4A (normative) Simplified full duplex media access control	324
4A.4 Specific implementations.....	324
4A.4.2 MAC parameters	324
Annex 31B (normative) MAC Control PAUSE operation	325
31B.3 Detailed specification of PAUSE operation.....	325
31B.3.7 Timing considerations for PAUSE operation	325
31B.4 Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation	325
31B.4.3 Major capabilities/options	325
31B.4.6 PAUSE command MAC timing considerations	325
Annex 93A (normative) Specification methods for electrical channels	326
93A.1 Channel Operating Margin	326
93A.1.4 Filters	327

93A.1.4.2 Transmitter equalizer	327
93A.1.6 Determination of variable equalizer parameters	327
93A.5 Effective Return Loss	328
93A.5.1 Pulse time-domain reflection signal	328
93A.5.2 Effective reflection waveform	329
93A.5.3 Sampled effective reflection	330
93A.5.4 x-quantile of the reflection distribution	330
93A.5.5 ERL	330
Annex 135A (informative) 50 Gb/s and 100 Gb/s PMA sublayer partitioning examples	331
135A.1 Partitioning examples of 50GBASE-R PHYs	331
135A.2 Partitioning examples of 100GBASE-P PHYs	336
Annex 135B (normative) Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)	337
135B.1 Overview	337
135B.2 LAUI-2 C2C compliance point definition	338
135B.3 LAUI-2 C2C electrical characteristics	338
135B.3.1 LAUI-2 C2C transmitter characteristics	338
135B.3.2 LAUI-2 C2C receiver characteristics	339
135B.4 LAUI-2 C2C channel characteristics	339
135B.5 Protocol implementation conformance statement (PICS) proforma for Annex 135B, Chip-to-Chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)	340
135B.5.1 Introduction	340
135B.5.2 Identification	340
135B.5.2.1 Implementation identification	340
135B.5.2.2 Protocol summary	340
135B.5.3 Major capabilities/options	341
135B.5.4 PICS proforma tables for chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2C)	341
135B.5.4.1 Transmitter	341
135B.5.4.2 Receiver	342
135B.5.4.3 Channel	342
Annex 135C (normative) Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)	343
135C.1 Overview	343
135C.1.1 Bit error ratio	344
135C.2 LAUI-2 C2M compliance point definitions	344
135C.3 LAUI-2 C2M electrical characteristics	344
135C.3.1 LAUI-2 C2M host output characteristics	344
135C.3.2 LAUI-2 C2M module output characteristics	344
135C.3.3 LAUI-2 C2M host input characteristics	345
135C.3.4 LAUI-2 C2M module input characteristics	345
135C.4 LAUI-2 C2M measurement methodology	345
135C.5 Protocol implementation conformance statement (PICS) proforma for Annex 135C, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)	346
135C.5.1 Introduction	346
135C.5.2 Identification	346
135C.5.2.1 Implementation identification	346
135C.5.2.2 Protocol summary	346
135C.5.3 Major capabilities/options	347

135C.5.4 PICS proforma tables for chip-to-module 50 Gb/s two-lane Attachment Unit Interface (LAUI-2 C2M)	347
135C.5.4.1 Host output	347
135C.5.4.2 Module output	348
135C.5.4.3 Host input	348
135C.5.4.4 Module input	348
Annex 135D (normative) Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)	349
135D.1 Overview	349
135D.2 50GAUI-2 C2C and 100GAUI-4 C2C compliance point definition	351
135D.3 50GAUI-2 C2C and 100GAUI-4 C2C electrical characteristics	351
135D.3.1 50GAUI-2 C2C and 100GAUI-4 C2C transmitter characteristics	351
135D.3.2 50GAUI-2 C2C and 100GAUI-4 C2C receiver characteristics	351
135D.4 50GAUI-2 C2C and 100GAUI-4 C2C channel characteristics	351
135D.5 Protocol implementation conformance statement (PICS) proforma for Annex 135D, Chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)	352
135D.5.1 Introduction	352
135D.5.2 Identification	352
135D.5.2.1 Implementation identification	352
135D.5.2.2 Protocol summary	352
135D.5.3 Major capabilities/options	353
135D.5.4 PICS proforma tables for chip-to-chip 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2C) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2C)	353
135D.5.4.1 Transmitter	353
135D.5.4.2 Receiver	354
135D.5.4.3 Channel	354
Annex 135E (normative) Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)	355
135E.1 Overview	355
135E.1.1 Bit error ratio	357
135E.2 50GAUI-2 C2M and 100GAUI-4 C2M compliance point definitions	357
135E.3 50GAUI-2 C2M and 100GAUI-4 C2M electrical characteristics	357
135E.3.1 50GAUI-2 C2M and 100GAUI-4 C2M host output characteristics	357
135E.3.2 50GAUI-2 C2M and 100GAUI-4 C2M module output characteristics	357
135E.3.3 50GAUI-2 C2M and 100GAUI-4 C2M host input characteristics	357
135E.3.4 50GAUI-2 C2M and 100GAUI-4 C2M module input characteristics	357
135E.4 50GAUI-2 C2M and 100GAUI-4 C2M measurement methodology	357
135E.5 Protocol implementation conformance statement (PICS) proforma for Annex 135E, Chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)	358
135E.5.1 Introduction	358
135E.5.2 Identification	358
135E.5.2.1 Implementation identification	358
135E.5.2.2 Protocol summary	358
135E.5.3 Major capabilities/options	359
135E.5.4 PICS proforma tables for chip-to-module 50 Gb/s two-lane Attachment Unit Interface (50GAUI-2 C2M) and 100 Gb/s four-lane Attachment Unit Interface (100GAUI-4 C2M)	359

135E.5.4.1 Host output	359
135E.5.4.2 Module output	360
135E.5.4.3 Host input	361
135E.5.4.4 Module input	361
 Annex 135F (normative) Chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)	 362
135F.1 Overview	362
135F.2 50GAUI-1 C2C and 100GAUI-2 C2C compliance point definition	364
135F.3 50GAUI-1 C2C and 100GAUI-2 C2C electrical characteristics	364
135F.3.1 50GAUI-1 C2C and 100GAUI-2 C2C transmitter characteristics	364
135F.3.2 50GAUI-1 C2C and 100GAUI-2 C2C receiver characteristics	364
135F.3.2.1 Transmitter precoder request (optional)	364
135F.4 50GAUI-1 C2C and 100GAUI-2 C2C channel characteristics	365
135F.5 Example usage of the optional transmitter precoder request	365
135F.5.1 Overview	365
135F.5.2 Configuring precoder setting in the transmit direction	365
135F.5.3 Configuring precoder setting in the receive direction	366
135F.6 Protocol implementation conformance statement (PICS) proforma for Annex 135F, Chip- to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)	 367
135F.6.1 Introduction	367
135F.6.2 Identification	367
135F.6.2.1 Implementation identification	367
135F.6.2.2 Protocol summary	367
135F.6.3 Major capabilities/options	368
135F.6.4 PICS proforma tables for chip-to-chip 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2C) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2C)	 368
135F.6.4.1 Transmitter	368
135F.6.4.2 Receiver	369
135F.6.4.3 Channel	369
 Annex 135G (normative) Chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)	 370
135G.1 Overview	370
135G.1.1 Bit error ratio	372
135G.2 50GAUI-1 C2M and 100GAUI-2 C2M compliance point definitions	372
135G.3 50GAUI-1 C2M and 100GAUI-2 C2M electrical characteristics	372
135G.3.1 50GAUI-1 C2M and 100GAUI-2 C2M host output characteristics	372
135G.3.2 50GAUI-1 C2M and 100GAUI-2 C2M module output characteristics	372
135G.3.3 50GAUI-1 C2M and 100GAUI-2 C2M host input characteristics	372
135G.3.4 50GAUI-1 C2M and 100GAUI-2 C2M module input characteristics	372
135G.4 50GAUI-1 C2M and 100GAUI-2 C2M measurement methodology	372
135G.5 Protocol implementation conformance statement (PICS) proforma for Annex 135G, Chip- to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)	 373
135G.5.1 Introduction	373
135G.5.2 Identification	373
135G.5.2.1 Implementation identification	373
135G.5.2.2 Protocol summary	373
135G.5.3 Major capabilities/options	374

135G.5.4 PICS proforma tables for chip-to-module 50 Gb/s one-lane Attachment Unit Interface (50GAUI-1 C2M) and 100 Gb/s two-lane Attachment Unit Interface (100GAUI-2 C2M)	374
135G.5.4.1 Host output.....	374
135G.5.4.2 Module output.....	375
135G.5.4.3 Host input.....	376
135G.5.4.4 Module input.....	376
Annex 136A (informative) TP0 and TP5 test point parameters and channel characteristics for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	377
136A.1 Overview.....	377
136A.2 Transmitter characteristics at TP0	377
136A.3 Receiver characteristics at TP5	377
136A.4 Transmitter and receiver differential printed circuit board trace loss.....	377
136A.5 Channel insertion loss	377
136A.6 Channel effective return loss	379
136A.7 Channel Operating Margin (COM).....	379
Annex 136B (normative) Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M.....	380
136B.1 Test fixtures.....	380
136B.1.1 Mated test fixtures.....	380
136B.1.1.1 Mated test fixtures differential insertion loss.....	380
136B.1.1.2 Mated test fixtures differential return loss	381
136B.1.1.3 Mated test fixtures common-mode conversion insertion loss.....	381
136B.1.1.4 Mated test fixtures common-mode return loss.....	381
136B.1.1.5 Mated test fixtures common-mode to differential mode return loss	381
136B.1.1.6 Mated test fixtures integrated crosstalk noise	381
136B.2 Protocol implementation conformance statement (PICS) proforma for Annex 136B, Test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M	383
136B.2.1 Introduction	383
136B.2.2 Identification	383
136B.2.2.1 Implementation identification	383
136B.2.2.2 Protocol summary	383
136B.2.3 Major capabilities/options	384
136B.2.4 PICS proforma tables for test fixtures for 50GBASE-CR, 100GBASE-CR2, 200GBASE-CR4, 50GAUI-1 C2M, and 100GAUI-2 C2M.....	384
Annex 136C (normative) MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	385
136C.1 Overview	385
136C.2 MDI connector types.....	388
136C.2.1 SFP28	388
136C.2.2 QSFP28	389
136C.2.3 MicroQSFP	389
136C.2.4 QSFP-DD	390
136C.2.5 OSFP	391
136C.3 Protocol implementation conformance statement (PICS) proforma for Annex 136C, MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4.....	392
136C.3.1 Introduction	392
136C.3.2 Identification	392

136C.3.2.1 Implementation identification	392
136C.3.2.2 Protocol summary	392
136C.3.3 Major capabilities/options	393
136C.3.4 PICS proforma tables for MDIs for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	393
136C.3.4.1 Contact Mapping	393
Annex 136D (informative) Host and cable assembly form factors for 50GBASE-CR, 100GBASE-CR2, and 200GBASE-CR4	394
136D.1 Overview	394
136D.2 Host form factors	394
136D.2.1 SFP28 host form factor	394
136D.2.2 QSFP28 host form factor	394
136D.2.3 microQSFP host form factor	395
136D.2.4 QSFP-DD host form factor	395
136D.2.5 OSFP host form factor	395
136D.3 Cable assembly form factors	396
136D.3.1 One-plug to one-plug cable assembly form factor	396
136D.3.2 One-plug to two-plug cable assembly form factor	397
136D.3.3 One-plug to four-plug cable assembly form factor	398
136D.3.4 One-plug to eight-plug cable assembly form factor	399

IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018 and IEEE Std 802.3bt™-2018.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.¹

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following new compatibility interfaces into 1.1.3.2 after m) “40 Gb/s Parallel Physical Interface (XLPPi)”:

- m1) *50 Gb/s Media Independent Interface (50GMII)*. The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.
- m2) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n)*. The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

Change the compatibility interface o) “100 Gb/s Attachment Unit Interface (CAUI-n)” in 1.1.3.2 as follows:

- o) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n)*. The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three ~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, ~~and~~ a four-lane version (CAUI-4/100GAUI-4) in Annex 83D, and Annex 83E, Annex 135D, and Annex 135E, ~~and~~ a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

1.3 Normative references

Change the following reference in 1.3 as shown:

IEC 61753-022-2:2012, Fibre optic interconnecting devices and passive components—Performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for category C—Controlled environment, performance Class M.

1.4 Definitions

Insert the following new definition after 1.4.25 “100GBASE-CR10”:

1.4.25a 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

Insert the following new definition after 1.4.26 “100GBASE-CR4”:

1.4.26a 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

Insert the following new definition after 1.4.28 “100GBASE-KP4”:

1.4.28a 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.34 “100GBASE-SR10”:

1.4.34a 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Change 1.4.36 as follows:

1.4.36 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. ThreeTwo widths of CAUI-n are defined: a ten-lane version (CAUI-10), and at two four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, [Annex 83A](#) and [Annex 83B](#) for CAUI-10, ~~or Annex 83D~~ and [Annex 83E](#) for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

Insert the following new definition after 1.4.82c “2.5GSEI” as inserted by IEEE Std 802.3cb-2018:

1.4.82d 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

Insert the following new definition after 1.4.84 “200GBASE-FR4”:

1.4.84a 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.86 “200GBASE-R”:

1.4.86a 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Insert the following new definitions before 1.4.128a “5GBASE-KR” as inserted by IEEE Std 802.3cb-2018:

1.4.128aa 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

1.4.128ab 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ac 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.128ad 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ae 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.128af 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 138.)

1.4.128ag 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.128ah 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132.)

Insert the following new definition after 1.4.255 “fast wake”:

1.4.255a FEC lane (FECL): In 50GBASE-R and 100GBASE-R, the FEC distributes encoded data to multiple logical lanes; these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

Change 1.4.386 as follows:

1.4.386 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes; these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83, and Clause 120, and Clause 135.)

1.5 Abbreviations

Insert the following new abbreviations into 1.5 in alphanumeric order:

100GAUI	100 Gb/s Attachment Unit Interface
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
ERL	effective return loss
FECL	FEC Lane
LAUI	50 Gb/s Attachment Unit Interface

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, <u>50 Gb/s</u> , 100 Gb/s, 200 Gb/s, and 400 Gb/s	10 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap ^a	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

^aReferences to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 in 4.4.2 as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry into “APPROPRIATE SYNTAX” in 30.3.2.1.2 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:
 50GBASE-R Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry into “APPROPRIATE SYNTAX” in 30.3.2.1.3 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:
 50GBASE-R Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph of “BEHAVIOUR DEFINED AS” in 30.3.2.1.5 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:
 For operation at 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the media independent interface (see Table 46-4 and Table 81-4).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

APPROPRIATE SYNTAX:

Insert the following new entries into “APPROPRIATE SYNTAX” in 30.5.1.1.2 after the entry for 40GBASE-T:

50GBASE-R Multi-lane PCS as specified in Clause 133 with PMA as specified in
 Clause 135 over undefined PMD

50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139

Insert the following new entries into “APPROPRIATE SYNTAX” in 30.5.1.1.2 after the entry for 100GBASE-ER4:

100GBASE-CR2	100GBASE-R PCS/PMA over 2 lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-SR2	100GBASE-R PCS/PMA over 2 lane multimode fiber PMD as specified in Clause 138
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140

Insert the following new entries into “APPROPRIATE SYNTAX” in 30.5.1.1.2 after the entry for 200GBASE-LR4:

200GBASE-CR4	200GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-KR4	200GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-SR4	200GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 138

Change the last paragraph of “BEHAVIOUR DEFINED AS” in 30.5.1.1.2 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 2.5GBASE-X, 5GBASE-R, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of “BEHAVIOUR DEFINED AS” in 30.5.1.1.4 as follows:

BEHAVIOUR DEFINED AS:

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”.

30.5.1.1.11 aBIPErrorCount

Change the text of “APPROPRIATE SYNTAX” and the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.11 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.12 aLaneMapping

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.12 as follows:

BEHAVIOUR DEFINED AS:

For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.17 aFECCorrectedBlocks

Change the text of “APPROPRIATE SYNTAX” in 30.5.1.1.17 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.17 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change the text of “APPROPRIATE SYNTAX” in 30.5.1.1.18 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.18 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.5.1.1.26 aRSFECBIPErrorCount

Change the text of “APPROPRIATE SYNTAX” and the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.26 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R_x and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.27 aRSFECLaneMapping

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.27 as follows:

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R_x and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.29 aRSFECBypassIndicationAbility

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.29 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability ~~(see 91.5.3.3).~~

30.5.1.1.31 aRSFECBypassIndicationEnable

Change the first sentence of “BEHAVIOUR DEFINED AS” in 30.5.1.1.31 as follows:

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function ~~(see 91.5.3.3).~~

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

APPROPRIATE SYNTAX:

Insert the following new entry into “APPROPRIATE SYNTAX” in 30.6.1.1.5 after the entry for 40GBASE-T:

50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137
------	--

Insert the following new entries into “APPROPRIATE SYNTAX” in 30.6.1.1.5 after the entry for 100GBASE-KP4:

100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.20	Reserved 50G PMA/PMD extended ability	45.2.1.17a
...		
1.25, 1.26	Reserved PMA/PMD extended ability 2	45.2.1.21a
1.26	Reserved	
...		
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.129, 45.2.1.130
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.131, 45.2.1.132
1.532 through 1.699 1.532 through 1.599	Reserved	
1.600	PMA precoder control Tx output	45.2.1.132a
1.601	PMA precoder control Rx input	45.2.1.132b
1.602	PMA precoder control Rx output	45.2.1.132c
1.603	PMA precoder control Tx input	45.2.1.132d
1.604	PMA precoder request flag	45.2.1.132e
1.605	PMA precoder request Rx input status	45.2.1.132f
1.606	PMA precoder request Tx input status	45.2.1.132g
1.607 through 1.649	Reserved	
1.650, 1.651	RS-FEC degraded SER activate threshold	45.2.1.132h
1.652, 1.653	RS-FEC degraded SER deactivate threshold	45.2.1.132i
1.654, 1.655	RS-FEC degraded SER interval	45.2.1.132j
1.656 through 1.699	Reserved	
...		

Table 45–3—PMA/PMD registers (continued)

Register address	Register name	Subclause
1.1110 through 1.1199 <u>1.1110 through 1.1119</u>	Reserved	
<u>1.1120 through 1.1123</u>	<u>BASE-R PAM4 PMD training LP control, lane 0 through lane 3</u>	<u>45.2.1.135a</u>
<u>1.1124 through 1.1199</u>	<u>Reserved</u>	
...		
1.1210 through 1.1299 <u>1.1210 through 1.1219</u>	Reserved	
<u>1.1220 through 1.1223</u>	<u>BASE-R PAM4 PMD training LP status, lane 0 through lane 3</u>	<u>45.2.1.136a</u>
<u>1.1224 through 1.1299</u>	<u>Reserved</u>	
...		
1.1310 through 1.1399 <u>1.1310 through 1.1319</u>	Reserved	
<u>1.1320 through 1.1323</u>	<u>BASE-R PAM4 PMD training LD control, lane 0 through lane 3</u>	<u>45.2.1.137a</u>
<u>1.1324 through 1.1399</u>	<u>Reserved</u>	
...		
1.1410 through 1.1449 <u>1.1410 through 1.1419</u>	Reserved	
<u>1.1420 through 1.1423</u>	<u>BASE-R PAM4 PMD training LD status, lane 0 through lane 3</u>	<u>45.2.1.138a</u>
<u>1.1424 through 1.1449</u>	<u>Reserved</u>	
...		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the bits 1.0.5:2 row in Table 45–4 as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = Reserved 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
...			

^aR/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 as follows:

For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.