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**AMENDMENT 9**
2021-12

# Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

## Part 3: Standard for Ethernet

## AMENDMENT 9: Physical layer specifications and management parameters for 25 Gb/s and 50 Gb/s passive optical networks

*Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —*

*Partie 3: Norme pour Ethernet*

*AMENDEMENT 9: Spécifications de couche physique et paramètres de gestion pour réseaux optiques passifs à 25 Gb/s et 50 Gb/s*

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**IEEE Std 802.3ca™-2020**
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018,
IEEE Std 802.3bt™-2018,
IEEE Std 802.3cd™-2018,
IEEE Std 802.3cn™-2019,
IEEE Std 802.3cg™-2019,
IEEE Std 802.3cq™-2020,
IEEE Std 802.3cm™-2020,
and IEEE Std 802.3ch™-2020)

# IEEE Standard for Ethernet

# Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks

Developed by the

**LAN/MAN Standards Committee**
of the
**IEEE Computer Society**

Approved 4 June 2020

**IEEE SA Standards Board**


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**Abstract:** This amendment to IEEE Std 802.3-2018 extends the operation of Ethernet passive optical networks (EPONs) to multiple channels of 25 Gb/s providing both symmetric and asymmetric operation for the following data rates (downstream/upstream): 25/10 Gb/s, 25/25 Gb/s, 50/10 Gb/s, 50/25 Gb/s, and 50/50 Gb/s. This standard specifies the 25 Gb/s EPON Multi-Channel Reconciliation Sublayer (MCRS), Nx25G-EPON Physical Coding Sublayers (PCSs), Physical Media Attachment (PMA) sublayers, and Physical Medium Dependent (PMD) sublayers that support both symmetric and asymmetric data rates while maintaining backward compatibility with already deployed 10 Gb/s EPON equipment. Backward compatibility with deployed 1G-EPON and ITU-T G.984 GPON is maintained with 25GBASE-PQ for the specific case of 1G-EPON and GPON ONUs using reduced-band (40 nm) lasers. The EPON operation is defined for distances of at least 20 km, and for a split ratio of at least 1:32.

**Keywords:** 25 Gb/s Ethernet passive optical networks (25G-EPON), 50 Gb/s Ethernet passive optical networks (50G-EPON), amendment, forward error correction (FEC), IEEE 802.3™, IEEE 802.3ca™, Multi-Channel Reconciliation Sublayer (MCRS), Multipoint MAC Control (MPMC), Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Physical Medium Dependent (PMD), PON, Point-to-Multipoint (P2MP)

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# Introduction

This introduction is not part of IEEE Std 802.3ca-2020, IEEE Standard for Ethernet. Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of IEEE Std 802.3ca-2020 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines


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services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt™-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

IEEE Std 802.3cn™-2019

Amendment 4—This amendment includes changes to IEEE Std 802.3-2018 and adds 50 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications and management parameters for operation over single-mode fiber with reaches of at least 40 km.


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IEEE Std 802.3cg™-2019

Amendment 5—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 146 through Clause 148 and Annex 146A and Annex 146B. This amendment adds 10 Mb/s Physical Layer specifications and management parameters for operation on a single balanced pair of conductors.

IEEE Std 802.3cq™-2020

Amendment 6—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 33 and related portions of the standard.

IEEE Std 802.3cm™-2020

Amendment 7—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 150. This amendment adds Physical Layer (PHY) specifications and management parameters for 400 Gb/s operation on four pairs (400GBASE-SR4.2) and eight pairs (400GBASE-SR8) of multimode fiber, over reaches of at least 100 m.

IEEE Std 802.3ch™-2020

Amendment 8—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 149, Annex 149A, Annex 149B, and Annex 149C. This amendment adds physical layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3ca™-2020

Amendment 9—This amendment to IEEE Std 802.3-2018 extends the operation of Ethernet passive optical networks (EPONs) to multiple channels of 25 Gb/s providing both symmetric and asymmetric operation for the following data rates (downstream/upstream): 25/10 Gb/s, 25/25 Gb/s, 50/10 Gb/s, 50/25 Gb/s, and 50/50 Gb/s. This amendment specifies the 25 Gb/s EPON Multi-Channel Reconciliation Sublayer (MCRS), Nx25G-EPON Physical Coding Sublayers (PCSs), Physical Media Attachment (PMA) sublayers, and Physical Medium Dependent (PMD) sublayers that support both symmetric and asymmetric data rates while maintaining backward compatibility with already deployed 10 Gb/s EPON equipment. The EPON operation is defined for distances of at least 20 km, and for a split ratio of at least 1:32.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.


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Document Sharing Hub
Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

# Contents

1. Introduction ..... 23

1.3 Normative references ..... 23
1.4 Definitions ..... 23
1.5 Abbreviations ..... 25

30. Management ..... 26

30.3 Layer management for DTEs ..... 26
30.3.2 PHY device managed object class ..... 26
30.3.2.1 PHY device attributes ..... 26
30.3.2.1.2 aPhyType ..... 26
30.3.2.1.3 aPhyTypeList ..... 26
30.3.5 MPCP managed object class ..... 27
30.3.5.1 MPCP Attributes ..... 27
30.3.5.1.2 aMPCPAdminState ..... 27
30.3.5.1.3 aMPCPMode ..... 27
30.3.5.1.4 aMPCPLinkID ..... 27
30.5 Layer management for medium attachment units (MAUs) ..... 27
30.5.1 MAU managed object class ..... 27
30.5.1.1 MAU attributes ..... 27
30.5.1.1.2 aMAUType ..... 27

45. Management Data Input/Output (MDIO) Interface ..... 31

45.2 MDIO Interface Registers ..... 31
45.2.1 PMA/PMD registers ..... 31
45.2.1.23a PMA/PMD control 3 register (Register 1.29) ..... 31
45.2.1.23a.1 Downstream differential encoding (1.29.15) ..... 31
45.2.1.23a.2 PMA/PMD type selection (1.29.5:0) ..... 31
45.2.1.134a Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002) ..... 33
45.2.1.134a.1 25GBASE-PQX-U3 (1.1000.15) ..... 35
45.2.1.134a.2 25GBASE-PQX-U2 (1.1000.14) ..... 35
45.2.1.134a.3 25GBASE-PQX-D3 (1.1000.13) ..... 35
45.2.1.134a.4 25GBASE-PQX-D2 (1.1000.12) ..... 35
45.2.1.134a.5 25GBASE-PQG-U3 (1.1000.11) ..... 35
45.2.1.134a.6 25GBASE-PQG-U2 (1.1000.10) ..... 35
45.2.1.134a.7 25GBASE-PQG-D3 (1.1000.9) ..... 36
45.2.1.134a.8 25GBASE-PQG-D2 (1.1000.8) ..... 36
45.2.1.134a.9 25/10GBASE-PQX-U3 (1.1000.7) ..... 36
45.2.1.134a.10 25/10GBASE-PQX-U2 (1.1000.6) ..... 36
45.2.1.134a.11 25/10GBASE-PQX-D3 (1.1000.5) ..... 36
45.2.1.134a.12 25/10GBASE-PQX-D2 (1.1000.4) ..... 36
45.2.1.134a.13 25/10GBASE-PQG-U3 (1.1000.3) ..... 36
45.2.1.134a.14 25/10GBASE-PQG-U2 (1.1000.2) ..... 36
45.2.1.134a.15 25/10GBASE-PQG-D3 (1.1000.1) ..... 36
45.2.1.134a.16 25/10GBASE-PQG-D2 (1.1000.0) ..... 37
45.2.1.134a.17 50/25GBASE-PQX-U3 (1.1001.15) ..... 37
45.2.1.134a.18 50/25GBASE-PQX-U2 (1.1001.14) ..... 37
45.2.1.134a.19 50/25GBASE-PQX-D3 (1.1001.13) ..... 37


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

45.2.1.134a.20 50/25GBASE-PQX-D2 (1.1001.12) ..... 37
45.2.1.134a.21 50/25GBASE-PQG-U3 (1.1001.11) ..... 37
45.2.1.134a.22 50/25GBASE-PQG-U2 (1.1001.10) ..... 37
45.2.1.134a.23 50/25GBASE-PQG-D3 (1.1001.9) ..... 37
45.2.1.134a.24 50/25GBASE-PQG-D2 (1.1001.8) ..... 37
45.2.1.134a.25 50/10GBASE-PQX-U3 (1.1001.7) ..... 38
45.2.1.134a.26 50/10GBASE-PQX-U2 (1.1001.6) ..... 38
45.2.1.134a.27 50/10GBASE-PQX-D3 (1.1001.5) ..... 38
45.2.1.134a.28 50/10GBASE-PQX-D2 (1.1001.4) ..... 38
45.2.1.134a.29 50/10GBASE-PQG-U3 (1.1001.3) ..... 38
45.2.1.134a.30 50/10GBASE-PQG-U2 (1.1001.2) ..... 38
45.2.1.134a.31 50/10GBASE-PQG-D3 (1.1001.1) ..... 38
45.2.1.134a.32 50/10GBASE-PQG-D2 (1.1001.0) ..... 38
45.2.1.134a.33 50GBASE-PQX-U3 (1.1002.7) ..... 38
45.2.1.134a.34 50GBASE-PQX-U2 (1.1002.6) ..... 39
45.2.1.134a.35 50GBASE-PQX-D3 (1.1002.5) ..... 39
45.2.1.134a.36 50GBASE-PQX-D2 (1.1002.4) ..... 39
45.2.1.134a.37 50GBASE-PQG-U3 (1.1002.3) ..... 39
45.2.1.134a.38 50GBASE-PQG-U2 (1.1002.2) ..... 39
45.2.1.134a.39 50GBASE-PQG-D3 (1.1002.1) ..... 39
45.2.1.134a.40 50GBASE-PQG-D2 (1.1002.0) ..... 39
45.2.3 PCS registers ..... 40
45.2.3.1 PCS control 1 register (Register 3.0) ..... 40
45.2.3.6 PCS control 2 register (Register 3.7) ..... 41
45.2.3.6.1 PCS type selection (3.7.34:0) ..... 41
45.2.3.8 PCS status 3 register (Register 3.9) ..... 41
45.2.3.8.aa 25GBASE-PQ capable (3.9.7) ..... 42
45.2.3.8.ab 25/10GBASE-PQ capable (3.9.6) ..... 42
45.2.3.8.ac 25GBASE-PQ Rx only capable (3.9.5) ..... 42
45.2.3.8.ad 25GBASE-PQ Tx only capable (3.9.4) ..... 42
45.2.3.41 10/1GBASE-PRX and 10GBASE-PR10G-EPON and Nx25G-EPON corrected FEC codewords counter (Register 3.76, 3.77) ..... 42
45.2.3.42 10/1GBASE-PRX and 10GBASE-PR10G-EPON and Nx25G-EPON uncorrected FEC codewords counter (Register 3.78, 3.79) ..... 43
45.2.3.43 10GBASE-PR and, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval timer control register (Register 3.80) ..... 43
45.2.3.44 10GBASE-PR and, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status (Register 3.81) ..... 44
45.2.3.44.1 10GBASE-PR and, 10/1GBASE-PRX, and Nx25G-EPON PCS high BER (3.81.0) ..... 44
45.2.3.44.2 10GBASE-PR and, 10/1GBASE-PRX, and Nx25G-EPON PCS latched high BER (3.81.1) ..... 45
45.2.3.45 10GBASE-PR and, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control (Register 3.82) ..... 45
45.2.3.45a Nx25G-EPON synchronization pattern registers (Registers 3.83 through 3.134) ..... 45
45.2.3.45a.1 SP3 bit 257 (3.83.5) ..... 46
45.2.3.45a.2 SP3 balanced (3.83.4) ..... 46
45.2.3.45a.3 SP2 bit 257 (3.83.3) ..... 46
45.2.3.45a.4 SP2 balanced (3.83.2) ..... 46
45.2.3.45a.5 SP1 bit 257 (3.83.1) ..... 47
45.2.3.45a.6 SP1 balanced (3.83.0) ..... 47
45.2.3.45a.7 SP1 pattern (3.84.0 through 3.99.15) ..... 47
45.2.3.45a.8 SP1 length (3.100.15:0) ..... 47


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

45.2.3.45a.9 SP2 pattern (3.101.0 through 3.116.15) ... 47
45.2.3.45a.10 SP2 length (3.117.15:0) ... 47
45.2.3.45a.11 SP3 pattern (3.118.0 through 3.133.15) ... 47
45.2.3.45a.12 SP3 length (3.134.15:0) ... 47
45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface ... 48
45.5.1 Introduction ... 48
45.5.2 Identification ... 48
45.5.2.1 Implementation identification ... 48
45.5.2.2 Protocol summary ... 48
45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface ... 49
45.5.3.3 PMA/PMD management functions ... 49
45.5.3.7 PCS management functions ... 49

56. Introduction to Ethernet for subscriber access networks ... 50

56.1 Overview ... 50
56.1.2 Summary of P2MP sublayers ... 50
56.1.2.1 Multipoint MAC Control Protocol (MPCP) ... 52
56.1.2.2 Reconciliation Sublayer (RS) and media independent interfaces ... 52
56.1.3 Physical Layer signaling systems ... 52

67. System considerations for Ethernet subscriber access networks ... 59

67.1 Overview ... 59

141. Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks ... 61

141.1 Overview ... 61
141.1.1 Terminology ... 61
141.1.2 Positioning of the PMD sublayer within the IEEE 802.3 architecture ... 61
141.1.3 PHY link types ... 61
141.2 PMD nomenclature ... 64
141.2.1 Introduction ... 64
141.2.2 PMD rate classes ... 64
141.2.3 PMD coexistence classes ... 64
141.2.4 PMD transmission direction classes ... 64
141.2.5 PMD power classes ... 64
141.2.6 PMD naming ... 65
141.2.7 Supported combinations of OLT and ONU PMDs ... 65
141.2.7.1 PHY Links supporting medium power budget ... 66
141.2.7.2 PHY Links supporting high power budget ... 67
141.3 PMD functional specifications ... 67
141.3.1 PMD service interface ... 67
141.3.1.1 Channel-to-wavelength mapping ... 67
141.3.1.2 Delay constraints ... 68
141.3.1.3 PMD_UNITDATA[i].request ... 68
141.3.1.4 PMD_UNITDATA[i].indication ... 68
141.3.1.5 PMD_SIGNAL[i].request ... 69
141.3.1.6 PMD_SIGNAL[i].indication ... 69
141.3.2 PMD block diagram ... 69
141.3.3 PMD transmit function ... 70
141.3.4 PMD receive function ... 70


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Documents
Document Sharing Hub
Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

141.3.5 PMD signal detect function ... 70
141.3.5.1 ONU PMD signal detect ... 70
141.3.5.2 OLT PMD signal detect ... 71
141.3.5.3 Nx25G-EPON signal detect functions ... 71
141.4 Wavelength allocation ... 71
141.5 PMD to MDI optical specifications for OLT PMDs ... 72
141.5.1 Transmitter optical specifications ... 72
141.5.2 Receiver optical specifications ... 72
141.6 PMD to MDI optical specifications for ONU PMDs ... 77
141.6.1 Transmitter optical specifications ... 77
141.6.2 Receiver optical specifications ... 80
141.7 Definitions of optical parameters and measurement methods ... 82
141.7.1 Insertion loss ... 82
141.7.2 Test patterns ... 82
141.7.3 Wavelength and spectral width measurement ... 82
141.7.4 Optical power measurements ... 82
141.7.5 Extinction ratio measurements ... 82
141.7.6 Optical Modulation Amplitude (OMA) test procedure ... 82
141.7.7 Relative intensity noise optical modulation amplitude (RINxOMA) measuring procedure ... 82
141.7.8 Transmit optical waveform (transmit eye) ... 83
141.7.9 Transmitter and dispersion penalty (TDP) for 25G ... 83
141.7.9.1 Reference transmitter requirements ... 83
141.7.9.2 Channel requirements ... 83
141.7.9.3 Reference receiver requirements ... 83
141.7.9.4 Test procedure ... 83
141.7.10 Receive sensitivity ... 84
141.7.11 Stressed receiver conformance test ... 84
141.7.12 Jitter measurements ... 84
141.7.13 Laser on/off timing measurement ... 84
141.7.13.1 Definitions ... 84
141.7.13.2 Test specification ... 84
141.7.14 Receiver settling timing measurement ... 86
141.7.14.1 Definitions ... 86
141.7.14.2 Test specification ... 86
141.8 Environmental, safety, and labeling ... 87
141.8.1 General safety ... 87
141.8.2 Laser safety ... 87
141.8.3 Installation ... 87
141.8.4 Environment ... 87
141.8.5 PMD labeling ... 87
141.9 Characteristics of the fiber optic cabling ... 88
141.9.1 Fiber optic cabling model ... 88
141.9.2 Optical fiber and cable ... 88
141.9.3 Optical fiber connection ... 88
141.9.4 Medium Dependent Interface (MDI) ... 89
141.10 Protocol implementation conformance statement (PICS) proforma for Clause 141, Physical Medium Dependent (PMD) sublayer and medium for Nx25G-EPON passive optical networks ... 90
141.10.1 Introduction ... 90
141.10.2 Identification ... 90
141.10.2.1 Implementation identification ... 90
141.10.2.2 Protocol summary ... 90
141.10.3 Major capabilities/options ... 91


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

141.10.4 PICS proforma tables for Physical Medium Dependent (PMD) sublayer and medium for passive optical networks, type 25/10GBASE-PQ, 25GBASE-PQ, 50/10GBASE-PQ, 50/25GBASE-PQ, and 50GBASE-PQ ..... 94
141.10.4.1 PMD functional specifications ..... 94
141.10.4.2 PMD to MDI optical specifications for 25/10GBASE-PQG-D2 ..... 95
141.10.4.3 PMD to MDI optical specifications for 25/10GBASE-PQG-D3 ..... 95
141.10.4.4 PMD to MDI optical specifications for 25/10GBASE-PQX-D2 ..... 95
141.10.4.5 PMD to MDI optical specifications for 25/10GBASE-PQX-D3 ..... 96
141.10.4.6 PMD to MDI optical specifications for 25GBASE-PQG-D2 ..... 96
141.10.4.7 PMD to MDI optical specifications for 25GBASE-PQG-D3 ..... 96
141.10.4.8 PMD to MDI optical specifications for 25GBASE-PQX-D2 ..... 96
141.10.4.9 PMD to MDI optical specifications for 25GBASE-PQX-D3 ..... 97
141.10.4.10 PMD to MDI optical specifications for 50/10GBASE-PQG-D2 ..... 97
141.10.4.11 PMD to MDI optical specifications for 50/10GBASE-PQG-D3 ..... 97
141.10.4.12 PMD to MDI optical specifications for 50/10GBASE-PQX-D2 ..... 97
141.10.4.13 PMD to MDI optical specifications for 50/10GBASE-PQX-D3 ..... 98
141.10.4.14 PMD to MDI optical specifications for 50/25GBASE-PQG-D2 ..... 98
141.10.4.15 PMD to MDI optical specifications for 50/25GBASE-PQG-D3 ..... 98
141.10.4.16 PMD to MDI optical specifications for 50/25GBASE-PQX-D2 ..... 98
141.10.4.17 PMD to MDI optical specifications for 50/25GBASE-PQX-D3 ..... 99
141.10.4.18 PMD to MDI optical specifications for 50GBASE-PQG-D2 ..... 99
141.10.4.19 PMD to MDI optical specifications for 50GBASE-PQG-D3 ..... 99
141.10.4.20 PMD to MDI optical specifications for 50GBASE-PQX-D2 ..... 99
141.10.4.21 PMD to MDI optical specifications for 50GBASE-PQX-D3 ..... 100
141.10.4.22 PMD to MDI optical specifications for 25/10GBASE-PQG-U2 ..... 100
141.10.4.23 PMD to MDI optical specifications for 25/10GBASE-PQG-U3 ..... 100
141.10.4.24 PMD to MDI optical specifications for 25/10GBASE-PQX-U2 ..... 100
141.10.4.25 PMD to MDI optical specifications for 25/10GBASE-PQX-U3 ..... 101
141.10.4.26 PMD to MDI optical specifications for 25GBASE-PQG-U2 ..... 101
141.10.4.27 PMD to MDI optical specifications for 25GBASE-PQG-U3 ..... 101
141.10.4.28 PMD to MDI optical specifications for 25GBASE-PQX-U2 ..... 101
141.10.4.29 PMD to MDI optical specifications for 25GBASE-PQX-U3 ..... 102
141.10.4.30 PMD to MDI optical specifications for 50/10GBASE-PQG-U2 ..... 102
141.10.4.31 PMD to MDI optical specifications for 50/10GBASE-PQG-U3 ..... 102
141.10.4.32 PMD to MDI optical specifications for 50/10GBASE-PQX-U2 ..... 102
141.10.4.33 PMD to MDI optical specifications for 50/10GBASE-PQX-U3 ..... 103
141.10.4.34 PMD to MDI optical specifications for 50/25GBASE-PQG-U2 ..... 103
141.10.4.35 PMD to MDI optical specifications for 50/25GBASE-PQG-U3 ..... 103
141.10.4.36 PMD to MDI optical specifications for 50/25GBASE-PQX-U2 ..... 103
141.10.4.37 PMD to MDI optical specifications for 50/25GBASE-PQX-U3 ..... 104
141.10.4.38 PMD to MDI optical specifications for 50GBASE-PQG-U2 ..... 104
141.10.4.39 PMD to MDI optical specifications for 50GBASE-PQG-U3 ..... 104
141.10.4.40 PMD to MDI optical specifications for 50GBASE-PQX-U2 ..... 104
141.10.4.41 PMD to MDI optical specifications for 50GBASE-PQX-U3 ..... 105
141.10.4.42 Definitions of optical parameters and measurement methods ..... 105
141.10.4.43 Characteristics of the fiber optic cabling and MDI ..... 106
141.10.4.44 Environmental specifications ..... 106

142. Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON ..... 107

142.1 Overview ..... 107
142.1.1 Conventions ..... 107
142.1.1.1 State diagrams ..... 107
142.1.1.2 Hexadecimal notation ..... 107


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

142.1.1.3 Timers ... 110
142.1.1.4 Operations on variables ... 110
142.1.1.5 Operations on wrap-around variables ... 111
142.1.1.6 FIFO access operations ... 111
142.1.2 Delay constraints ... 112
142.1.3 Burst transmission ... 112
142.1.3.1 Default synchronization pattern parameters ... 113
142.2 PCS transmit data path ... 114
142.2.1 64B/66B line encoder ... 114
142.2.2 Scrambler ... 116
142.2.3 64B/66B to 256B/257B transcoder ... 116
142.2.4 FEC encoder ... 116
142.2.4.1 Low-density parity-check coding ... 116
142.2.4.2 FEC encoder processing ... 119
142.2.4.3 Interleaver ... 121
142.2.5 Transmit data path state diagrams ... 126
142.2.5.1 Constants ... 126
142.2.5.2 Variables ... 127
142.2.5.3 Functions ... 129
142.2.5.4 State diagrams ... 130
142.2.5.4.1 PCS Input process ... 130
142.2.5.4.2 PCS Framer process ... 131
142.2.5.4.3 PCS Transmit process ... 132
142.3 PCS receive data path ... 133
142.3.1 FEC decoder ... 133
142.3.1.1 Receive interleaving ... 133
142.3.2 256B/257B to 64B/66B transcoder ... 134
142.3.3 Descrambler ... 134
142.3.4 64B/66B decoder ... 135
142.3.5 Receive data path state diagrams ... 136
142.3.5.1 Constants ... 136
142.3.5.2 Variables ... 137
142.3.5.3 Functions ... 139
142.3.5.4 OLT Synchronizer process state diagram ... 140
142.3.5.5 ONU Synchronizer process state diagram ... 140
142.3.5.6 PCS ONU BER Monitor process ... 141
142.3.5.7 PCS Output process ... 142
142.4 Nx25G-EPON PMA ... 142
142.4.1 Service Interface ... 142
142.4.1.1 PMA_UNITDATA[i].request ... 143
142.4.1.1.1 Semantics of the service primitive ... 143
142.4.1.1.2 When generated ... 143
142.4.1.1.3 Effect of receipt ... 143
142.4.1.2 PMA_UNITDATA[i].indication ... 143
142.4.1.2.1 Semantics of the service primitive ... 143
142.4.1.2.2 When generated ... 143
142.4.1.2.3 Effect of receipt ... 143
142.4.1.3 PMA_SIGNAL[i].request ... 144
142.4.1.4 PMA_SIGNAL[i].indication ... 144
142.4.1.4.1 Semantics of the service primitive ... 144
142.4.1.4.2 When generated ... 144
142.4.1.4.3 Effect of receipt ... 144
142.4.2 Differential encoder ... 144
142.4.3 Differential decoder ... 145


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

142.4.4 PMA transmit clock ... 145
142.4.4.1 Loop-timing specifications for ONUs ... 145
142.4.5 TCDR measurement ... 145
142.4.5.1 Definitions ... 145
142.4.5.2 Test specification ... 145
142.5 Protocol implementation conformance statement (PICS) proforma for Clause 142, Physical Coding Sublayer and Physical Media Attachment for Nx25G-EPON ... 147
142.5.1 Introduction ... 147
142.5.2 Identification ... 147
142.5.2.1 Implementation identification ... 147
142.5.2.2 Protocol summary ... 147
142.5.3 PCS capabilities/options ... 148
142.5.4 PCS processes ... 148
142.5.5 PMA processes ... 149

143. Multi-Channel Reconciliation Sublayer ... 150

143.1 Overview ... 150
143.2 Summary of major concepts ... 150
143.2.1 Concept of a logical link and LLID ... 151
143.2.2 Concept of an MCRS channel ... 151
143.2.3 Binding of multiple MACs to multiple xMII instances ... 151
143.2.4 Transmission and reception over multiple MCRS channels ... 152
143.2.4.1 Transmission unit ... 152
143.2.4.2 Transmission envelopes ... 152
143.2.4.3 Envelope headers ... 152
143.2.4.4 Interpacket gap adjustment ... 153
143.2.5 Dynamic channel bonding ... 154
143.2.5.1 LLID transmission over multiple MCRS channels ... 155
143.2.5.2 MCRS channel skew remediation mechanism ... 156
143.2.5.3 *EnvTx* and *EnvRx* buffers ... 156
143.2.5.4 Envelope position alignment marker ... 158
143.2.6 MDIO addressing model for multi-channel architecture ... 158
143.3 MCRS functional specifications ... 160
143.3.1 MCRS interfaces ... 160
143.3.1.1 PLS service primitives ... 160
143.3.1.1.1 Mapping of PLS_DATA[ch].request primitive ... 161
143.3.1.1.2 Mapping of PLS_SIGNAL[ch].indication primitive ... 161
143.3.1.1.3 Mapping of PLS_DATA[ch].indication primitive ... 161
143.3.1.1.4 Mapping of PLS_DATA_VALID[ch].indication primitive ... 162
143.3.1.1.5 Mapping of PLS_CARRIER[ch].indication primitive ... 162
143.3.1.2 MCRS control primitives ... 162
143.3.1.2.1 MCRS_CTRL[ch].request(link_id, epam, env_length) primitive ... 162
143.3.1.2.2 MCRS_CTRL[ch].indication() primitive ... 162
143.3.1.2.3 MCRS_ECH[ch].indication(Llid) primitive ... 162
143.3.1.3 XGMII interfaces ... 162
143.3.1.4 25GMII interfaces ... 162
143.3.2 Envelope header format ... 163
143.3.2.1 CRC8 calculation test sequences ... 164
143.3.3 Transmit functional specifications ... 165
143.3.3.1 Conventions ... 166
143.3.3.2 Application-specific parameter definitions ... 166
143.3.3.3 Constants ... 166
143.3.3.4 Variables ... 167


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

143.3.3.5 Functions ... 169
143.3.3.6 State diagrams ... 171
143.3.3.6.1 Input process ... 171
143.3.3.6.2 Transmit process ... 171
143.3.4 Receive functional specifications ... 173
143.3.4.1 Conventions ... 174
143.3.4.2 Constants ... 174
143.3.4.3 Variables ... 175
143.3.4.4 Functions ... 176
143.3.4.5 State diagrams ... 177
143.3.4.5.1 Receive process ... 177
143.3.4.5.2 Output process ... 178
143.4 Nx25G-EPON MCRS requirements ... 178
143.4.1 Nx25G-EPON architecture ... 178
143.4.1.1 MCRS channels ... 180
143.4.1.2 Symmetric and asymmetric data rates ... 180
143.4.1.3 Nx25G-EPON application-specific parameters ... 181
143.4.1.3.1 Constants ... 181
143.4.1.3.2 Transmit variables ... 181
143.4.2 MCRS time synchronization ... 181
143.4.3 Delay variability constraints ... 182
143.4.4 Asymmetric rate operation ... 182
143.5 Protocol implementation conformance statement (PICS) proforma for Clause 143, Multi-Channel Reconciliation Sublayer ... 185
143.5.1 Introduction ... 185
143.5.2 Identification ... 185
143.5.2.1 Implementation identification ... 185
143.5.2.2 Protocol summary ... 185
143.5.3 Generic MCRS ... 186
143.5.4 MCRS in Nx25G-EPON ... 186
143.5.4.1 Major capabilities/option ... 186
143.5.4.2 MCRS implementation in Nx25G-EPON ... 187

144. Multipoint MAC Control for Nx25G-EPON ... 188

144.1 Overview ... 188
144.1.1 Principles of point-to-multipoint operation ... 188
144.1.1.1 Transmission arbitration ... 188
144.1.1.2 Concept of logical links ... 189
144.1.1.3 ONU discovery and registration ... 191
144.1.2 Position of Multipoint MAC Control (MPMC) within the IEEE 802.3 hierarchy ... 191
144.1.3 Functional block diagram ... 191
144.1.4 Service interfaces ... 191
144.1.4.1 MAC Control service (MCS) interface ... 191
144.1.4.2 MAC Control interconnect (MCI) ... 194
144.1.4.3 MAC service Interface ... 194
144.1.4.4 MCRS Control interface ... 194
144.1.5 Conventions ... 194
144.2 Protocol-independent operation ... 194
144.2.1 Control Parser and Control Multiplexer ... 195
144.2.1.1 Constants ... 195
144.2.1.2 Counters ... 195
144.2.1.3 Variables ... 195
144.2.1.4 Functions ... 196


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

144.2.1.5 Control Parser state diagram ..... 197
144.2.1.6 Control Multiplexer state diagram ..... 198
144.3 Multipoint Control Protocol (MPCP) ..... 198
144.3.1 Principles of Multipoint Control Protocol (MPCP) ..... 198
144.3.1.1 Ranging measurement and time synchronization ..... 198
144.3.1.2 Granting access to the PON media by the OLT ..... 201
144.3.2 MPCP block diagram ..... 202
144.3.3 Delay variability requirements ..... 204
144.3.4 Logical link identifier (LLID) types ..... 204
144.3.4.1 Physical Layer ID (PLID) ..... 204
144.3.4.2 Management link ID (MLID) ..... 205
144.3.4.3 User link ID (ULID) ..... 205
144.3.4.4 Group link ID (GLID) ..... 205
144.3.5 Allocation of LLID values ..... 205
144.3.6 MPCPDU structure and encoding ..... 206
144.3.6.1 GATE description ..... 207
144.3.6.2 REPORT description ..... 209
144.3.6.3 REGISTER_REQ description ..... 211
144.3.6.4 REGISTER description ..... 212
144.3.6.5 REGISTER_ACK description ..... 214
144.3.6.6 DISCOVERY description ..... 216
144.3.6.7 SYNC_PATTERN description ..... 218
144.3.7 Discovery process ..... 220
144.3.7.1 Constants ..... 222
144.3.7.2 Counters ..... 223
144.3.7.3 Variables ..... 223
144.3.7.4 Functions ..... 225
144.3.7.5 Messages ..... 226
144.3.7.6 Discovery Initiation state diagram ..... 226
144.3.7.7 Registration Completion state diagram ..... 227
144.3.7.8 ONU Registration state diagram ..... 228
144.3.8 Granting process ..... 230
144.3.8.1 Constants ..... 230
144.3.8.2 Counters ..... 231
144.3.8.3 Variables ..... 231
144.3.8.4 Functions ..... 232
144.3.8.5 Timers ..... 232
144.3.8.6 Messages ..... 232
144.3.8.7 GATE Generation state diagram ..... 232
144.3.8.8 GATE Reception state diagram ..... 233
144.3.8.9 OLT Envelope Commitment state diagram ..... 233
144.3.8.10 ONU Envelope Commitment state diagram ..... 234
144.3.8.11 Envelope Activation state diagram ..... 235
144.3.9 Discovery process in dual-rate systems ..... 235
144.3.9.1 OLT rate-specific discovery ..... 235
144.3.9.2 ONU rate-specific registration ..... 236
144.4 Channel Control Protocol (CCP) ..... 237
144.4.1 CCP block diagram ..... 237
144.4.2 Principles of Channel Control Protocol ..... 238
144.4.2.1 Disabling a downstream channel at an ONU ..... 239
144.4.2.2 Enabling a downstream channel at an ONU ..... 239
144.4.2.3 Disabling an upstream channel at an ONU ..... 239
144.4.2.4 Enabling an upstream channel at an ONU ..... 240
144.4.2.5 Local channel state changes at an ONU ..... 240


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Documents
Document Sharing Hub

Full document details: ISO IEC IEEE 08802-3-2021 amd9-2021

144.4.3 CCPDU structure and encoding ..... 240
144.4.3.1 CC_REQUEST description ..... 241
144.4.3.2 CC_RESPONSE description ..... 243
144.4.4 Channel Control operation ..... 244
144.4.4.1 Constants ..... 244
144.4.4.2 Variables ..... 245
144.4.4.3 Functions ..... 246
144.4.4.4 Messages ..... 247
144.4.4.5 OLT CCPDU processing state diagram ..... 247
144.4.4.6 ONU CCPDU processing state diagram ..... 248
144.5 Protocol implementation conformance statement (PICS) proforma for Clause 144, Multipoint MAC Control for Nx25G-EPON ..... 249
144.5.1 Introduction ..... 249
144.5.2 Identification ..... 249
144.5.2.1 Implementation identification ..... 249
144.5.2.2 Protocol summary ..... 249
144.5.3 Major capabilities/options ..... 250
144.5.4 PICS proforma tables for Multipoint MAC Control ..... 250
144.5.4.1 Clock tracking ..... 250
144.5.4.2 LLID ..... 250
144.5.4.3 Protocol-independent state diagrams ..... 251
144.5.4.4 MPCP ..... 251
144.5.4.5 CCP ..... 254

Annex A (informative) Bibliography ..... 255

Annex 31A (normative) MAC Control opcode assignments ..... 256

Annex 142A (informative) Encoding example for QC-LDPC(16952,14392) FEC and interleaving ..... 258

142A.1 Example of initial control seed sequence ..... 258
142A.2 QC-LDPC FEC encoder test vectors ..... 258


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# IEEE Standard for Ethernet

# Amendment 9: Physical Layer Specifications and Management Parameters for 25 Gb/s and 50 Gb/s Passive Optical Networks

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018, IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018, IEEE Std 802.3cn™-2019, IEEE Std 802.3cg™-2019, IEEE Std 802.3cq™-2020, IEEE Std 802.3cm™-2020, and IEEE Std 802.3ch™-2020.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

[1] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.


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# 1. Introduction

## 1.3 Normative references

***Change the references for ITU-T Recommendations G.652 and G.657 as follows:***

ITU-T Recommendation G.652, ~~2009~~2016—Characteristics of a single-mode optical fibre and cable.[2]

ITU-T Recommendation G.657, ~~2009~~2016—Characteristics of a bending-loss insensitive single-mode optical fibre and cable~~ for the access network~~.

## 1.4 Definitions

***Insert the following two new definitions after 1.4.90 "200GXS":***

**1.4.90a 25/10G-EPON:** An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate).

**1.4.90b 25/25G-EPON:** An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in both downstream and upstream directions (symmetric rate).

***Insert the following new definition after 1.4.100 "25GBASE-T":***

**1.4.100a 25G-EPON:** An EPON architecture supporting a maximum sustained throughput of 25 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 25/10G-EPON and 25/25G-EPON architectures.

***Insert the following three new definitions before 1.4.128aa "50GBASE-CR" as inserted by IEEE Std 802.3cd-2018:***

**1.4.128aaa 50/10G-EPON:** An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 10 Gb/s in the upstream direction (asymmetric rate).

**1.4.128aab 50/25G-EPON:** An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in the downstream direction and 25 Gb/s in the upstream direction (asymmetric rate).

**1.4.128aac 50/50G-EPON:** An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in both downstream and upstream directions (symmetric rate).

***Insert the following new definition after 1.4.128ah "50 Gb/s Media Independent Interface (50GMII)" as inserted by IEEE Std 802.3cd-2018:***

**1.4.128ai 50G-EPON:** An EPON architecture supporting a maximum sustained throughput of 50 Gb/s in either downstream or both downstream and upstream directions. This term collectively refers to 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures.

***Insert the following three new definitions after 1.4.244 "Energy-Efficient Ethernet (EEE)":***

**1.4.244a envelope:** In the Multi-Channel Reconciliation Sublayer (MCRS, see IEEE Std 802.3, Clause 143), an envelope encapsulates data belonging to a specific LLID being transmitted on a specific

[2]ITU-T publications are available from the International Telecommunications Union (https://www.itu.int/).


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MCRS channel, i.e., the data or idles sourced from a specific MAC instance and sent over a specific MCRS channel.

**1.4.244b envelope allocation:** In Nx25G-EPON, an envelope allocation represents a transmission window allocated to a single LLID (including GLID). A single GATE MPCPDU can carry up to seven envelope allocations.

**1.4.244c envelope descriptor:** A set of parameters consisting of LLID, StartTime, and EnvLength. An envelope descriptor defines a specific envelope pending transmission. Envelope descriptors are generated by the local MPCP sublayer and are passed to MCRS at the appropriate time to start the envelope transmission.

***Insert the following three new definitions after 1.4.245 "envelope frame":***

**1.4.245a envelope header:** An MCRS-specific marker that is inserted at the beginning of every envelope (envelope start header) and in place of every frame preamble (envelope continuation header). The envelope header includes fields that identify the LLID that sourced the encapsulated data and the length of the data (in units of EQ). Envelope headers also include a CRC8 field used to detect bit errors.

**1.4.245b envelope quantum:** A unit of information volume. Each envelope quantum represents 64 bits of data plus the layer-specific encoding. Thus, at the MAC Control sublayer and above, an envelope quantum is equal to 64 bits. Within the MCRS, an envelope quantum contains 72 bits (i.e., 64 bits of data and 8 bits of control). Within the PCS, after the 64B/66B encoding, an envelope quantum contains 66 bits, and after 256B/257B encoding, four envelope quanta are packed into a single 257-bit block.

**1.4.245c EQT:** The unit of measurement of time for time-related parameters specified in IEEE Std 802.3, Clause 144 Multipoint MAC Control for Nx25G-EPON. Each EQT is equal to the time required to transmit one EQ between the MCRS and the PCS across 25GMII, and equal to 2.56 ns.

***Insert the following new definition after 1.4.277 "Gigabit Media Independent Interface (GMII)":***

**1.4.277a GPON:** A Gigabit-capable Passive Optical Network, as specified in ITU-T G.984.2.

NOTE—ITU-T G.984.2 [B48a].

***Change definition 1.4.278 as shown below:***

**1.4.278 grant:** Within P2MP protocols, a permission to transmit at a specific time, for a specific duration. Grants are issued by the OLT (master) to ONUs (slaves) by means of GATE messages. In IEEE Std 802.3, Clause 64 and Clause 77, a GATE MPCPDU contains one or multiple grants issued to a single LLID, with each grant resulting in one or multiple upstream bursts transmitted by the ONU. In Clause 144, a grant includes envelope allocations for multiple LLIDs and there is a one-to-one correspondence between the grants issued to an ONU and upstream bursts transmitted by that ONU.

***Change 1.4.312 (renumbered from 1.4.313 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018) as follows:***

**1.4.312 Logical Link Identifier (LLID):** A numeric identifier assigned to a P2MP association between an OLT and ONU established through the Point-to-Point Emulation sublayer. Each P2MP association is assigned a unique LLID. The P2MP association is bound to an ONU DTE, where ~~a~~ the ONU MAC ~~would~~ is to observe a private association. In Nx25G-EPON, an LLID is also a collective term that refers to a Physical Layer ID (PLID), management link ID (MLID), user link ID (ULID), and a group link ID (GLID).


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***Insert the following new definition after 1.4.319 "maximum differential input" (renumbered from 1.4.320 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):***

**1.4.319a MCRS channel:** In IEEE Std 802.3, Clause 143, an MCRS channel represents one of a number of defined paths along which data passes in an MCRS.

***Insert the following new definition after 1.4.332 "modulation error ratio (MER)" (renumbered from 1.4.333 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):***

**1.4.332a Multi-Channel Reconciliation Sublayer (MCRS)**: The MCRS provides a mapping function that reconciles the signals at a specific Media Independent Interface (xMII) to a specific Media Access Control (MAC) Physical Signaling Sublayer (PLS) service definitions.

***Insert the following new definition after 1.4.350 "NRZI" (renumbered from 1.4.351 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018):***

**1.4.350a Nx25G-EPON:** An EPON architecture operating at a number of different downstream and upstream speeds. This term collectively refers to 25/10G-EPON, 25/25G-EPON, 50/10G-EPON, 50/25G-EPON, and 50/50G-EPON architectures.

## 1.5 Abbreviations

***Insert the following new abbreviations into the list, in alphabetical order:***

| | |
|---|---|
| ECH | envelope continuation header |
| EQ | envelope quantum |
| EQT | envelope quantum time |
| ESH | envelope start header |
| GLID | group link ID |
| GPON | Gigabit-capable Passive Optical Network (see ITU-T G.984.2 [B48a]) |
| MACI | MA_CONTROL.indication |
| MACR | MA_CONTROL.request |
| MADI | MA_DATA.indication |
| MADR | MA_DATA.request |
| MCRS | Multi-Channel Reconciliation Sublayer |
| MLID | management link ID |
| PLID | Physical Layer ID |
| QC-LDPC | quasi-cyclic low-density parity check |
| ULID | user link ID |


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# 30. Management

## 30.3 Layer management for DTEs

### 30.3.2 PHY device managed object class

#### 30.3.2.1 PHY device attributes

#### 30.3.2.1.2 aPhyType

***Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 25GBASE-T as follows:***

…
25GBASE-PQ Clause 142 25/25G-EPON 256B/257B
25/10GBASE-PQ Clause 142 25/10G-EPON 256B/257B
…

***Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 50GBASE-R (inserted by IEEE Std 802.3cd-2018) as follows:***

…
50GBASE-PQ Clause 142 50/50G-EPON 256B/257B
50/25GBASE-PQ Clause 142 50/25G-EPON 256B/257B
50/10GBASE-PQ Clause 142 50/10G-EPON 256B/257B
…

#### 30.3.2.1.3 aPhyTypeList

***Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 25GBASE-T as follows:***

…
25GBASE-PQ Clause 142 25/25G-EPON 256B/257B
25/10GBASE-PQ Clause 142 25/10G-EPON 256B/257B
…

***Insert new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 50GBASE-R (inserted by IEEE Std 802.3cd-2018) as follows:***

…
50GBASE-PQ Clause 142 50/50G-EPON 256B/257B
50/25GBASE-PQ Clause 142 50/25G-EPON 256B/257B
50/10GBASE-PQ Clause 142 50/10G-EPON 256B/257B
…


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#### 30.3.5 MPCP managed object class

#### 30.3.5.1 MPCP Attributes

#### 30.3.5.1.2 aMPCPAdminState

***Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.2 as follows:***

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, ~~or~~ Clause 103, or Clause 144 is enabled to do so when this attribute has the enumeration "enabled". When this attribute has the enumeration "disabled", the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

#### 30.3.5.1.3 aMPCPMode

***Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.3 as follows:***

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, Clause 77, ~~or~~ Clause 103, or Clause 144. When this attribute has the enumeration "OLT", the interface acts as an OLT. When this attribute has the enumeration "ONU", the interface acts as an ONU. When this attribute has the enumeration "CLT", the interface acts as a CLT. When this attribute has the enumeration "CNU", the interface acts as a CNU.;

#### 30.3.5.1.4 aMPCPLinkID

***Change the text of the BEHAVIOUR DEFINED AS section of 30.3.5.1.3 as follows:***

BEHAVIOUR DEFINED AS:

A read-only value that identifies the Logical Link identity (LLID) associated with the MAC port as specified in 65.1.3.2.2, ~~or~~ 76.2.6.1.3.2, or 144.3.4, as appropriate.;

### 30.5 Layer management for medium attachment units (MAUs)

#### 30.5.1 MAU managed object class

#### 30.5.1.1 MAU attributes

#### 30.5.1.1.2 aMAUType

***Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 25GBASE-T as follows:***

…

| | |
|---|---|
| 25/10GBASE-PQG-D2 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141 |


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| | |
|---|---|
| 25/10GBASE-PQG-D3 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 25/10GBASE-PQG-U2 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 25/10GBASE-PQG-U3 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 25/10GBASE-PQX-D2 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 25/10GBASE-PQX-D3 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 25/10GBASE-PQX-U2 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 25/10GBASE-PQX-U3 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 25GBASE-PQG-D2 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 25GBASE-PQG-D3 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 25GBASE-PQG-U2 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 25GBASE-PQG-U3 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 25GBASE-PQX-D2 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 25GBASE-PQX-D3 | One single mode fiber, 1 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 25GBASE-PQX-U2 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 25GBASE-PQX-U3 | One single mode fiber, 1 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |

…

***Insert new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 50GBASE-ER (inserted by IEEE Std 802.3cn-2019) as follows:***

...

| | |
|---|---|
| 50/10GBASE-PQG-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141 |


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| | |
|---|---|
| 50/10GBASE-PQG-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50/10GBASE-PQG-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 50/10GBASE-PQG-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 50/10GBASE-PQX-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 50/10GBASE-PQX-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 10.3125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50/10GBASE-PQX-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 50/10GBASE-PQX-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 10.3125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 50/25GBASE-PQG-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 50/25GBASE-PQG-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50/25GBASE-PQG-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 50/25GBASE-PQG-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 50/25GBASE-PQX-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 50/25GBASE-PQX-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 1 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50/25GBASE-PQX-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 50/25GBASE-PQX-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 1 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 50GBASE-PQG-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 50GBASE-PQG-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50GBASE-PQG-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |


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| | |
|---|---|
| 50GBASE-PQG-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |
| 50GBASE-PQX-D2 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, medium power class, as specified in Clause 141 |
| 50GBASE-PQX-D3 | One single mode fiber, 2 × 25.78125 GBd continuous transmission / 2 × 25.78125 GBd burst mode reception, high power class, as specified in Clause 141 |
| 50GBASE-PQX-U2 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, medium power class, as specified in Clause 141 |
| 50GBASE-PQX-U3 | One single mode fiber, 2 × 25.78125 GBd continuous reception / 2 × 25.78125 GBd burst mode transmission, high power class, as specified in Clause 141 |

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# 45. Management Data Input/Output (MDIO) Interface

## 45.2 MDIO Interface Registers

### 45.2.1 PMA/PMD registers

***Change rows for 1.29 and 1.901 through 1.1099 in Table 45–3 as follows (unchanged rows not shown):***

**Table 45–3—PMA/PMD registers**

| Register address | Register name | Subclause |
|---|---|---|
| … | | |
| 1.29 | ~~Reserved~~PMA/PMD control 3 | 45.2.1.23a |
| … | | |
| 1.901 through 1.~~1099~~999 | Reserved | |
| 1.1000 through 1.1002 | Nx25G-EPON PMA/PMD extended ability | 45.2.1.134a |
| 1.1003 through 1.1099 | Reserved | |
| … | | |

***Insert 45.2.1.23a after 45.2.1.23 as follows:***

#### 45.2.1.23a PMA/PMD control 3 register (Register 1.29)

The assignment of bits in the PMA/PMD control 3 register is shown in Table 45–26a.

##### 45.2.1.23a.1 Downstream differential encoding (1.29.15)

Downstream differential encoding is selected using bit 1.29.15. This bit is read/write in the OLT and read only in the ONU with the default value of 0 (indicating that downstream differential encoding is not enabled).

In the OLT, this bit controls whether downstream differential encoding is selected for the transmit PMA output.

In the ONU, this bit indicates whether the downstream differential decoding is enabled in the ONU receive PMA.

##### 45.2.1.23a.2 PMA/PMD type selection (1.29.5:0)

The PMA/PMD type of the PMA/PMD is selected using bits 5 to 0. The PMA/PMD type abilities of the PMA/PMD are advertised in the Nx25G-EPON PMA/PMD extended ability registers (Registers 1.1000 through 1.1002, see 45.2.1.134a). A PMA/PMD shall ignore writes to the PMA/PMD type selection bits that select PMA/PMD types it has not advertised. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY.


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**Table 45–26a—PMA/PMD control 3 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.29.15 | Downstream differential encoding | 1 = Downstream differential encoding enabled<br>0 = Downstream differential encoding disabled | R/W in OLT<br>RO in ONU |
| 1.29.14:6 | Reserved | Value always 0 | RO |
| 1.29.5:0 | PMA/PMD type selection | 5 4 3 2 1 0<br>1 1 x x x x = Reserved<br>1 0 1 x x x = Reserved<br>1 0 0 1 1 1 = 50GBASE-PQX-U3<br>1 0 0 1 1 0 = 50GBASE-PQX-U2<br>1 0 0 1 0 1 = 50GBASE-PQX-D3<br>1 0 0 1 0 0 = 50GBASE-PQX-D2<br>1 0 0 0 1 1 = 50GBASE-PQG-U3<br>1 0 0 0 1 0 = 50GBASE-PQG-U2<br>1 0 0 0 0 1 = 50GBASE-PQG-D3<br>1 0 0 0 0 0 = 50GBASE-PQG-D2<br>0 1 1 1 1 1 = 50/25GBASE-PQX-U3<br>0 1 1 1 1 0 = 50/25GBASE-PQX-U2<br>0 1 1 1 0 1 = 50/25GBASE-PQX-D3<br>0 1 1 1 0 0 = 50/25GBASE-PQX-D2<br>0 1 1 0 1 1 = 50/25GBASE-PQG-U3<br>0 1 1 0 1 0 = 50/25GBASE-PQG-U2<br>0 1 1 0 0 1 = 50/25GBASE-PQG-D3<br>0 1 1 0 0 0 = 50/25GBASE-PQG-D2<br>0 1 0 1 1 1 = 50/10GBASE-PQX-U3<br>0 1 0 1 1 0 = 50/10GBASE-PQX-U2<br>0 1 0 1 0 1 = 50/10GBASE-PQX-D3<br>0 1 0 1 0 0 = 50/10GBASE-PQX-D2<br>0 1 0 0 1 1 = 50/10GBASE-PQG-U3<br>0 1 0 0 1 0 = 50/10GBASE-PQG-U2<br>0 1 0 0 0 1 = 50/10GBASE-PQG-D3<br>0 1 0 0 0 0 = 50/10GBASE-PQG-D2<br>0 0 1 1 1 1 = 25GBASE-PQX-U3<br>0 0 1 1 1 0 = 25GBASE-PQX-U2<br>0 0 1 1 0 1 = 25GBASE-PQX-D3<br>0 0 1 1 0 0 = 25GBASE-PQX-D2<br>0 0 1 0 1 1 = 25GBASE-PQG-U3<br>0 0 1 0 1 0 = 25GBASE-PQG-U2<br>0 0 1 0 0 1 = 25GBASE-PQG-D3<br>0 0 1 0 0 0 = 25GBASE-PQG-D2<br>0 0 0 1 1 1 = 25/10GBASE-PQX-U3<br>0 0 0 1 1 0 = 25/10GBASE-PQX-U2<br>0 0 0 1 0 1 = 25/10GBASE-PQX-D3<br>0 0 0 1 0 0 = 25/10GBASE-PQX-D2<br>0 0 0 0 1 1 = 25/10GBASE-PQG-U3<br>0 0 0 0 1 0 = 25/10GBASE-PQG-U2<br>0 0 0 0 0 1 = 25/10GBASE-PQG-D3<br>0 0 0 0 0 0 = 25/10GBASE-PQG-D2 | R/W |

[a]R/W = Read/Write, RO = Read only


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*Insert 45.2.1.134a after 45.2.1.134 as follows:*

### 45.2.1.134a Nx25G-EPON PMA/PMD extended ability register (Registers 1.1000 through 1.1002)

The assignment of bits in the Nx25G-EPON PMA/PMD extended ability register is shown in Table 45–103a.

**Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.1000.15 | 25GBASE-PQX-U3 | 1 = PMA/PMD is able to perform 25GBASE-PQX-U3<br>0 = PMA/PMD is not able to perform 25GBASE-PQX-U3 | RO |
| 1.1000.14 | 25GBASE-PQX-U2 | 1 = PMA/PMD is able to perform 25GBASE-PQX-U2<br>0 = PMA/PMD is not able to perform 25GBASE-PQX-U2 | RO |
| 1.1000.13 | 25GBASE-PQX-D3 | 1 = PMA/PMD is able to perform 25GBASE-PQX-D3<br>0 = PMA/PMD is not able to perform 25GBASE-PQX-D3 | RO |
| 1.1000.12 | 25GBASE-PQX-D2 | 1 = PMA/PMD is able to perform 25GBASE-PQX-D2<br>0 = PMA/PMD is not able to perform 25GBASE-PQX-D2 | RO |
| 1.1000.11 | 25GBASE-PQG-U3 | 1 = PMA/PMD is able to perform 25GBASE-PQG-U3<br>0 = PMA/PMD is not able to perform 25GBASE-PQG-U3 | RO |
| 1.1000.10 | 25GBASE-PQG-U2 | 1 = PMA/PMD is able to perform 25GBASE-PQG-U2<br>0 = PMA/PMD is not able to perform 25GBASE-PQG-U2 | RO |
| 1.1000.9 | 25GBASE-PQG-D3 | 1 = PMA/PMD is able to perform 25GBASE-PQG-D3<br>0 = PMA/PMD is not able to perform 25GBASE-PQG-D3 | RO |
| 1.1000.8 | 25GBASE-PQG-D2 | 1 = PMA/PMD is able to perform 25GBASE-PQG-D2<br>0 = PMA/PMD is not able to perform 25GBASE-PQG-D2 | RO |
| 1.1000.7 | 25/10GBASE-PQX-U3 | 1 = PMA/PMD is able to perform 25/10GBASE-PQX-U3<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U3 | RO |
| 1.1000.6 | 25/10GBASE-PQX-U2 | 1 = PMA/PMD is able to perform 25/10GBASE-PQX-U2<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQX-U2 | RO |
| 1.1000.5 | 25/10GBASE-PQX-D3 | 1 = PMA/PMD is able to perform 25/10GBASE-PQX-D3<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D3 | RO |
| 1.1000.4 | 25/10GBASE-PQX-D2 | 1 = PMA/PMD is able to perform 25/10GBASE-PQX-D2<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQX-D2 | RO |
| 1.1000.3 | 25/10GBASE-PQG-U3 | 1 = PMA/PMD is able to perform 25/10GBASE-PQG-U3<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U3 | RO |
| 1.1000.2 | 25/10GBASE-PQG-U2 | 1 = PMA/PMD is able to perform 25/10GBASE-PQG-U2<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQG-U2 | RO |
| 1.1000.1 | 25/10GBASE-PQG-D3 | 1 = PMA/PMD is able to perform 25/10GBASE-PQG-D3<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D3 | RO |
| 1.1000.0 | 25/10GBASE-PQG-D2 | 1 = PMA/PMD is able to perform 25/10GBASE-PQG-D2<br>0 = PMA/PMD is not able to perform 25/10GBASE-PQG-D2 | RO |
| 1.1001.15 | 50/25GBASE-PQX-U3 | 1 = PMA/PMD is able to perform 50/25GBASE-PQX-U3<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U3 | RO |


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**Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)***

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.1001.14 | 50/25GBASE-PQX-U2 | 1 = PMA/PMD is able to perform 50/25GBASE-PQX-U2<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQX-U2 | RO |
| 1.1001.13 | 50/25GBASE-PQX-D3 | 1 = PMA/PMD is able to perform 50/25GBASE-PQX-D3<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D3 | RO |
| 1.1001.12 | 50/25GBASE-PQX-D2 | 1 = PMA/PMD is able to perform 50/25GBASE-PQX-D2<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQX-D2 | RO |
| 1.1001.11 | 50/25GBASE-PQG-U3 | 1 = PMA/PMD is able to perform 50/25GBASE-PQG-U3<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U3 | RO |
| 1.1001.10 | 50/25GBASE-PQG-U2 | 1 = PMA/PMD is able to perform 50/25GBASE-PQG-U2<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQG-U2 | RO |
| 1.1001.9 | 50/25GBASE-PQG-D3 | 1 = PMA/PMD is able to perform 50/25GBASE-PQG-D3<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D3 | RO |
| 1.1001.8 | 50/25GBASE-PQG-D2 | 1 = PMA/PMD is able to perform 50/25GBASE-PQG-D2<br>0 = PMA/PMD is not able to perform 50/25GBASE-PQG-D2 | RO |
| 1.1001.7 | 50/10GBASE-PQX-U3 | 1 = PMA/PMD is able to perform 50/10GBASE-PQX-U3<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U3 | RO |
| 1.1001.6 | 50/10GBASE-PQX-U2 | 1 = PMA/PMD is able to perform 50/10GBASE-PQX-U2<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQX-U2 | RO |
| 1.1001.5 | 50/10GBASE-PQX-D3 | 1 = PMA/PMD is able to perform 50/10GBASE-PQX-D3<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D3 | RO |
| 1.1001.4 | 50/10GBASE-PQX-D2 | 1 = PMA/PMD is able to perform 50/10GBASE-PQX-D2<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQX-D2 | RO |
| 1.1001.3 | 50/10GBASE-PQG-U3 | 1 = PMA/PMD is able to perform 50/10GBASE-PQG-U3<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U3 | RO |
| 1.1001.2 | 50/10GBASE-PQG-U2 | 1 = PMA/PMD is able to perform 50/10GBASE-PQG-U2<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQG-U2 | RO |
| 1.1001.1 | 50/10GBASE-PQG-D3 | 1 = PMA/PMD is able to perform 50/10GBASE-PQG-D3<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D3 | RO |
| 1.1001.0 | 50/10GBASE-PQG-D2 | 1 = PMA/PMD is able to perform 50/10GBASE-PQG-D2<br>0 = PMA/PMD is not able to perform 50/10GBASE-PQG-D2 | RO |
| 1.1002.15:8 | Reserved | Value always 0 | RO |
| 1.1002.7 | 50GBASE-PQX-U3 | 1 = PMA/PMD is able to perform 50GBASE-PQX-U3<br>0 = PMA/PMD is not able to perform 50GBASE-PQX-U3 | RO |
| 1.1002.6 | 50GBASE-PQX-U2 | 1 = PMA/PMD is able to perform 50GBASE-PQX-U2<br>0 = PMA/PMD is not able to perform 50GBASE-PQX-U2 | RO |
| 1.1002.5 | 50GBASE-PQX-D3 | 1 = PMA/PMD is able to perform 50GBASE-PQX-D3<br>0 = PMA/PMD is not able to perform 50GBASE-PQX-D3 | RO |
| 1.1002.4 | 50GBASE-PQX-D2 | 1 = PMA/PMD is able to perform 50GBASE-PQX-D2<br>0 = PMA/PMD is not able to perform 50GBASE-PQX-D2 | RO |
| 1.1002.3 | 50GBASE-PQG-U3 | 1 = PMA/PMD is able to perform 50GBASE-PQG-U3<br>0 = PMA/PMD is not able to perform 50GBASE-PQG-U3 | RO |


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**Table 45–103a—Nx25G-EPON PMA/PMD extended ability register bit definitions *(continued)***

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.1002.2 | 50GBASE-PQG-U2 | 1 = PMA/PMD is able to perform 50GBASE-PQG-U2<br>0 = PMA/PMD is not able to perform 50GBASE-PQG-U2 | RO |
| 1.1002.1 | 50GBASE-PQG-D3 | 1 = PMA/PMD is able to perform 50GBASE-PQG-D3<br>0 = PMA/PMD is not able to perform 50GBASE-PQG-D3 | RO |
| 1.1002.0 | 50GBASE-PQG-D2 | 1 = PMA/PMD is able to perform 50GBASE-PQG-D2<br>0 = PMA/PMD is not able to perform 50GBASE-PQG-D2 | RO |

[a]RO = Read only

#### 45.2.1.134a.1 25GBASE-PQX-U3 (1.1000.15)

When read as a one, bit 1.1000.15 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.15 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.2 25GBASE-PQX-U2 (1.1000.14)

When read as a one, bit 1.1000.14 indicates that the PMA/PMD is able to support a 25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.14 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.3 25GBASE-PQX-D3 (1.1000.13)

When read as a one, bit 1.1000.13 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.13 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.4 25GBASE-PQX-D2 (1.1000.12)

When read as a one, bit 1.1000.12 indicates that the PMA/PMD is able to support a 25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.12 indicates that the PMA/PMD is not able to support a 25GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.5 25GBASE-PQG-U3 (1.1000.11)

When read as a one, bit 1.1000.11 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.11 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.6 25GBASE-PQG-U2 (1.1000.10)

When read as a one, bit 1.1000.10 indicates that the PMA/PMD is able to support a 25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.10 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-U2 PMA/PMD type.


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#### 45.2.1.134a.7 25GBASE-PQG-D3 (1.1000.9)

When read as a one, bit 1.1000.9 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.9 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.8 25GBASE-PQG-D2 (1.1000.8)

When read as a one, bit 1.1000.8 indicates that the PMA/PMD is able to support a 25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.8 indicates that the PMA/PMD is not able to support a 25GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.9 25/10GBASE-PQX-U3 (1.1000.7)

When read as a one, bit 1.1000.7 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1000.7 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.10 25/10GBASE-PQX-U2 (1.1000.6)

When read as a one, bit 1.1000.6 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1000.6 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.11 25/10GBASE-PQX-D3 (1.1000.5)

When read as a one, bit 1.1000.5 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1000.5 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.12 25/10GBASE-PQX-D2 (1.1000.4)

When read as a one, bit 1.1000.4 indicates that the PMA/PMD is able to support a 25/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1000.4 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.13 25/10GBASE-PQG-U3 (1.1000.3)

When read as a one, bit 1.1000.3 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1000.3 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.14 25/10GBASE-PQG-U2 (1.1000.2)

When read as a one, bit 1.1000.2 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1000.2 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.15 25/10GBASE-PQG-D3 (1.1000.1)

When read as a one, bit 1.1000.1 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1000.1 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D3 PMA/PMD type.


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#### 45.2.1.134a.16 25/10GBASE-PQG-D2 (1.1000.0)

When read as a one, bit 1.1000.0 indicates that the PMA/PMD is able to support a 25/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1000.0 indicates that the PMA/PMD is not able to support a 25/10GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.17 50/25GBASE-PQX-U3 (1.1001.15)

When read as a one, bit 1.1001.15 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.15 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.18 50/25GBASE-PQX-U2 (1.1001.14)

When read as a one, bit 1.1001.14 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.14 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.19 50/25GBASE-PQX-D3 (1.1001.13)

When read as a one, bit 1.1001.13 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.13 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.20 50/25GBASE-PQX-D2 (1.1001.12)

When read as a one, bit 1.1001.12 indicates that the PMA/PMD is able to support a 50/25GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.12 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.21 50/25GBASE-PQG-U3 (1.1001.11)

When read as a one, bit 1.1001.11 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.11 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.22 50/25GBASE-PQG-U2 (1.1001.10)

When read as a one, bit 1.1001.10 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.10 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.23 50/25GBASE-PQG-D3 (1.1001.9)

When read as a one, bit 1.1001.9 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.9 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.24 50/25GBASE-PQG-D2 (1.1001.8)

When read as a one, bit 1.1001.8 indicates that the PMA/PMD is able to support a 50/25GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.8 indicates that the PMA/PMD is not able to support a 50/25GBASE-PQG-D2 PMA/PMD type.


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#### 45.2.1.134a.25 50/10GBASE-PQX-U3 (1.1001.7)

When read as a one, bit 1.1001.7 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1001.7 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U3 PMA/PMD type.

#### 45.2.1.134a.26 50/10GBASE-PQX-U2 (1.1001.6)

When read as a one, bit 1.1001.6 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1001.6 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.27 50/10GBASE-PQX-D3 (1.1001.5)

When read as a one, bit 1.1001.5 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1001.5 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.28 50/10GBASE-PQX-D2 (1.1001.4)

When read as a one, bit 1.1001.4 indicates that the PMA/PMD is able to support a 50/10GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1001.4 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.29 50/10GBASE-PQG-U3 (1.1001.3)

When read as a one, bit 1.1001.3 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1001.3 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.30 50/10GBASE-PQG-U2 (1.1001.2)

When read as a one, bit 1.1001.2 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1001.2 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.31 50/10GBASE-PQG-D3 (1.1001.1)

When read as a one, bit 1.1001.1 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1001.1 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.32 50/10GBASE-PQG-D2 (1.1001.0)

When read as a one, bit 1.1001.0 indicates that the PMA/PMD is able to support a 50/10GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1001.0 indicates that the PMA/PMD is not able to support a 50/10GBASE-PQG-D2 PMA/PMD type.

#### 45.2.1.134a.33 50GBASE-PQX-U3 (1.1002.7)

When read as a one, bit 1.1002.7 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U3 PMA/PMD type. When read as a zero, bit 1.1002.7 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U3 PMA/PMD type.


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#### 45.2.1.134a.34 50GBASE-PQX-U2 (1.1002.6)

When read as a one, bit 1.1002.6 indicates that the PMA/PMD is able to support a 50GBASE-PQX-U2 PMA/PMD type. When read as a zero, bit 1.1002.6 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-U2 PMA/PMD type.

#### 45.2.1.134a.35 50GBASE-PQX-D3 (1.1002.5)

When read as a one, bit 1.1002.5 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D3 PMA/PMD type. When read as a zero, bit 1.1002.5 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D3 PMA/PMD type.

#### 45.2.1.134a.36 50GBASE-PQX-D2 (1.1002.4)

When read as a one, bit 1.1002.4 indicates that the PMA/PMD is able to support a 50GBASE-PQX-D2 PMA/PMD type. When read as a zero, bit 1.1002.4 indicates that the PMA/PMD is not able to support a 50GBASE-PQX-D2 PMA/PMD type.

#### 45.2.1.134a.37 50GBASE-PQG-U3 (1.1002.3)

When read as a one, bit 1.1002.3 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U3 PMA/PMD type. When read as a zero, bit 1.1002.3 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U3 PMA/PMD type.

#### 45.2.1.134a.38 50GBASE-PQG-U2 (1.1002.2)

When read as a one, bit 1.1002.2 indicates that the PMA/PMD is able to support a 50GBASE-PQG-U2 PMA/PMD type. When read as a zero, bit 1.1002.2 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-U2 PMA/PMD type.

#### 45.2.1.134a.39 50GBASE-PQG-D3 (1.1002.1)

When read as a one, bit 1.1002.1 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D3 PMA/PMD type. When read as a zero, bit 1.1002.1 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D3 PMA/PMD type.

#### 45.2.1.134a.40 50GBASE-PQG-D2 (1.1002.0)

When read as a one, bit 1.1002.0 indicates that the PMA/PMD is able to support a 50GBASE-PQG-D2 PMA/PMD type. When read as a zero, bit 1.1002.0 indicates that the PMA/PMD is not able to support a 50GBASE-PQG-D2 PMA/PMD type.


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### 45.2.3 PCS registers

***Change the rows for registers 3.76 through 3.199 in Table 45–176 as follows (unchanged rows not shown):***

**Table 45–176—PCS registers**

| Register address | Register name | Subclause |
|---|---|---|
| … | | |
| 3.76, 3.77 | ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter | 45.2.3.41 |
| 3.78, 3.79 | ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter | 45.2.3.42 |
| 3.80 | 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval~~timer~~ control | 45.2.3.43 |
| 3.81 | 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status | 45.2.3.44 |
| 3.82 | 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control | 45.2.3.45 |
| 3.83 through 3.134 | Nx25G-EPON synchronization pattern | 45.2.3.45a |
| ~~3.83~~3.135 through 3.199 | Reserved | |
| … | | |

#### 45.2.3.1 PCS control 1 register (Register 3.0)

***Change the row for bits 3.0.5:2 in Table 45–177 (as modified IEEE Std 802.cd-2018) as follows (unchanged rows not shown):***

**Table 45–177—PCS control 1 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| … | | | |
| 3.0.5:2 | Speed selection | 5 4 3 2<br>1 1 x x = Reserved<br>1 0 1 1 = ~~Reserved~~25/10 Gb/s<br>1 0 1 0 = 400 Gb/s<br>1 0 0 1 = 200 Gb/s<br>1 0 0 0 = 5 Gb/s<br>0 1 1 1 = 2.5 Gb/s<br>0 1 1 0 = 50 Gb/s<br>0 1 0 1 = 25 Gb/s<br>0 1 0 0 = 100 Gb/s<br>0 0 1 1 = 40 Gb/s<br>0 0 1 0 = 10/1 Gb/s<br>0 0 0 1 = 10PASS-TS/2BASE-TL<br>0 0 0 0 = 10 Gb/s | R/W |
| … | | | |

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing


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### 45.2.3.6 PCS control 2 register (Register 3.7)

***Change Table 45–180 (as modified by IEEE Std 802.3cb-2018 and IEEE Std 802.cd-2018) as follows (unchanged rows not shown):***

**Table 45–180—PCS control 2 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.7.15:~~4~~5 | Reserved | Value always 0 | RO |
| 3.7.~~3~~4:0 | PCS type selection | ~~4~~ 3 2 1 0<br>1 1 x x x = reserved<br>1 0 1 x x = reserved<br>1 0 0 1 1 = Select 25GBASE-PQ PCS type<br>1 0 0 1 0 = Select 25/10GBASE-PQ PCS type<br>1 0 0 0 1 = Select 25GBASE-PQ PCS type, Tx only<br>1 0 0 0 0 = Select 25GBASE-PQ PCS type, Rx only<br>0 1 1 1 1 = Select 5GBASE-R PCS type<br>0 1 1 1 0 = Select 2.5GBASE-X PCS type<br>0 1 1 0 1 = Select 400GBASE-R PCS type<br>0 1 1 0 0 = Select 200GBASE-R PCS type<br>0 1 0 1 1 = Select 5GBASE-T PCS type<br>0 1 0 1 0 = Select 2.5GBASE-T PCS type<br>0 1 0 0 1 = Select 25GBASE-T PCS type<br>0 1 0 0 0 = Select 50GBASE-R PCS type<br>0 0 1 1 1 = Select 25GBASE-R PCS type<br>0 0 1 1 0 = Select 40GBASE-T PCS type<br>0 0 1 0 1 = Select 100GBASE-R PCS type<br>0 0 1 0 0 = Select 40GBASE-R PCS type<br>0 0 0 1 1 = Select 10GBASE-T PCS type<br>0 0 0 1 0 = Select 10GBASE-W PCS type<br>0 0 0 0 1 = Select 10GBASE-X PCS type<br>0 0 0 0 0 = Select 10GBASE-R PCS type | R/W |

[a]RO = Read only, R/W = Read/Write

***Change the title and text of 45.2.3.6.1 as follows:***

### 45.2.3.6.1 PCS type selection (3.7.~~3~~4:0)

The PCS type shall be selected using bits ~~3~~4 through 0. The PCS type abilities of the PCS are advertised in bits 3.8.9~~:0, 3.8.7:0,~~ and 3.9.~~1~~7:0. A PCS shall ignore writes to the PCS type selection bits that select PCS types it has not advertised in the PCS status 2 register or the PCS status 3 register. It is the responsibility of the STA entity to ensure that mutually acceptable MMD types are applied consistently across all the MMDs on a particular PHY. The PCS type selection defaults to a supported ability.

### 45.2.3.8 PCS status 3 register (Register 3.9)

***Change the row for bits 3.9.15:4 in Table 45–182 (as modified by IEEE Std 802.3cb-2018) as follows (unchanged rows not shown):***


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**Table 45–182—PCS status 3 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.9.15:~~4~~8 | Reserved | Value always 0 | RO |
| 3.9.7 | 25GBASE-PQ capable | 1 = PCS is able to support 25GBASE-PQ PCS type<br>0 = PCS is not able to support 25GBASE-PQ PCS type | RO |
| 3.9.6 | 25/10GBASE-PQ capable | 1 = PCS is able to support25/10GBASE-PQ PCS type<br>0 = PCS is not able to support 25/10GBASE-PQ PCS type | RO |
| 3.9.5 | 25GBASE-PQ Rx only capable | 1 = PCS is able to support 25GBASE-PQ Rx only PCS type<br>0 = PCS is not able to support 25GBASE-PQ Rx only PCS type | RO |
| 3.9.4 | 25GBASE-PQ Tx only capable | 1 = PCS is able to support 25GBASE-PQ Tx only PCS type<br>0 = PCS is not able to support 25GBASE-PQ Tx only PCS type | RO |
| … | | | |

[a]RO = Read only

***Insert 45.2.3.8.aa through 45.2.3.8.ad (before 45.2.3.8.a as inserted by IEEE Std 802.3cb-2018) as follows:***

#### 45.2.3.8.aa 25GBASE-PQ capable (3.9.7)

When read as a one, bit 3.9.7 indicates that the PCS is able to support the 25GBASE-PQ PCS type. When read as a zero, bit 3.9.7 indicates that the PCS is not able to support the 25GBASE-PQ PCS type.

#### 45.2.3.8.ab 25/10GBASE-PQ capable (3.9.6)

When read as a one, bit 3.9.6 indicates that the PCS is able to support the 25/10GBASE-PQ PCS type. When read as a zero, bit 3.9.6 indicates that the PCS is not able to support the 25/10GBASE-PQ PCS type.

#### 45.2.3.8.ac 25GBASE-PQ Rx only capable (3.9.5)

When read as a one, bit 3.9.5 indicates that the PCS is able to support the 25GBASE-PQ Rx only PCS type. When read as a zero, bit 3.9.5 indicates that the PCS is not able to support the 25GBASE-PQ Rx only PCS type.

#### 45.2.3.8.ad 25GBASE-PQ Tx only capable (3.9.4)

When read as a one, bit 3.9.4 indicates that the PCS is able to support the 25GBASE-PQ Tx only PCS type. When read as a zero, bit 3.9.4 indicates that the PCS is not able to support the 25GBASE-PQ Tx only PCS type.

***Change the title, text and tables for 45.2.3.41 through 45.2.3.45 as follows:***

#### 45.2.3.41 ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter (Register 3.76, 3.77)

The assignment of bits in the ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter register is shown in Table 45–213. See 76.3.3.3.2 for a definition of ~~this~~the


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10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

**Table 45–213—~~10GBASE-PR~~10G-EPON and Nx25G-EPON corrected FEC codewords counter register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.76.15:0 | corrected FEC codewords lower | corrected_FEC_codewords_counter[15:0] | RO, MW, NR |
| 3.77.15:0 | corrected FEC codewords upper | corrected_FEC_codewords_counter[31:16] | RO, MW, NR |

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

### 45.2.3.42 ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter (Register 3.78, 3.79)

The assignment of bits in the ~~10/1GBASE-PRX and 10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register is shown in Table 45–214. See 76.3.3.3.2 for a definition of ~~this~~the 10G-EPON counters and 142.3.5.2 for the definition of the Nx25-EPON counters. These bits shall be reset to all zeros when the register is read by the management function or upon PCS reset. These bits shall be held at all ones in the case of overflow.

**Table 45–214—~~10GBASE-PR~~10G-EPON and Nx25G-EPON uncorrected FEC codewords counter register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.78.15:0 | uncorrected FEC codewords lower | uncorrected_FEC_codewords_counter[15:0] | RO, MW, NR |
| 3.79.15:0 | uncorrected FEC codewords lower | uncorrected_FEC_codewords_counter[32:16] | RO, MW, NR |

[a]RO = Read only, MW = Multi-word, NR = Non Roll-over

### 45.2.3.43 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register (Register 3.80)

The assignment of bits in the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register is shown in Table 45–215. This register is defined only when 10GBASE-PR, ~~or~~ 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.


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**Table 45–215—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor interval ~~timer~~ control register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.80.15:8 | Reserved | Value always 0 | RO |
| 3.80.7:0 | ~~10G~~ EPON BER monitor ~~timer~~ interval | For 10GBASE-PR and 10/1GBASE-PRX: Duration (in units of 5 microseconds) of the timer used by the ~~10G EPON~~ BER monitor function. Default value is 25 (i.e., 125 microseconds). A value of zero indicates that the BER monitor function is disabled.<br>For Nx25G-EPON: QC-LDPC codeword count (in units of 16 codewords) of the monitoring interval used by the BER Monitor function. Default value is 12 (i.e., 192 codewords). | R/W |

[a]RO = Read only, R/W = Read/Write

### 45.2.3.44 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status (Register 3.81)

The assignment of bits in the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register is shown in Table 45–216. This register is defined only when 10GBASE-PR ~~or~~, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported.

**Table 45–216—10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor status register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.81.15:2 | Reserved | Value always 0 | RO |
| 3.81.1 | Latched high BER | 10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS:<br>1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reported a high BER.<br>0 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ did not report a high BER. | RO, LH |
| 3.81.0 | high BER | 10GBASE-PR, 10/1GBASE-PRX, or Nx25G-EPON PCS:<br>1 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ reporting a high BER.<br>0 = ~~10GBASE-PR or 10/1GBASE-PRX PCS~~ not reporting a high BER. | RO |

[a]RO Read only, LH = Latching high

#### 45.2.3.44.1 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS high BER (3.81.0)

In the 10GBASE-PR ~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.0 indicates that the receiver is detecting a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.0 indicates that the receiver is detecting a BER lower than the configurable threshold (low BER state). This bit mirrors the state of the hi_ber variable, defined in 76.3.3.4 for 10GBASE-PR and, 10/1GBASE-PRX, and the HiBer variable in 142.3.5.2 for Nx25G-EPON.


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### 45.2.3.44.2 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS latched high BER (3.81.1)

In the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON PCS, when read as a one, bit 3.81.1 indicates that the receiver detected a BER greater than the configurable threshold (high BER state). When read as a zero, bit 3.81.1 indicates that the receiver detected BER lower than the configurable threshold (low BER state).

This bit is a latching high version of the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON high BER status bit (3.81.0).

### 45.2.3.45 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control (Register 3.82)

The assignment of bits in the 10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register is shown in Table 45–217. This register is defined only when 10GBASE-PR~~or~~, 10/1GBASE-PRX, or Nx25G-EPON ONU capability is supported. The 10G-EPON BER monitor is described in 76.3.3.4. The Nx25G-EPON QC-LDPC BER Monitor is described in 142.3.5.6.

**Table 45–217—10GBASE-PR~~and~~, 10/1GBASE-PRX, and Nx25G-EPON BER monitor threshold control register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.82.15:0 | ~~10G-~~EPON BER monitor threshold | For 10G-EPON: n~~N~~umber of sync header errors within a timer interval that triggers a high BER condition for the ~~10G-EPON~~ BER monitor function. Default value is 1600. A value of zero indicates that the BER monitor function is disabled.<br>For Nx25G-EPON: number of invalid QC-LDPC codeword parity checks within a BER monitor interval that triggers a high BER condition for the BER Monitor function. Default value is 18. A value of zero indicates that the BER Monitor function is disabled. | R/W |

[a]R/W = Read/Write

***Insert 45.2.3.45a and subclauses after 45.2.3.45 as follows:***

### 45.2.3.45a Nx25G-EPON synchronization pattern registers (Registers 3.83 through 3.134)

The assignment of bits in registers 3.83 through 3.134 is shown in Table 45–217a. The Nx25G-EPON synchronization pattern (see 142.1.3 and 144.3.6.7) is used in the upstream data transmissions to facilitate the OLT in locking to the incoming data burst.

**Table 45–217a—Nx25G-EPON synchronization pattern registers bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.83.15:6 | Reserved | Value always 0 | RO |
| 3.83.5 | SP3 bit 257 | The MSB of the 257-bit SP3. | R/W |
| 3.83.4 | SP3 balanced | Balance setting for SP3. | R/W |
| 3.83.3 | SP2 bit 257 | The MSB of the 257-bit SP2. | R/W |


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**Table 45–217a—Nx25G-EPON synchronization pattern registers bit definitions *(continued)***

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 3.83.2 | SP2 balanced | Balance setting for SP2. | R/W |
| 3.83.1 | SP1 bit 257 | The MSB of the 257-bit SP1. | R/W |
| 3.83.0 | SP1 balanced | Balance setting for SP1. | R/W |
| 3.99.15 through 3.84.0 | SP1 pattern | The lower 256 bits of SP1. Bit 0 is stored in 3.84.0, and bit 255 is stored in 3.99.15. | R/W |
| 3.100.15:0 | SP1 length | The number of times SP1 is to be repeated. | R/W |
| 3.116.15 through 3.101.0 | SP2 pattern | The lower 256 bits of SP2. Bit 0 is stored in 3.101.0, and bit 255 is stored in 3.116.15. | R/W |
| 3.117.15:0 | SP2 length | The number of times SP2 is to be repeated. | R/W |
| 3.133.15 through 3.118.0 | SP3 pattern | The lower 256 bits of SP3. Bit 0 is stored in 3.118.0, and bit 255 is stored in 3.133.15. | R/W |
| 3.134.15:0 | SP3 length | The number of times SP3 is to be repeated. | R/W |

[a]RO = Read only, R/W = Read/Write

#### 45.2.3.45a.1 SP3 bit 257 (3.83.5)

In the Nx25G-EPON PCS, bit 3.83.5 indicates the value to be used for the 257th bit of SP3. See 142.1.3 and 144.3.6.7 for additional details.

#### 45.2.3.45a.2 SP3 balanced (3.83.4)

In the Nx25G-EPON PCS, bit 3.83.4 indicates that repeating SP3 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP3 is to remain unbalanced, i.e., SP3 is always transmitted using the values from 3.83.5 and 3.118.0 through 3.133.15. When this bit is set to a one SP3 is to be balanced, i.e., each 257-bit block of SP3 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.

#### 45.2.3.45a.3 SP2 bit 257 (3.83.3)

In the Nx25G-EPON PCS, bit 3.83.3 indicates the value to be used for the 257th bit of SP2. See 142.1.3 and 144.3.6.7 for additional details.

#### 45.2.3.45a.4 SP2 balanced (3.83.2)

In the Nx25G-EPON PCS, bit 3.83.2 indicates that repeating SP2 synchronization patterns are to have a balanced number of one and zero bits transmitted. When this bit is set to a zero then SP2 is to remain unbalanced, i.e., SP2 is always transmitted using the values from 3.83.3 and 3.101.0 through 3.116.15. When this bit is set to a one SP2 is to be balanced, i.e., each 257-bit block of SP2 (starting with the second block) is an inversion of the preceding block. See 142.1.3 and 144.3.6.7 for additional details.


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