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IEEE Standard for Heterogenous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Contruction

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Abstract: Enabling the construction of high-performance, scalable, modular, parallel systems with low system integration cost is discussed. Complementary use of physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating at speeds of 10–200 Mb/s and at 1 Gb/s in copper and optic technologies, is described.
Keywords:low control, encoding schemes, OMI/HIC, packet routing, parallelism, point-to-point serial scalable interconnect, protocols, routing fabric, serial links, serialization, silicon integration, switch chip, transaction layer, wormhole routing

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Introduction

[This introduction is not part of IEEE Std 1355-1995, IEEE Standard for Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction).]

The construction of high-performance systems with parallel communications, parallel processing, and/or parallel I/O demands a fast, low-cost, low-latency interconnect. It must be fast and low-latency, otherwise it will be the limiting factor in system performance; and it must be low-cost, or it will dominate the system cost. It must also scale well in both performance and cost relative to the system size, otherwise highly parallel systems will be limited in performance or too expensive. Existing standards do not meet these criteria, because they are designed for communication over long distances (which incurs high costs), or because they aim at the extreme of currently achievable performance (which again increases costs), or because they are based on a restricted model such as a bus, which limits overall performance and scalability. A detailed rationale for this standard is given in annex D.

This standard has been developed to complement recent technical developments of highly integrated, low power interconnect technology implemented in high volume commodity VLSI processes, and to exploit the simplifications in encodings and protocols resulting from the use of relatively reliable media over relatively short distances. Aspects of the baseline for this standard have their origins in work on parallel systems, which has taken place in a number of ESPRIT projects. In particular, the routing strategy was established in the PUMA project, and the DS-Links were developed partially in the GP MIMD project. Work at interconnect for high performance mainframe computers at Bull led to the development of the gigabit link technology implemented in Bi-CMOS and CMOS processes. More recently, these developments, together with corresponding optical technology, have been brought together in the OMI/HIC Project (Open Microprocessor Systems Initiative—High Performance Heterogeneous Interconnect—ESPRIT 7252).

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IEEE Standard for Heterogeneous InterConnect (HIC) (Low-Cost, Low-Latency Scalable Serial Interconnect for Parallel System Construction)

1. Overview

1.1 Scope

The scope of this standard is the physical connectors and cables, electrical properties, and logical protocols for point-to-point serial scalable interconnect, operating speeds of 10–200 Mb/s and at 1 Gb/s in copper and optic technologies [as developed in Open Microprocessor Systems Initiative/Heterogeneous InterConnect Project (OMI/HIC)].

1.2 Purpose

The purpose of this standard is to enable high performance, scalable, modular, parallel systems to be constructed with low system integration cost; to support communications systems fabric; to provide a transparent implementation of a range of high level protocols [communications (e.g., ATM), message passing, shared memory transactions, etc.], and to support links between heterogeneous systems.

2. References

This standard shall be used in conjunction with the following publications:

CISPR 22: 1993, Limits and methods of measurement of radio disturbance characteristics of information technology equipment. [1]

DIN-VDE 0472-517, Testing of cables, wires cords; crosstalk attenuation.[2]

[1]CISPR documents are available from the International Electrotechnical Commission, 3 rue de Varembé, Case Postale 131, CH 1211, Genève 20, Switzerland/Suisse. CISPR documents are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.
[2]DIN documents are available from the Deutsches Institut Füer Normung DIN, Burggrafenstrasse 6, Posffach 1007, 12623 Berlin 30, Germany.

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IEC 48B (Germany) 141, Time domain reflectrometry.

IEC 352-5: 1995, Solderless connections—Part 5.: Solderless press-in connections—General requirements, test methods and practical guidance.[3]

IEC 512-2:1985, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 2.: General examination, electrical continuity and contact resistance tests, insulation tests and voltage stress tests.

IEC 512-3:1976, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 3.: Current carrying capacity tests.

IEC 512-4 :1976, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 4.: Dynamic stress tests.

IEC 512-5 : 1992, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 5.: Impact tests (free components), static load tests (fixed components), endurance tests and overload tests.

IEC 512-6 : 1984, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 6.: Climatic tests and soldering tests.

IEC 512-7 : 1993, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 7.: Mechanical operating tests and sealing tests.

IEC 512-8 : 1993, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 8.: Connector tests (mechanical) and mechanical tests on contacts and terminations.

IEC 512-9 : 1992, Electromechanical components for electronic equipment; basic testing procedures and measuring methods—Part 9.: Miscellaneous tests.

IEC 793-1 :1992, Optical fibres—Part 1.: Generic specifications.

IEC 793-2 :1992, Optical fibres—Part 2.: Product specifications.

IEC 801-4 : 1988, Electromagnetic compatibility for industrial-process measurement and control equipment—Part 4.: Electrical fast transient/burst requirements (to be replaced by future IEC 1000-4-4).

IEC 825-1 : 1993, Safety of laser products—Part 1.: Equipment classification, requirements and user's guide.

IEC 825-2 : 1993, Safety of laser products—Part 2.: Safety of optical fiber communication systems.

IEC 917 : 1988, Modular order for the development of mechanical structures for electronic equipment practices.

IEC 1076-4-101 : 1995, Connectors with assessed quality for use in dc and low frequency analogue applications and in digital applications with high speed data rates. Part 4.: Printed board connectors—Section 101: Sectional specification.

IEC 1076-4-107 : 1995, Two part connectors for basic grid of 2.0 mm, with free connectors for nonaccessible insulation displacement termination.

[3]IEC publications are available from the IEC Sales Department, Case Postale 131, 3, rue de Varembé, CH-1211, Genve 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, II West 42nd Street, 13th Floor, New York, NY 10036, USA.

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IEC 1300 —, Fibre optic interconnecting devices and passive components—Basic test and measurement procedures.

IEC 1196-1 :1995, Radio-frequency cables—Specifications—Part 1.: Generic Specification, General Definitions, Requirements and Test Methods.

IEC 1196-2, Radio-frequency cables—Specifications—Semi-rigid radio-frequency and coaxial cables with polytetrafluoroethylene (PTFE) insulation—Sectional specification.

IEC 1754-6 :1995 [CDV document 86 B (Secretariat) 473], Fibre optic connector interfaces—Part 6.: Type MU connector family.

IEEE Std 100-1992 , The New IEEE Standard Dictionary of Electrical and Electronics Terms (ANSI).[4]

IEEE Std 1301.3-1992, IEEE Standard for Metric Practice for Microcomputers—Convection Cooled with 2.5 mm Connector (ANSI).

QC 210000: 1987, Connectors for optical fibres and cables. Part 1.: Generic specification.[5]

3. Definitions

3.1 General

Common terms are as defined in IEEE Std 100-1992. [6] The terms defined in this clause are specific to this standard.

The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform with the standard and from which no deviation is permitted.

The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited.

The word *may* is used to indicate a course of action:permissible within the limits of the standard.

3.2 Glossary

3.2.1 BER: *See:* **bit error rate.**

3.2.2 bit error rate: The ratio of errors to the total number of bits being sent in a data transmission from one location to another.

3.2.3 box: A mechanical unit that contains links; the links may either remain inside the box, connecting internal devices, or may leave the box in order to connect internal devices to external ones. A box is assumed to be an EMC compliant enclosure and to operate under a single electrical environment.

[4]IEEE publicatons are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA.
[5]*This publication also bears the number IEC 874-1*. QC 210000 is available from International Electrotechnical Commission, IEC publications are available from IEC Sales Department, Case Postale 131, 3, rue de Varembé, CH-1211, Genève 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.
[6]Information on references can be found in clause 2.

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3.2.4 character: A group of consecutive bits used to represent control or data information. Characters are of two types: normal characters (N_chars) or link characters (L_chars). *See also*: **control character, data character, link character, normal character.**

3.2.5 character layer: The layer of the protocol stack that specifies the representation of characters in terms of groups of consecutive bits. The character layer provides the service to the higher layers of the transmission of a continuous sequence of characters on a link.

3.2.6 coding: The translation from the original set of bits (character) to a new set of bits (coded character) suitable for serial transmission. *See also*: **decoding**

3.2.7 control character: A character used for signaling purposes by the exchange, packet or transaction layers of the stack. Both N_chars and L_chars are used as control characters. *See also:* **link character; normal character.**

3.2.8 data character: A character used for packet payload or packet header. A data character represents one of the values of a byte, i.e., 0—255 (decimal). Only N_chars are used as data characters. *See also:* **link character; normal character.**

3.2.9 decoding: The translation from the coded set of bits (coded character) to the original set of bits (character). *See also:* **coding.**

3.2.10 deserialization: The assembly of a coded character from the sequence of serial bits. *See also:* **serialization.**

3.2.11 destination: One or more destination_identifiers, identifying the destination node(s) to which the packet is to be transmitted. *See also:* **destination_identifier.**

3.2.12 destination_identifier (dest_id): An implementation dependent identity of a destination node for a packet.

3.2.13 destination node: The terminal node(s) that is/are to receive a particular packet. *See also:* **node.**

3.2.14 digital sum variation: The difference between the number of logical ls and the logical Os transmitted by a link output since commencing operation. *See also:* **running disparity.**

3.2.15 disparity: The difference between the number of logical 1s and logical 0s in a character. A positive or negative disparity indicates an excess of 1s or 0s, respectively.

3.2.16 end_of_packet marker: A control character that indicates the end of a packet. *See also:* **packet.**

3.2.17 exchange layer: The exchange layer describes the procedure of the node-to-node exchange of characters to ensure the proper functioning of the link. The exchange layer provides the service to the higher layers of the transmission of an indefinite sequence of N_chars.

3.2.18 fabric: A device or a collection of devices that provides a general routing capability, constructed from one or more switches using links. *See also:* **link; switch.**

3.2.19 flow control character (FCC): A control character transmitted on a link in the opposite direction to data flow for each direction of data flow, i.e., to the transmitter of data from the receiver, indicating that the receiver has space reserved to receive a further F N_chars. The value of F is specified separately for each technology in this standard.

3.2.20 functional: A link interface becomes functional when the start-up procedure has successfully completed and the link interface is ready to transmit data.

3.2.21 link: A means of communicating digital information bidirectionally in serial format between two devices or subsystems. A link comprises two link interfaces connected by an appropriate medium (or media, for connections between boards or cabinets), such that the link output of each interface is connected to the link input of the other.

3.2.22 link cable: The physical medium connecting two link interfaces, comprising of two or more electrical or optical cables.

3.2.23 link character (or L_char): Control characters that are used on a link in order to ensure flow control and the proper functioning of the link. *See also:* **normal character.**

3.2.24 link input: A connection point for receiving signals. *See also:* **link interface.**

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3.2.25 link interface (or port): A connection point comprising a link input and a link output and implementing one of the relevant conformance subsets defined in 10.2. *See also:* **link.**

3.2.26 link output: A connection point for transmitting signals. *See also:* **link interface.**

3.2.27 network: Any set of devices or subsystems connected by links joining (directly or indirectly) a set of terminal nodes.

3.2.28 node: A device or subsystem having one or more link interfaces. A node may be a terminal node (q.v.). A node may perform a muting function, muting packets between its node interfaces according to the information in the destination field of the packet.

3.2.29 node interface: A link interface on a switch. *See also:* **link interface; switch.**

3.2.30 normal character (or N_char): N_chars represent, at the minimum, the 256 values of a byte (i.e., all the data characters) plus a control character representing an end_of_packet marker.

3.2.31 packet: A sequence of N_chars with a specific order and format. A packet consists of a destination followed by a payload. A packet is delimited by an end_of_packet marker. *See also:* **destination; payload.**

3.2.32 packet layer: The layer of the protocol concerned with end-to-end transmission of information, possibly through a number of intermediate routers. It is at the packet layer that the muting decisions are taken.

3.2.33 payload: The data (a message, a memory access request, an acknowledgment, etc.) that is to be transferred from the source node to the destination node. It has a specific format, defined in the transaction layer. Note that a payload may be null. *See also:* **packet.**

3.2.34 physical medium: *See:* **transmission medium.**

3.2.35 port: *See:* **link interface.**

3.2.36 routing function: Inside a switch, this is function that determines to which numbered node interface a packet is to be sent, based on the information contain in the packet destination. *See also:* **switch.**

3.2.37 run length: The maximum number of succesive bits of the same value that can occur in the coded 3.2.37 run length: The maximum number of successive bits of the same bit stream.

3.2.38 running disparity: The cumulative sum of the disparities of characters transmitted from the start of operation of the link up to the present time. A link has two running disparities, one for each direction.

3.2.39 serialization: The process of transmitting coded characters one bit at a time. *See also:* **deserialization.**

3.2.40 signal: A measurable quantity (e.g., a voltage) that varies in time in order to transmit information. A signal propagates along a wire or an optic fiber. It is interpreted as a sequence of bits that is grouped into a sequence of characters by the character layer of the protocol stack. Signals are generated by a link output and are absorbed by a link input.

3.2.41 signal layer: The layer of the protocol stack at which signals are specified.

3.2.42 sink: A consumer of normal characters at a link interface. *See also:* **normal character.**

3.2.43 source: A generator of normal characters at a link interface. *See also:* **normal character.**

3.2.44 source node: A terminal node that originates data. *See also:* **destination node**

3.2.45 switch: A routing device (for example, a box or board) providing a set of numbered node interfaces, constructed from one or more switch chips (or by other methods). *See also:* **fabric, node interface, switch chip.**

3.2.46 switch chip: A VLSI integrated circuit with two or more link interfaces, between which it provides packet routing. *See also:* **link; switch.**

3.2.47 terminal node: A node with one or more link interfaces that are used to originate or consume data across an interconnect complying with this standard. *See also:* **source; sink.**

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3.2.48 transaction: A sequence of packets sent between two or more terminal nodes to perform some function. *See also:* **transaction layer.**

3.2.49 transaction layer: The layer above the packet layer for use by applications. It is unspecified in this standard. *See also:* **transaction.**

3.2.50 transmission medium: A means of transporting electrical or optical signals. *See also:* **signal.**

4. Physical media and logical layers

This standard defines a set of rules for information exchange (the logical layers) together with the ways in that it shall be implemented on a variety of physical media. The logical layers are defined as a protocol stack. Each layer of the protocol stack defines representations (information formats) in terms of the immediately lower layer, together with rules (protocols) for the exchange of these representations.

The use of the physical media and logical layers is illustrated in figure 4-1. The physical medium and the signal, character and exchange layers are concerned with point-to-point communication between adjacent nodes, while the packet layer provides end-to-end communication between terminal nodes.

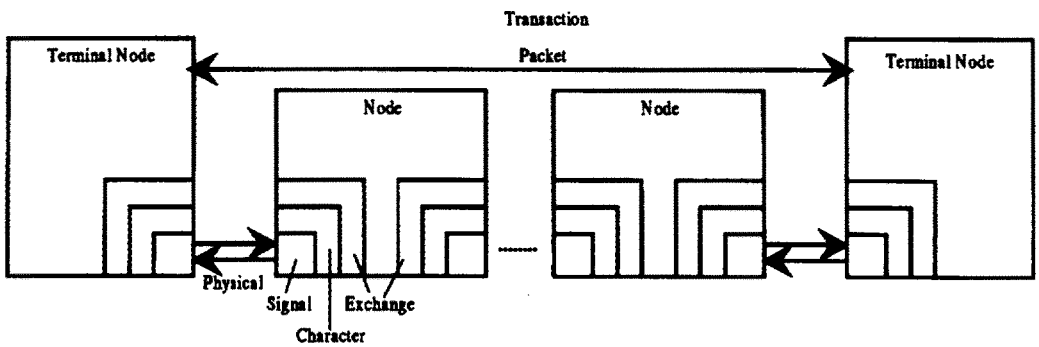

Figure 4-1 —Protocol stack between nodes

4.1 Physical media

For electrical links, the physical characteristics include the specification of

a) Circuit board physical characteristics
b) Connectors and contacts
c) Cables
d) Shielding requirements
e) Line impedance
f) Crosstalk
g) Electromagnetic emission
h) ESD susceptibility

For optical links, the physical characteristics include the specification of

— Optical transceiver properties
— Optical connectors
— Optical fiber

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4.2 Logical layers

4.2.1 Layer 0: signal layer

4.2.1.1 General description

For electrical links, the signal layer includes the specification of

a) Line signal levels and rates
b) Power budget, from which transmission distance may be calculated, taking into account the loss from the cables and connectors
c) Noise margins

For optical links, the signal layer includes the specification of

— Spectral center wavelength, aperture
— Optical power budget

It is important to note that there is a difference between signals and bits. Signals are the values of a measurable quantity (e.g., voltage levels) that are on the transmission line; bits are the logical ls and Os that the signals represent. The measurable quantities vary both in nature and in value depending on the implementation (CMOS, ECL, CML, light pulses on a fiber optic cable, etc.).

The signals may have various properties, such as limited running disparity, limited run length,and/or dc balance, over a period of time.

4.2.2 Layer 1: character layer

4.2.2.1 Definition of character

Bits are transmitted in groups called characters. The character layer provides the service to the higher layers of the transmission of a continuous sequence of characters on a link.

4.2.2.2 General description

Characters are used by the higher layers of the protocol to communicate both data information and control information. The number and representations of the various control characters and the representations of the 256 possible data values varies according to the different types of links specified in this standard.

4.2.3 Layer 2: exchange layer

4.2.3.1 Definition of the exchange layer

A link is the means of communicating digital information bidirectionally in serial format between two very large scale integration (VLSI) devices. A link comprises two link interfaces connected by an appropriate medium (or media, for connections between boards or cabinets), such that the link output of each link interface is connected to the link input of the other.

The exchange layer describes the procedure of the node-to-node exchange of characters to ensure the proper functioning of the link.

4.2.3.2 General description

Two types of character are defined: link character (L_char) and normal character (N_char).

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a) L_chars: L_chars are used on a node-to-node link in order to ensure flow control and the proper functioning of the link.
b) N_chars: N_chars represent, at the minimum, the 256 values of a byte plus an end_of_packet marker. The exchange layer provides the service to the higher layers of the transmission of an indefinite sequence of N_chars. It is specified in such a way as to ensure that N_chars are not lost due to limitations of resources (e.g., lack of available buffer space).

L_chars may be arbitrarily interleaved with N_ehars on the link as required by the exchange layer.

Note that in the text of this standard the data values of a byte (0 to 255) are referred to as data characters, and all the other used characters (i.e., all L_chars and the remainder of the N_chars) as control characters.

Consider two connected nodes, NODE_A and NODE_B (see figure 4-2). Each node uses a link interface or port (LINK_INTERFACE_A and LINK_INTERFACE_B respectively) in order to communicate with the other node. Note that a node may have more than one link interface. Each link interface is divided into two parts: a transmitter and a receiver, referred to as transmitter_A and receiver_A for NODE_A and transmitter_B and receiver_B for NODE_B.

Each link interface has a N_char source (SOURCE_A and SOURCE_B) that supply Nchars to transmitter_A and transmitter_B respectively and a N_char sink (SINK_A and SINK_B) that accept data from receiver_A and receiver_B respectively.

Exchange layer information generated and sent, for example, by transmitter_A are received and filtered by the receiver_B and passed directly to transmitter_B (and vice-versa). L_chars shall not be generated by the source nor written into the sink.

4.2.3.3 Flow control

The N_char sink associated with a link interface has a maximum capacity, defined by the physical implementation. N_chars are written into the sink by the receiver as it receives them at the link interface, and are read from the sink by the application using the link. In order to prevent sink overrun a flow control mechanism shall be implemented.

The source (at the other end of the link) maintains a “credit” associated with the receiving link interface that indicates how many N_chars the source can transmit over the link without overrunning the sink at the receiving end. For every N_char that the source sends, it shall decrement the credit by one. When the credit reaches zero, the source shall not send any further N_chars, but it may continue to send L_chars. The credit maintained by the source shall be increased by a block value (sometimes referred to as a “flit”) of F characters when the source receives a Flow Control Character (FCC) from the opposite receiver. If this happens when the credit was zero (which will have inhibited the transmission of N_chars), then the source may recommence transmitting N_chars. An implementation may restrict the amount of credit that a source can record. If a FCC is received when this credit has its maximum value, the FCC may be discarded (ignored) without affecting the operation of the link. A source shall be able to record at least F N_chars of credit.

The initial value of the credit shall be O. The block size (value of F) is defined as a function of the technology used.

The sink should send a FCC to the source when it has the space to receive F N_chars. Each time the sink authorizes the sending of a FCC it shall reserve the space corresponding to F N_chars. While the sink has unreserved space available it should send FCCs until all its space associated with the link interface is reserved. One of the first actions of each sink after the link has been started from a reset condition should therefore be to send the number of FCCs corresponding to its unreserved space.

Using the flow control mechanism described above, there exists a theoretical maximum line length over which “continuous transmission” can be obtained in the case where every N_char written into the sink is immediately read out of the sink by the receiving application. This maximum length is determined by the size of the sink (which determines the number of PCCs that the receiver sends to the transmitter after the link has been started from a reset

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condition and thus the initial transmitter credit) and a number of implementation-dependent parameters. This is detailed in annex H.

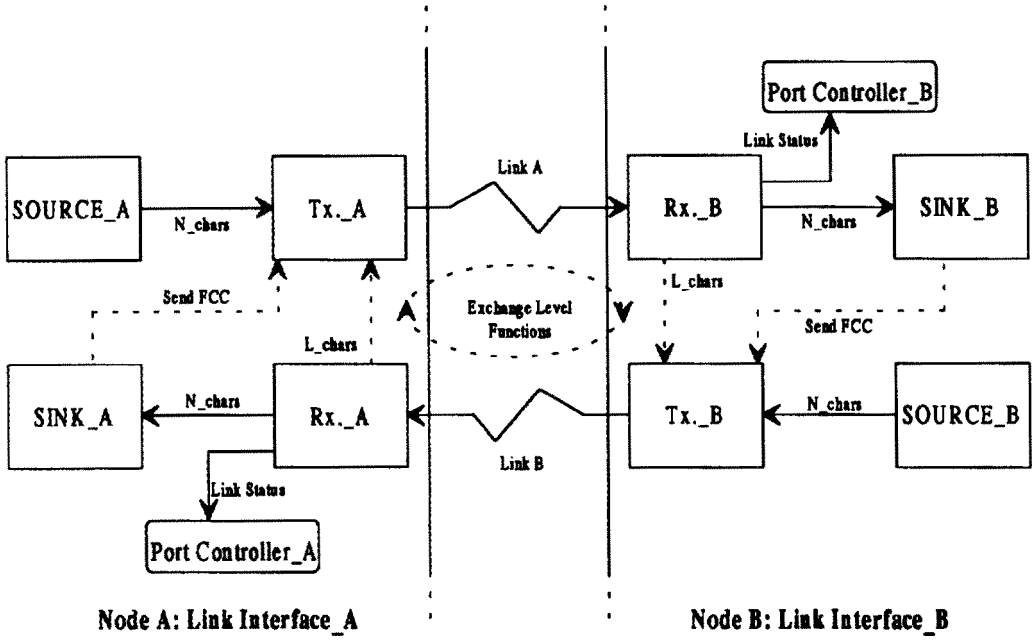

Figure 4-2 —Exchange layer

Exchange layer flow control greatly simplifies the higher layers of the protocol, since it prevents data from being lost due to buffer overflow and so removes the need for re-transmission unless errors occur. To the user of the system, the net result is that a link functions as a pair of fully handshaken first-in, first-outs, one in each direction.

Note that the link interface regulates the flow of data items without regard to the higher layer objects that they may constitute. At any instant the N_chars buffered by a link interface may form part or all of one or more consecutive higher layer objects. L_chars, including FCC, do not belong to such objects and are not buffered.

4.2.4 Layer 3: packet layer

4.2.4.1 Definition of a packet

A packet is a sequence of characters (N_chars only) with a specific order and format. Constituent characters of different packets shall not be interleaved on a link. A packet consists of a *destination* followed by a *payload*. A packet is delimited by an end_of_packet marker.

4.2.4.2 General description

Terminal nodes generate (source node) and consume (destination node) packets. A network is any set of devices connected by links joining (directly or indirectly) a set of terminal nodes.

The protocol assumes the use of packet-switched networks in which the routing information necessary to correctly transmit the packet across the network is contained in the first K N_chars of the packet (where K is fixed throughout a subnetwork). It is at the packet layer that the routing decisions are taken. The protocol does not define a specific (or maximum) size for a packet. Successive packets transmitted on a link may have different lengths and/or destinations.

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Each packet is transmitted in its entirety, i.e., the transmission of a packet on a link shall be completed before the transmission of the successive packet may commence. Packets sent from a given source node to a given destination node over a network may be delivered in an order different from the sending order. The details of mechanisms to ensure in-order delivery are outside the scope of this standard.

4.2.4.3 Destination

The destination contains one or more destination identifiers (dest_id) that are used as the input to the routing function, enabling the routing network to transit the packet from its source node to its destination node. The destination could be null for specific case of a point-to-point link (i.e., the network is just one link). More than one dest_id may denote the same destination node. The method of allocating dest_ids to destinations is outside the scope of this standard. See also clause 9. and annex E.

4.2.4.4 Payload

The payload is the data (a message, a memory access request, an acknowledgment, etc.) that has to be transferred from the source node to the destination node. It has a specific format, defined in the transaction layer. Note that a payload may be null.

4.2.4.5 End of packet marker

A packet is delimited by an end of packet marker.

4.2.5 Layer 4: transaction layer

A transaction is a sequence of packets sent between two or more terminal nodes to perform some function. At this layer there are two concepts:

a) Definition of the specific payload formats necessary to perform the function
b) Definition of the sequence of exchanges of packets necessary to perform required function

The definition of any form of transaction is outside the scope of this standard. Annexes F and I illustrate the use of the transaction layer.

4.3 Interaction of layers

The interaction of the layers is illustrated in figure 4-3.

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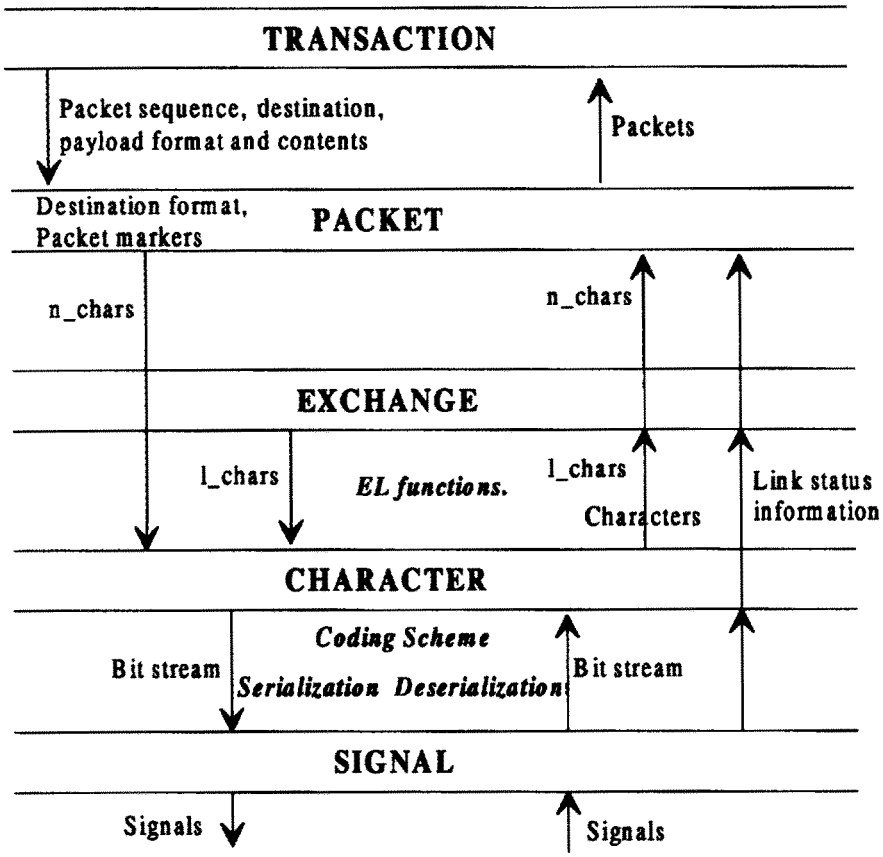

Figure 4-3 —Protocol stack diagram showing interaction of layers

4.3.1 "Downward going"

4.3.1.1 Transaction layer to packet layer

The transaction layer provides packets to the packet layer. The packet sequence, payload contents and destination address(es) are all determined by the transaction layer. The packet layer forms the packet destination from the destination address(es) and appends the packet with the appropriate end_of_packet marker.

4.3.1.2 Packet layer to exchange layer

The packet layer provides the sequence of N_chars that forms each packet to the exchange layer.

4.3.1.3 Exchange layer to character layer

The exchange layer passes the N_chars that have been provided to it by the packet layer onto the character layer. In order to perform the exchange layer functions, it intefieaves L_chars arbitrarily into the sequence of N_chars. The sequence of N_chars is unchanged.

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4.3.1.4 Character layer to signal layer

The character layer translates the characters (N_chars and L_chars) it receives from the exchange layer into a bit stream that it passes to the signal layer. The translation is formed of two parts: coding and serialization. Coding is the translation from the original set of bits (character) to a new set of bits (coded character) suitable for serial transmission. Serialization is the process of transmitting coded characters one bit at a time.

4.3.1.5 Signal layer

The signal layer takes the bit stream and outputs signals onto the physical medium.

4.3.2 “Upward Going”

4.3.2.1 Signal layer to character layer

At the receiver end, the signal layer receives signals from the line and generates the corresponding bit stream.

4.3.2.2 Character layer to exchange layer

The character layer deserializes and decodes the bit stream to produce a sequence of characters. Deserialization is the assembly of a coded character from the sequence of serial bits. Decoding is the translation from the coded set of bits (coded character) to the original set of bits (character). The characters are passed to the exchange layer.

4.3.2.3 Exchange layer to packet layer

The exchange layer filters out L_chars for exchange layer functions and passes the N_chars to the packet layer.

4.3.2.4 Packet layer to transaction layer

The packet layer reconstitutes the packets from the received N_chars. This is a logical reconstitution and need not imply that a whole packet is physically assembled. Routing functions are carried out at the packet layer, based on the information in the packet destination. When necessary (e.g., when a packet has arrived at its destination node), the packets are delivered to the transaction layer.

4.3.2.5 Link status information

Link status information is passed up between the layers from the signal layer to the packet layer. The link status information necessary is dependent on the implementation of the link and includes, for example, information on the calibration of the receiver, parity errors, etc. It is for each layer to filter the information that is relevant to its functioning and to pass up the remaining information.

4.4 Implementations defined in the standard

The physical and logical layers defined in this standard are illustrated in figure 4-4.

The physical layer may be implemented in a number of different technologies, identified according to signaling convention, transmission medium, and maximum operating speed.

The format for this identification is given by three parameters:

SC-TM-dd

The possible values of these parameters are given in table 4-1.

Table 4-2 provides the major properties of each of the defined implementations.

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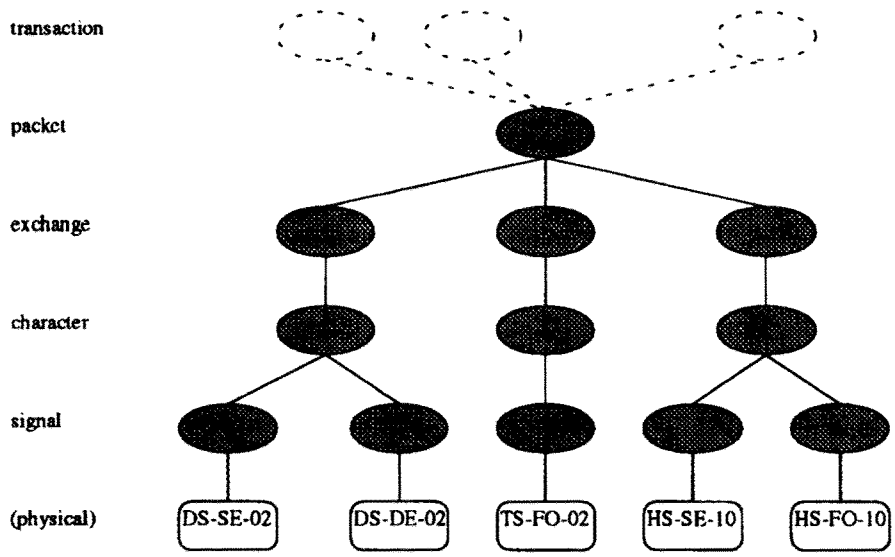

Figure 4-4 —Defined implementations of physical and logical layers

Table 4-1 —Identification format for technologies

Parameter	Values	Description
SC	DS	Data/strobe encoding
	TS	Three-of-six encoding
	HS	High speed encoding
TM	SE	Single-ended electrical transmission
	DE	Differential electrical transmission
	FO	Fiber optic transmission
dd	Two digits, representing the maximum operating speed in units of 100 MBd	

DS-SE links are intended for use for chip-to-chip and board-to-board interconnect. This standard does not therefore specify any cable/connector system for these links. DS-DE links are intended for interconnecting sub-racks and adjacent racks using a protocol compatible with DS-SE link from the character layer upwards. TS-FO links are intended to provide longer distance transmission using, necessarily, optical technology, but at speeds compatible with DS-SE links. The use of optical technology necessitates some differences at the exchange layer. HS-SE links are intended for high speed rack-to-rack interconnect. They can, of course, also be used between chips and between boards (across a backplane), given suitable attention to maintaining appropriate signal integrity. HS-FO links are intended to provide longer distance transmission using a protocol compatible with HS-SE links from the character layer upwards.

This standard specifies an appropriate cable/connector system for each of the technologies specified within this standard, with the exception of DS-SE links. The connector system is intended as a front-panel adapter and matching cable mounted connector.

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Table 4-2 —Defined implementations

Technology	Baud Rate	Maximum bidirectional data rate	Type of transmission (full duplex)	Maximum distance	Connector specification
Units	**Baud**	**MByte/s**	**—**	**Meters**	**—**
DS-SE-02	1.333-200 M	38	4 wires	1	None
TS-FO-02	250 M	39.4	2 multimode fibers	300	IEC 1754-6
DS-DE-02	1.333-200 M	38	8 wires	10	IEC 1076-4-107
HS-SE-10	700-1 000 M	160	2 coax cables	8	IEC 1076-4-107
HS-FO-10	700-1 000 M	160	2 62.5 µm multimode fibers	100	IEC 1754-6
			2 50 µm multimode fibers	1 000	IEC 1754-6
			2 single-mode fibers	3 000	IEC 1754-6

This standard does not specify any backplane or mezzanine connector standards. This is considered more appropriately specified as an adjunct to specific existing backplane standards.

5. DS-SE and DS-DE

5.1 General

The DS-SE and DS-DE links are designed for point-to-point communication that may be on a single PCB, board to board (DS-SE links), or box to box (DS-DE links). Since this implies that transmission line problems might be present, the electrical level is specified as a transmission line system. In order to reduce the power required for each link (permitting single chips to have a large number of link ports) source-only termination is used for DS-SE links.

A DS-SE/DS-DE input is self-clocking, which means that in any particular system the actual operating speed may be chosen to suit the system, rather than the more normal case of having to engineer a system to suit a pre-determined transmission speed. The maximum speed at which it may run is a function of the maximum speed of the circuitry at each end, plus the properties of the medium connecting the two ends. A link may be operated at lower speeds, for example to provide power saving, down to a level at which the disconnection detection mechanism is triggered.

A link shall operate at a speed of 10 MBd unless and until the system in which it operates determines that it may operate at a different speed. The electrical specification of the link has been designed to allow operating speeds of up to 200 MBd, but the actual operating speed is left open to allow the design of any particular system to trade off engineering costs against operating speed. The means of setting the speed of a link is not defined within this standard.

5.2 DS-SE: physical medium

5.2.1 Transmission line requirements

For distances greater than a few centimeters, signal integrity considerations dictate that the link line has to be considered as a transmission line. Discontinuities or variations in characteristic impedance should be kept to a minimum. The transmission line may be made on PCBs but care shall be taken to provide a good ground or power plane beneath the link track and crosstalk with other tracks should be minimized (including between data and strobe

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lines of the same link). The longest length of line achievable will depend on the materials used for interconnect and the grounding arrangements.

DS-SE supports two standard nominal characteristic impedances for the physical medium, 50 Ω and 100 Ω. Drivers conforming to the DS-SE electrical standard shall support one of these impedances and may support both. Each direction (i.e., the data and the strobe line) of a single point-to-point link shall use either one or other impedance throughout the length of the link and use a matched driver. The opposing directions of a single point-to-point link may however use different impedances.

5.3 DS-SE signal level

5.3.1 General

Each connection of a DS-SE link shall be implemented as a unidirectional point-to-point transmission line. The transmission line shall have a characteristic impedance of either 50 Ω or 100 Ω and shall be terminated by high impedance at the receiver. The transmission line may be provided by PCB, coax or other suitable controlled impedance interconnect. The receiver shall be designed to accept standard TTL input switching levels with a high input impedance. The driver output impedance should be close to the characteristic impedance of the transmission line both when the driver is driving low or high and also while switching. This is to ensure that reflections generated by the receiver are sufficiently damped by the driver that they do not cause spurious transitions. The range 0.8 V to-2.0 V at the receiver is defined as the transition region. It is very important that the signal at the receiver is monotonic in the transition region, and that the reflections do not cause spurious transitions. This should be ensured by careful design of the interconnect and the driver output.

The propagation of signals is as follows. Assuming that the line is in a steady-state low condition, a high going transition is output by the driver. Because of the relatively high output impedance of the driver compared to the line, this is attenuated, typically to a level of about 1.4 V at the driver output. At the receiver, the high input impedance of the receiver (effectively an open circuit) causes this to appear as a 2.8 V step (taking the input cleanly through the transition region), and the reflection travels back down the line to the driver. Depending on how closely the driver output impedance is matched to the line, this may cause further reflections: it is crucial that the driver is matched sufficiently well that these reflections do not cause spurious transitions at the receiver, or interfere with subsequent output transitions. Propagation for a low-going transition is similar. Figure 5-1 shows example, waveforms for the driver and the receiver end of the transmission line for a 100 Ω system operating from a 5 V supply.

Note that the signal levels at the receiver and the specification of the driver allows DS-SE links to be interconnected between devices operating from 5 V and 3.3 V supply rails as long as the inputs of the 3.3 V devices are tolerant of 5 V signals.

5.3.2 DS-SE link driver

Each driver should have a nominal output impedance of either 50 Ω or 100 Ω depending on the transmission medium to terminate the reflections from the receiver. The output impedance shall be controlled when the output is fully on driving a high or low level, and also while switching. In order to be adequately matched, the characteristics of the driver and the transmission line shall be related as shown in the table 5-1.

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Table 5-1 —Driver to line impedance matching table

		Vdd = 3.0 V to 3.6 V				Vdd = 4.5 V to 5.5 V			
		Zn		Zp		Zn		Zp	
	Units	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Zo=45–55	ohms	29	56	37	67	32	52	55	123
Zo=90–110	ohms	58	112	73	135	64	104	l10	247

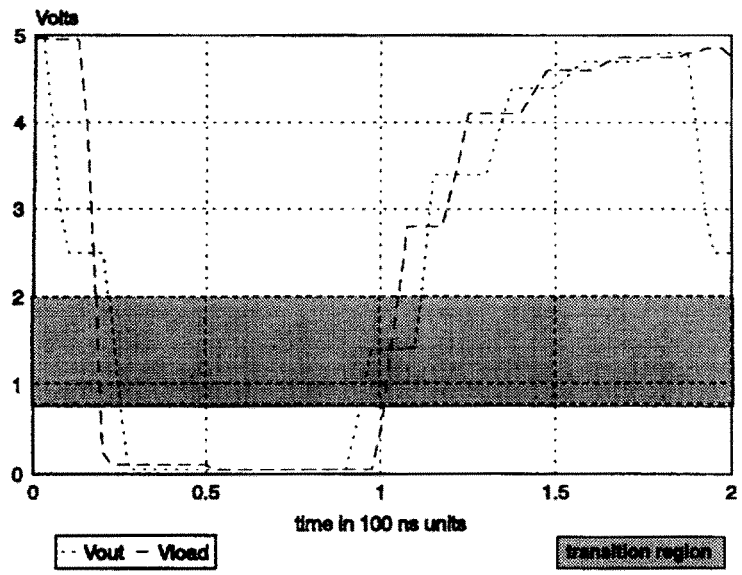

Figure 5-1 —DS-SE link signal propagation

Zo is the characteristic impedance of the transmission line. Zn is the impedance of the driver when the output is driving low, and Zp the impedance when it is driving high. The figures depend on the supply voltage used by the driver because the input threshold is fixed.

It is recommended that nominal 50 Ω characteristic impedance transmission lines be used in nominal 3.3 V systems and on backplanes.

On power on and reset, a DS-SE !ink output shall hold both the data and strobe signals low.

Annex J gives an example DS-SE link driver circuit for a 100 Ω transmission line with 5 V supplies.

5.3.3 DS-SE link receiver

A DS-SE link input shall present a high impedance termination to the transmission line. An impedance of >10 kΩ is recommended. This high input impedance is essential to ensure that the correct signal levels are produced at the receiver input.

The input threshold of the receiver is nominally 1.4 V and shall be within the transition region, which is defined as 0.8–2.0 V.

The input capacitance is modelled as described in 5.3.4 (see figure 5-2) and specified in table 5-2.

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Table 5-2 —DS-SE input capacitance

Symbol	Parameter	Units	100 MBd		100 MBd		200 MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Ci	Input capacitance	pF	—	300	—	30	—	4	—

5.3.4 DS-SE link timing

A link shall operate at a speed of I0 MBd, until the system in which it operates shall determine it may operate at a different speed. A link may be operated at a speed lower than its nominal speed to suit the transmission medium. If a link is operated at a lower speed, the same timing constraints shall apply at the receiver inputs.

DS-SE parameters are relative to a reference model, as shown in figure 5-2.

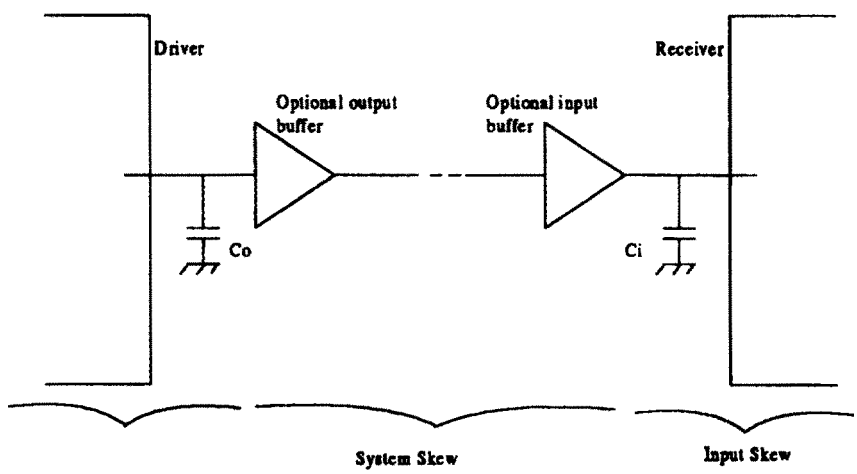

Figure 5-2 —DS-SE timing reference model

This model shows the possibility of buffers in the signal path, in which case the output impedance of the second buffer is assumed to be not more than 100 Ω and Co is assumed to be not more than Ci. If buffers are not used then Ci and Co are combined into a single capacitive load that may be twice the figure given in table 4. If the output drivers are matched to 100 Ω and it is required to use 50 Ω transmission lines, then buffers will be required.

Three sets of timing parameters are defined (see table 5.3 figure 5-3), to allow for operation at the default speed of 10 MBd (DS-SE-00 links), 100 MBd (DS-SE-01 links), and 200 MBd (DS-SE-02 links). A higher speed link type will always be able to operate at a lower speed.

Table 5-3 —DS-SE timing and swings

Symbol	Parameter	Units	10 MBd		100 MBd		200MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
tDSI	D/S edge min. separation	ns	—	20	—	2.5	—	1	1.2
tDSDSI	Sustainable input bit period	ns	80	750	9	750	4.5	750	3
tLIDSf	Input fall time (2.0–0.8 V)	ns	—	100	—	100	—	100	4
tLIDSr	Input rise time (0.8–2.0 V)	ns	—	100	—	100	—	100	4

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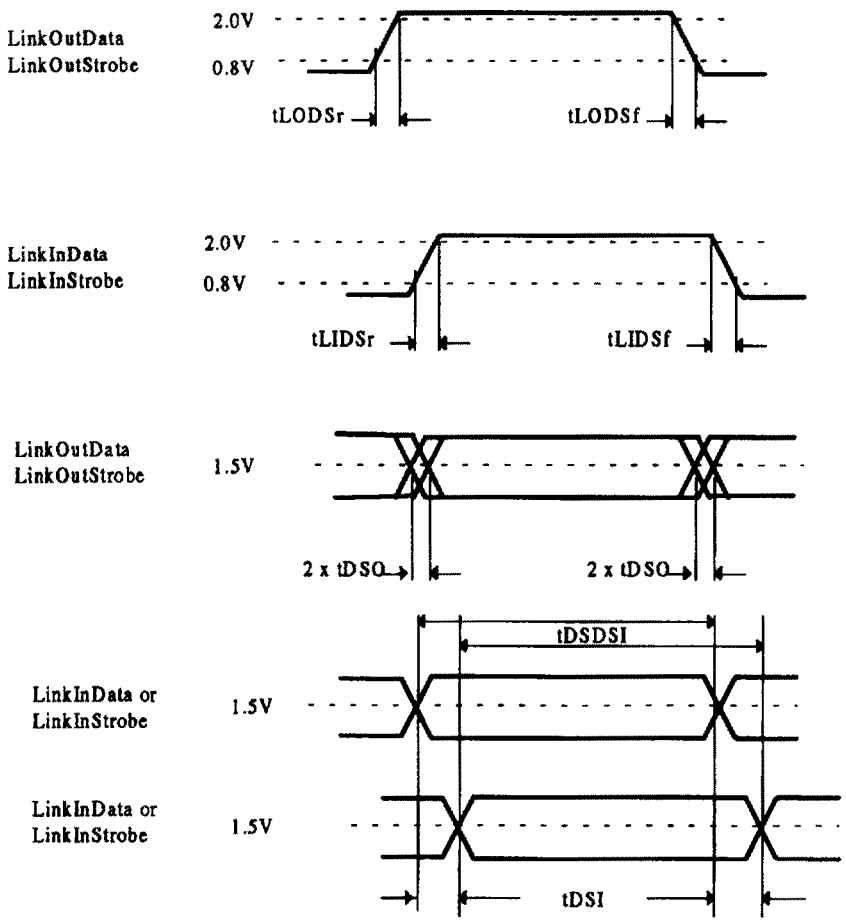

NOTES

1—tDSI is the minimum separation between consecutive edges on the data and strobe inputs (one edge of either sense on each wire) that the link can discriminate correctly. An implementation shall not require this to be greater than the appropriate value specified in table 5-3.

2—The same figure applies to consecutive edges of opposite sense on either the data or the strobe input.

3—In general a link input cannot handle a continuous stream of edges separated by tDSI. This figure specifies the sustained bit period that shall be accepted for the nominal baud rate. The maximum nominal bit time is determined by disconnect time-out period of the link receiver.

4—This is the slowest edge that the input shall accept.

Figure 5-3 —DS-SE link timings

The output skew is determined by parameters given in table 5-4.

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Table 5-4 —S-SE output skew parameters

Symbol	Parameter	Unit	10 MBd		100 MBd		200 MBd		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
tDSO	Output DIS skew	ns	—	±5	—	±1	—	±0.5	1
tLODSf	Output fall time (2.0–0.8 V)	ns	—	40	—	4	—	2	—
tLODSr	Output rise time (0.8–2.0 V)	ns	—	40	—	4	—	2	—
NOTE — This is a skew measured at the 1.5 V threshold relative to the nominal time at which it is specified to cross it, defined in terms of consecutive edges. For example, if two consecutive edges are nominally 5 ns apart, the length of time between the time at which each will cross the threshold can be 5 ns apart, the length of time between the time at which each will cross the threshold can be 5 ns ±tDSO.									

Allowable system skew is determined by the constraint that the sum of tDSI, the range of tDSO and the system skew shall not exceed nominal bit time. Thus, for DS-SE-01 links the system skew shall not exceed 5.5 ns.

5.3.5 DS-SE link signals

Information on a DS-SE link shall be transmitted using two connections, referred to as data and strobe respectively, in each direction. Each connection shall satisfy the electrical constraints specified in the previous subclause. The data line carries binary data values, and the accompanying strobe line changes state each time the next bit has the same value as the previous one (this does not correspond with the usual meaning of “strobe,” which would be a signal that indicates every time that another signal is valid). By this means each DS pair carries an encoded clock, in a way that allows up to a full bit-time of skew-tolerance between the two connections. Figure 5-4 shows the form of signals on the data and strobe connections.

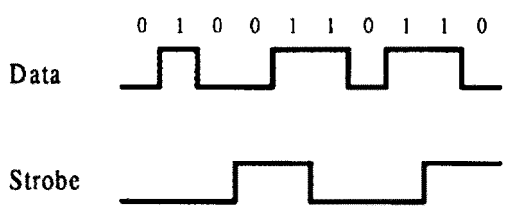

Figure 5-4 —DS-SE link signal encoding

Since the data-strobe system carries a clock, the links are asynchronous; the receiving device synchronizes to the incoming data, This means that DS-SE (and DS-DE) links autobaud; the only restriction on the transmission rate is that it does not exceed the maximum speed of the receiver. This also simplifies clock distribution within a system, since the exact phase or frequency of the clock on a pair of communicating devices is not critical. It is not essential that both link outputs of one link connection should operate at the same speed, nor that a link output operate at a constant speed. A link output might choose to vary its speed of operation to reduce power consumption when there is no data to be transmitted, for example. The only constraint on the transmission rate is that the bit time limits given in table 5-3 are not violated, and that it is high enough to prevent a disconnect timeout being triggered (see 5.7.4.2).

A DS-SE link output transmits information on a pair of lines, and a DS-SE link input receives information on a pair of lines. A DS-SE link interface shall comprise a DS-SE link output and a DS-SE link input.

A device providing one or more DS-SE link interfaces shall identify the pins used for each link interface by a convention (using subscription where multiple links are supported) based on function and direction of transmission as shown in table 5-5.

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Table 5-5 —Identification of multiple link interfaces

DS_SE_data_in	For input of data to the device through the link interface
DS_SE_strobe_in	
DS_SE_data_out	For output of data from the device through the link interface
DS_SE_strobe_out	

A DS-SE link is constructed by connecting the DS_SE_data_out and DS_SE_strobe_out of one link interface to the DS_SE_data_in and DS_SE_strobe_in respectively of the other link interface, and vice versa.

The DS_SE_data_out and DS_SE_strobe_out of a link interface may be connected to the DS_SE_data_in and DS_SE_strobe_in respectively of the same link interface to create a loopback, e.g., for link testing.

5.4 DS-DE: physical medium

5.4.1 Link cable

A DS-DE link cable shall provide ten connections. Eight connections (in four pairs) shall support the eight signals in the DS-DE link; the ninth and tenth connections shall support an optional remote power facility.

A recommendation for the DS-DE cable is given in annex M.

Each connection in the cable shall be color coded as given in table 5-6 and have the characteristics as given in table 5-7. Note that attenuation and skew budgets are given in 5.5.3 and 5.5.4. (See also 10.3.)

Table 5-6 —DS-DE cable color code

Component	Conductor 1	Conductor 2
Pair 1	Red	Green
Pair 2	Brown	Blue
Pair 3	Orange	Yellow
Pair 4	Violet	Gray
Pair 5	Black	White

The link cable shall be clearly marked “IEEE 1355 DS-DE Link Cable.”

5.4.2 Connector

The connector system consists of a through-panel (fixed) connector and a cable-mounted (free) connector.

It provides the following features:

a) A full duplex link connection per connector
b) Option for multiple connections on the cable connector
c) Complete screening
d) Robust
e) Latching
f) Small size

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The DS-DE connectors shall be as specified in IEC 1076-4-107.

Table 5-7 —Electrical and mechanical characteristics and safety certification of DS-DE cable

Electrical characteristics	
Differential impedance	95 Ω ± 10 Ω
EMC	Cable shall allow system to meet CISPR 22 regulations
Near end crosstalk (backward)	2% maximum at 100 MHz measured on 10 m sample in differential mode
Far end crosstalk (forward)	4% maximum at 100 MHz measured on 10 m sample in differential mode
Mechanical performance	
Flexibility	A 60 mm maximum radius shall result when 610 mm of cable is loaded with a suspended weight of 100 g
Flex life	1000 cycles through 180 degrees at 60 mm bend radius and 100 g load. Following this test, the insulation and jacket should be free of cracks and the conductors free of opens and shorts.
Minimum bending radius (static operation)	40 mm
Safety certification	
For cables up to 10 ft (3 m) in the US	UL listing: AWM style 20276, 80C, 30 V, VW1
For cables 10 ft (3 m) to 100 m	UL listed class 2 power limited circuit cable (CL2)

The (free) connector at either end of the cable shall be connected to the conductors in the cable according to table 5-8.

Table 5-8 —DS-DE link cable conductors/connectors wiring

Pin	Conductor	Pin
1a	Pair 2 brown	2e
2a	Pair 2 blue	1e
1b	Pair 1 red	2d
2b	Pair 1 green	1d
1c	Pair 5 white	1c
2c	Pair 5 black	2c
1d	Pair 3 orange	2b
2d	Pair 3 yellow	1b
1e	Pair 4 violet	2a
2e	Pair 4 grey	1a

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Note that the effect of the cable/plugs assembly is to provide a single twist in each of Pairs 1, 2, 3, and 4, and to provide a single twist between Pairs 1 and 3 and between Pairs 2 and 4. This is shown in figure 5-5 using Pairs 2 and 4 as an example.

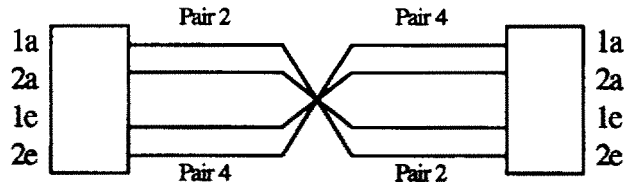

Figure 5-5 —DS-DE cable assembly twist example

Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 5-6.

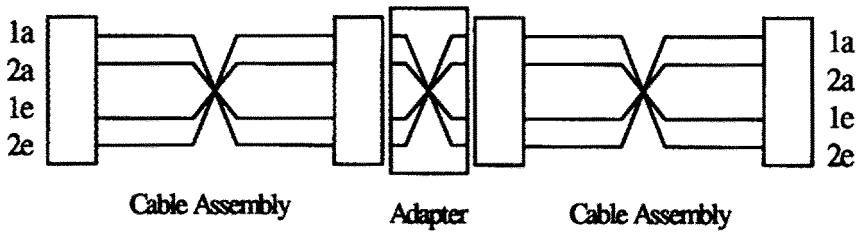

Figure 5-6 —DE-DE extension adapter

The allocation of DS-DE signals to the connector pins shall be as given in table 5-9 [which is oriented to correspond to the external view of the through-panel (fixed) connector when mounted on the upper surface of a horizontal PCB. See figure 5-7.]. The direction of the signals is as on the fixed connector.

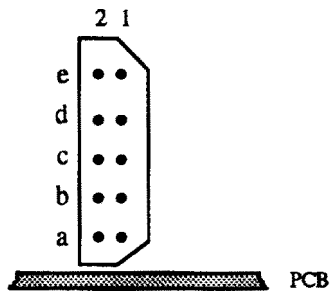

Figure 5-7 —DS-DE fixed connector external view

Pins 1c and 2c of the DS-DE fixed connector are either both left unconnected on the PCB, or are used to implement an optional power supply, as specified in 5.4.4. It is recommended that fixed DS-DE link connectors with neither source nor sink power connections should include 10 MΩ bleeders to ground on pins 1c and 2c to prevent static build-up on otherwise unconnected power conductors.

In addition to the interface specification of IEC 1076-4-107, the connectors shall have the properties described in table 5-10.

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Annex L provides a recommendation for the PCB layout of the fixed connector.

Table 5-9 —Pin allocation of DS-DE connector

	2	1	
e	DS_DE_data_in_plus	DS_DE_data_in_minus	(Chamfer corners at this side of the connector)
d	DS_DE_strobe_in_plus	DS_DE_strobe_in_minus	
c	No connect or optional power return	No connect or optional power	
b	DS_DE_strobe_out_minus	DS_DE_strobe_out_plus	
a	DS_DE_data_out_minus	DS_DE_data_out_plus	

Table 5-10 —DS-DE connector modularity specifications

Characteristic	Specification
Modularity	Fixed connector modules shall be placed on a 6 mm pitch, or their centerlines separated by more than 12 mm
Connector width	5.9 mm maximum

5.4.3 Environmental constraints

The environmental requirements for the DS-DE link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 5-11. Note that specific applications may have requirements for extended temperature range, or other environmental parameters.

Table 5-11 —DS-DE environmental constraints

Parameter	Value
Operating temperature	–10 °C to +60 °C
Non-operating temperature	–40 °C to +85 °C

5.4.4 Optional power supply to DS-DE cable

5.4.4.1 Optional power supply

An explanation of the remote power, and recommendations of components that should meet the following specification, are given in annex K.

Pin 1c either provides an output power supply based on the equipment's 5 V VCC, with a self-healing fuse for overcurrent protection and a (Schottky) diode for reverse-current protection, or provides power to local circuitry from a remote source. Components should be chosen to meet the specification given in table 5-12. Pin 2c provides for power return.

The load drawn from this power supply at the end of 500 mm cable with conductors as specified for the DS-DE link cable, shall meet the specification given in table 5-13. The product of power used and cable length shall not exceed 1 W·m.

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Table 5-12 —Optional power supply

Symbol	Parameter	Value
IpHold	Hold current, the operating current that the overcurrent protection device will pass without going high impedance	750 mA minimum
VpOHmin.	Output voltage with respect to pin 2c at maximum steady state output current	3.75 V minimum at 750 mA
VpOHmax.	Output voltage with respect to pin 2c at any output current greater than a leakage current of 1 mA	5.0 V maximum
IpReverse	Reverse-current	1 mA maximum at reverse voltage of 12 V with respect to pin 2c

Table 5-13 —Optional power supply load

Symbol	Parameter	Value
Pp	Power consumption	2.5 W maximum
VpRemoteLow	Lowest input voltage with respect to pin 2c at remote power supply at which the remote power supply is able to supply the required power	3.5 V maximum
VpRemoteHigh	Highest input voltage with respect to pin 2c at remote power supply that the remote power supply can tolerate	5.0 V minimum

5.4.4.2 Power supply protection

The above specification for the remote power supply defines the minimal requirements for operation in the absence of a fault. It is recommended that the overcurrent protection device meets the specification given in table 5-14 in the event of an overcurrent fault.

Table 5-14 —Optional power supply protective device

Symbol	Parameter	Value
IpTrip	Trip current, the minimum current that will cause the overcurrent protection device to switch to a high-impedance state	2.5 A
TpTrip	Trip time, the maximum time for the overcurrent protection device to switch to its high impedance state with a fault current of 10 A	0.5 s
TpReset	Reset time, the time from when a fault is removed to when the overcurrent protection device returns to its specified characteristics	1 h maximum (but note typical recovery to within 20% of specification, normally within less than 1 min)

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5.4.4.3 Layout convention

It is recommended that in any block of adjacent DS-DE link connectors, the end connector with space adjacent to its pins 1 (the end with the D chamfers of the connector pointing outwards from the block), be supplied with power on pin 1c, and that if more than one connector in any block be supplied with power, all such connectors should be adjacent (see figure 5-8). Equipment need not have special markings to identify connectors supplying power, but it is recommended that such connectors are clearly documented.

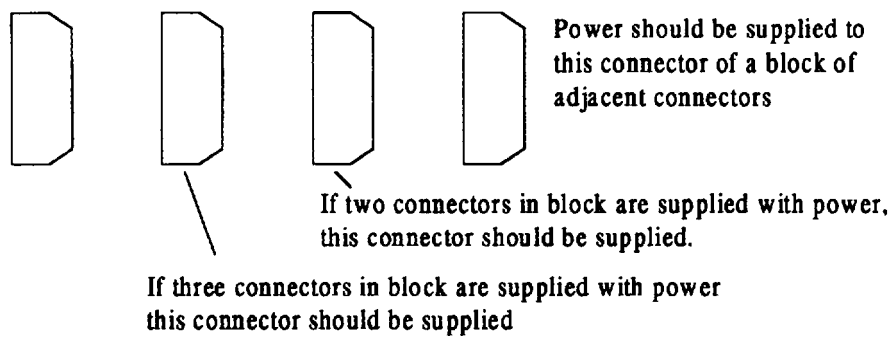

Figure 5-8 —Multiple power connectors

5.5 DS-DE signal level

5.5.1 General

Differential signaling may be used, e.g., for connections between equipment. Differential signaling provides the following advantages over single-ended signaling:

a) Increased noise immunity
b) Avoidance of ground loops between equipment

A DS-DE link interface may be constructed by connecting two differential drivers and two differential receivers to a DS-SE link interface as follows:

— Each connection point of the DS-SE link output is connected to the input of a differential driver, generating a pair of balanced signals from the on-board DS-SE electrical specification. The two pairs of signals form the DS-DE link output.
— Each connection point of the DS-SE link input is connected to the output of a differential receiver, converting two pairs of balanced signals into two signals conforming to the on-board DS-SE electrical specification. The two pairs of signals form the DS-DE link input.

A DS-DE link interface shall have the logical properties that it would inherit if connected to a DS-SE link interface in this way. This is the recommended implementation of a DS-DE link interface.

A DS-DE link is constructed by connecting two DS-DE link interfaces by a suitable eight-wire transmission line, in the manner defined in 5.4.

A system built using DS-DE links shall meet CISPR 22 regulations concerning electromagnetic emissions.

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5.5.2 DS-DE signals

Each connection in a DS-DE link shall be made with a nominal 95 Ω transmission line. The transmission line shall be terminated at the receiver inputs: the combination of receiver input impedance and line termination shall be 100 Ω.

The signaling uses a pair of balanced pseudo-ECL signals. Pseudo-ECL signals have ECL-levels shifted by 5 V. See table 5-15.

Table 5-15 —DS-DE signal levels

Parameter	Units	Min.	Typ	Max
Driver differential output voltage	V	0.8	1.0	1.4
Driver common mode output voltage	V	2.5	—	4
Driver output rise time (20–80%)	ns	0.5	—	2
Receiver input impedance (including termination resistance)	Ohms	90	100	110
Receiver input common mode voltage	V	–1.2	—	7.2
Receiver sensitivity	mV	200	—	—

The relevant buffer shall not be placed more than 3 cm from the corresponding fixed connector unless the tracks between the buffer and the connector are matched to 100 Ω.

The DS-SE connection consists of four signals. Each pair of DS-DE signals is specified by reference to a corresponding DS-SE signal, as defined in table 5-16. Note that DS-DE signals need not be implemented by being derived from the corresponding DS-SE signals.

Table 5-16 —DS-DE correspondence

Single-ended side	Differential side	
DS_SE_data_out	DS_DE_data_out_plus	DS_DE_data_out_minus
DS_SE_strobe_out	DS_DE_strobe_out_plus	DS_DE_strobe_out_minus
DS_SE_data_in	DS_DE_data_in_plus	DS_DE_data_in_minus
DS_SE_strobe_in	DS_DE_strobe_in_plus	DS_DE_strobe_in_minus

In each differential pair, the plus version of the signal is positive going when the corresponding single ended signal is positive going, and vice versa.

A link shall connect two sets of differential pairs by connecting the DS_DE_data_out_plus of one set to DS_DE_data_in_plus of the other set, DS_DE_strobe_out_plus of one set to DS_DE_strobe_in_plus of the other set, and similarly for the _minus signals.

5.5.3 DS-DE_attenuation budget

The total attenuation for each of the DS-DE signals (from output of the driver to input of the receiver) shall be less than or equal to 6 dB at 100 MHz. This attenuation shall be divided following the guidelines given in table 5-17.

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Table 5-17 —Attribution of attenuation budget

Parameter	Maximum attenuation/dB
Output of driver to output of connector	0.5
Across cable	5
Input to connector and input of receiver	0.5

5.5.4 DS-DE skew budget

The skew shall be divided following the guidelines given in table 5-18.

Table 5-18 —Attribution of skew budget

Parameter	Maximum skew between D and S/ns		
	10 MBd	100 MBd	200 MBd
Output of differential driver to output of connector	5	0.5	0.35
Across cable	15	1.5	1.3
Input to connector and input of differential receiver	5	0.5	0.35

If the DS-DE links are implemented by using transceivers to convert between the differential signals and the corresponding single ended DS-SE signals, then the differential skew between D and S shall be controlled so that the resulting single ended signal respects the guidelines given in 5.3.1.

5.5.5 DS-DE link timing

DS-DE link timing is as for DS-SE timing (see 5.3.4, with references to DS-SE replaced by DS-DE).

5.5.6 EM Susceptibility

A system using DS-DE links shall meet or exceed IEC 801-4 specifications on EM susceptibility as a function of the intended operating environment. To reduce susceptibility to EMC it is recommended that it is ensured that the fixed connector is connected to housings by using appropriate EMC brackets and/or gaskets (similar to B.3), or that small common-mode chokes are used in series on the signal lines, and the power lines if connected. A suitable specification for such chokes is 200 Ω min at 20–300 MHz, 800 Ω typ at 100 MHz.

5.6 DS-SE and DS-DE character level

In order to provide efficient support for higher level protocols, it is useful to be able to encode characters that may contain a data byte or control information (in other standards these might be referred to as symbols). Each character shall start with a parity bit followed by a control bit that is used to distinguish between data and control characters. In addition to the parity and control bits, data characters contain 8 b of data, and control characters have 2 b to indicate the character type. This is illustrated in figure 5-9.

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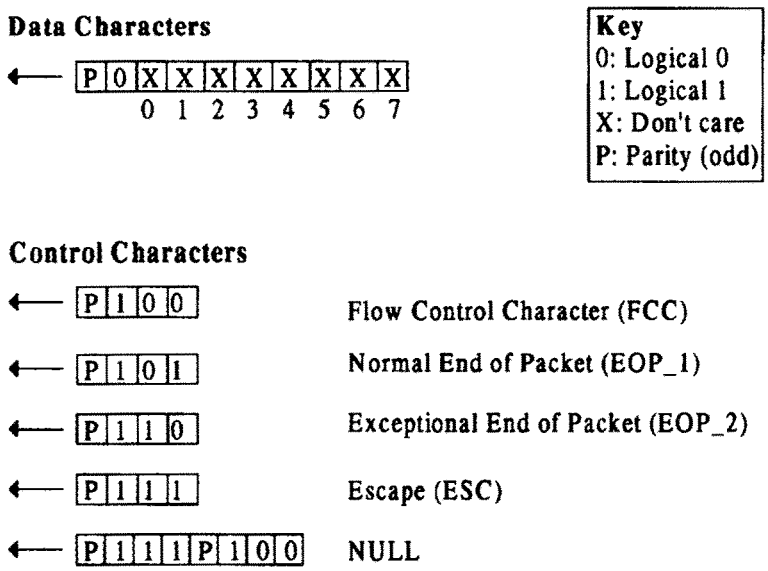

Figure 5-9 —-DS-SE/DS character encoding

Data bits shall be transmitted using the “little endian” convention, i.e., the least significant bit of data shall be transmitted first (immediately after the zero control bit). The first bit transmitted after a reset state shall be a zero (which implies that the first transition is on the strobe wire).

The parity bit in any character covers the parity of the data/control flag in the same character, and the data or control bits in the previous character, as in figure 5-10. This allows an error in any single bit of a character, including the character type flag, to be detected even though the characters are not all the same length. The parity bit is set such that the total number of 1s in all the bits covered (including the parity bit) is odd.

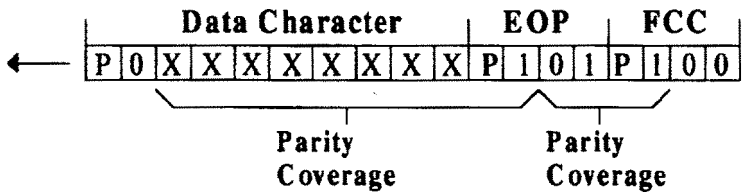

Figure 5-10 —DS-SE/DS-DE parity coverage

DS-SE/DS-DE links code the N_chars EOP_1 and EOP_2 as shown in table 5-19, in which P indicates the position of the parity bit in the character.

DS-SE/DS-DE links define and code L_chars as shown in table 5-20, and their application is discussed in 5.7.

The null character is composed of two characters. The scope of the parity bit in a character that follows a null character includes only the second 4 b control character of the null character; i.e., it will be a one if the following character is a data character, and will be a zero if following character is a control character.

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Table 5-19 —Terminator character codings

Name	Description	Code
EOP_1	Normal end_of_packet marker	P101
EOP_2	Exceptional end_of_packet marker	P110

Table 5-20 —Link control character codings

Name	Description	Code
FCC	Flow control character	P100
ESC	Escape character	P111
NULL	Null character	ESC P100

5.7 DS-SE and DS-DE exchange level

5.7.1 General

Once a link output has been started it shall send characters continuously at such a rate that the bit time constraints given in table 5-2 are never exceeded, unless and until instructed to cease operation or an error is detected. In the absence of other characters, a DS-SE/DS-DE link transmits NULL characters. This ensures the following:

a) Physical disconnection of a link detected; because a DS-SE/DS-DE link transmits characters continuously even in message, a physical disconnect can be assumed if the inputting link detects that there are no-characters being received, given that some have been received previously.
b) The final parity bit of a packet is transmitted immediately; because the parity of each character is validated by the parity bit of the following character, the validation of the final character of a packet would otherwise be delayed for an arbitrary amount of time.

5.7.2 DS-SE and DS-DE initialization

After reset, a DS-SE link output shall maintain both signals at their reset level until started, i.e., instructed to begin operation (note that receipt of a character by the corresponding link input may be taken as such an instruction). Thereafter it shall send only NULL characters unless and until at least one character has been received by the corresponding link input since reset. After the link output has been started and at least one character has been received by the corresponding link input since reset, the link shall begin normal operation. In normal operation, N_chars provided for transmission are sent when there is flow control credit available, and flow control credit is issued by transmitting FCCs corresponding to available space in the link input buffer. A timeline diagram illustrating DS-DE and DS-DE initalization and reset is given in figure 5-12.

If a link interface is reset during normal operation, then it shall cease to transmit. This will be detected as a disconnection error by the receiving interface, which then will also cease to transmit. After the exchange of silence protocol, described in 5.7.4.2 and illustrated in figures 5-11 and 5-12, both ends of the link will enter the ready state and normal operation may begin. The exchange of silence protocol allows the reset procedure to have the desired effect if the two links are operating in separate reset domains

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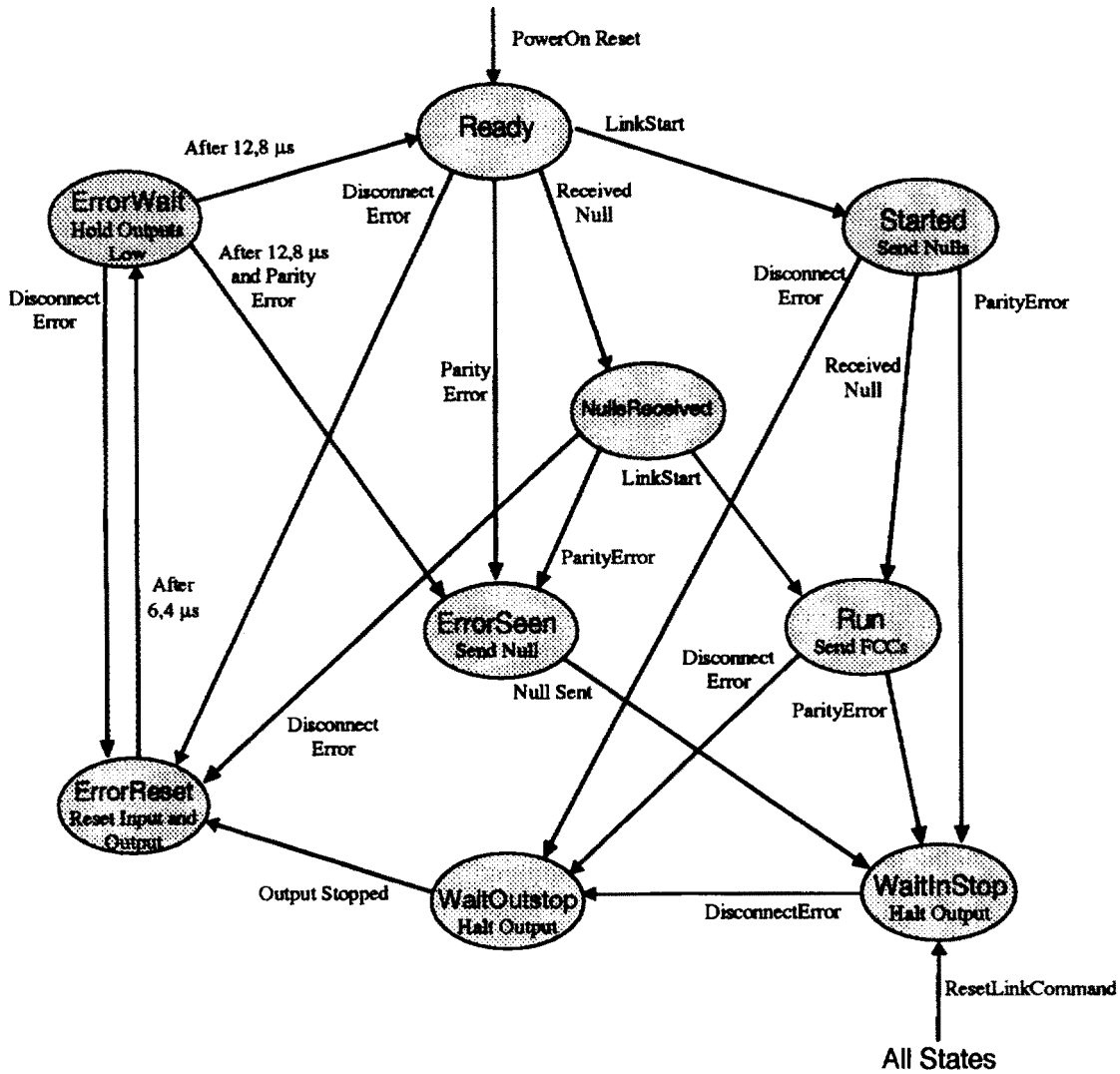

NOTE—In the ErrorReset state, all transitions on the link input shall be ignored, and the flow-control credit counters and input buffer shall be reset.

Figure 5-11 —DS link states

5.7.3 Flow control

The credit value (F) of each Flow Control Character (FCC) is set at 8 N_chars.

5.7.4 DS-SE and DS-DE error detection

5.7.4.1 General

DS-SE/DS-DE links can detect various types of errors. The handling of link errors is a subject of annex G.

The DS-SE/DS-DE link exchange protocol allows two common types of error to be detected. First, because each output link, once started, continues to transmit an uninterrupted stream of characters, the physical disconnection of a

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link can be detected. Second, the parity system will detect all single bit errors at the DS-SE/DS-DE link exchange level.

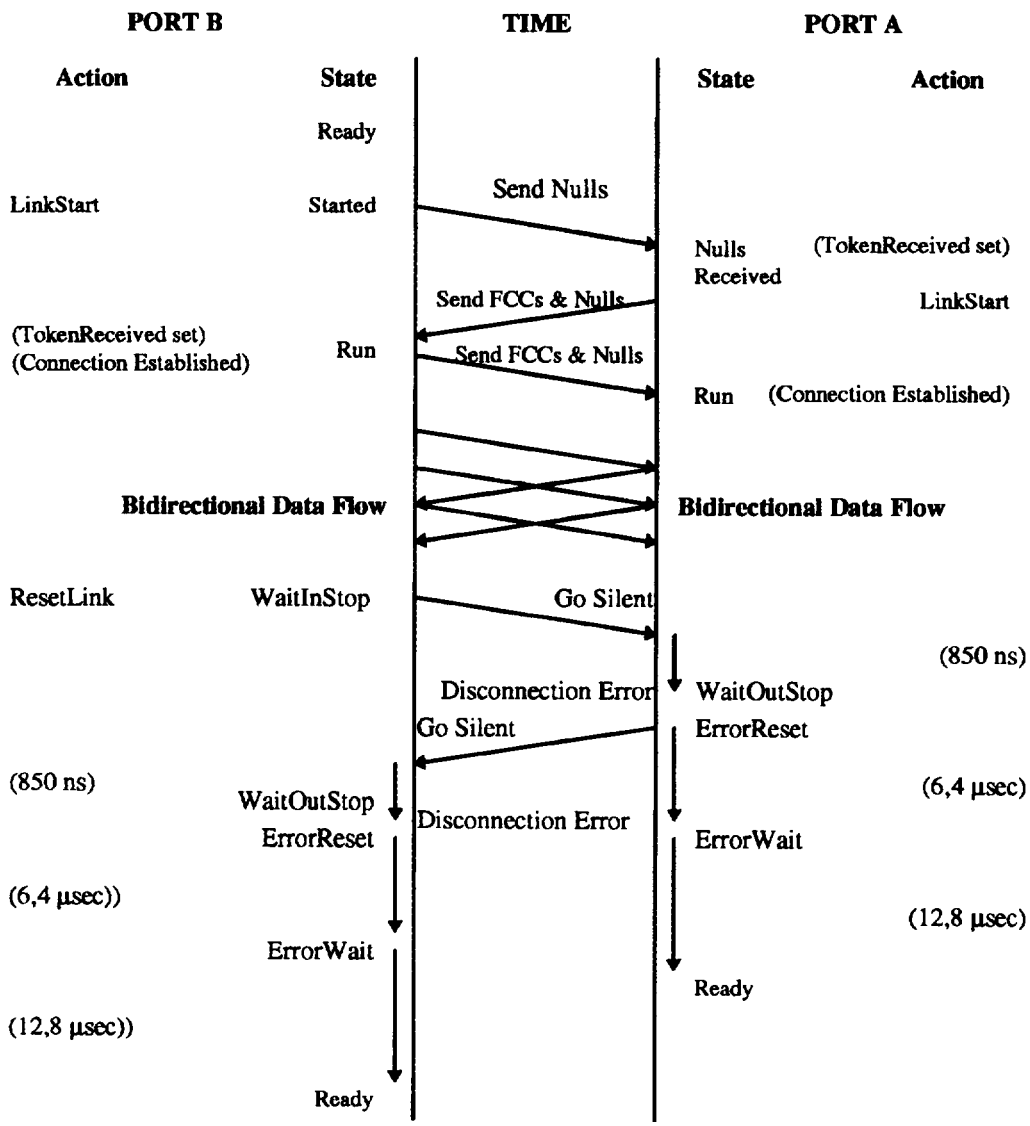

Figure 5-12 —DS link start-up and reset

5.7.4.2 Disconnection errors

If the links are disconnected for any reason while they are running, then flow control and character synchronization may be lost. In order to restart the link it is therefore necessary to reset both ends to a known flow control and character synchronization point.

Disconnection is detected if, after a bit has been received, no bits are seen by a link input in any 850 ns window. Once a disconnection error has been detected the link shall halt its output. This will subsequently be detected as a disconnect error at the other end, and will cause that link to halt its output also. Once the output has halted, the link shall reset both its transmitter and its receiver for 6.4 µs, during which time its receiver is insensitive to transitions on the data and

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strobe inputs. After this, the link shall wait at least 12.8 µs before allowing communication to restart. This time is sufficient to ensure that both ends of the link have observed disconnection and cycled through reset back into the waiting state. The connection may now be restarted as described above. If a link interface detects a disconnect error before it has started, it shall start, transmit at least one character, and then halt, to ensure that a disconnection error is also detected by the other end, in the case that it was caused by an externally applied reset rather than physical disconnection. Figure 5-11 illustrates a suitable state machine for DS-SE and DS-DE error handling.

5.7.4.3 Parity errors

Following a parity error, both character-level synchronization and flow control status are no longer valid, therefore both ends of the link must be reset. This is done autonomously by the DS-SE/DS-DE link using an exchange-of-silence protocol.

When a link interface detects a parity error on its input it shall halt its output. This will subsequently be detected as a disconnect error at the other end, and will cause that link interface to halt its output also, causing a disconnect to be detected at the first end. The normal disconnect behavior described above will then ensure that both ends are reset (irrespective of line delay) before either is allowed to restart. If a link interface detects a parity error before it has been started, it shall start, transmit at least one character, and then stop to ensure that a disconnection error is detected by the other end.

6. TS-FO-02 fiber optic link

6.1 Physical medium

6.1.1 General optical characteristics

The TS-FO-02 optical link cable is a fiber cable containing two fibers, one for transmission in each direction. A 62.5 µm multimode fiber shall be used, and shall meet, at minimum, the specifications given in IEC 793-1 -A1-b. A summary of the main optical characteristics (as specified in IEC 793-1 -Al-b) of the fiber is given in table 6-1.

The link cable shall be clearly marked “IEEE 1355 TS-FO Link Cable.” A recommendation for fiber construction is given in annex S. (See also 10.3.)

Table 6-1 —Summary of main optical characteristics of TS-FO fibers

Parameter	Units	Value
Fiber type	—	Multimode
Core diameter	micrometers	62.5
Cladding diameter	micrometers	125
NA	—	0.275
Attenuation	dB/km	4 maximum at 850 nm

6.1.2 Optical connector

The TS-FO link optical connector is a MU connector-duplex. The MU connector-duplex consists of a through-panel (fixed) adapter and a cable mounted (free) plug. It provides the following features:

a) A dual multimode fiber connection per connector

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b) Push-pull coupling
c) Small size

The connectors shall be as specified in IEC 1754-6. Prior to approval of IEC 1754-6, annex C provides an interim specification.

In addition to the interface specification of IEC 1754-6, the connectors shall have the properties described in table 6-2.

Table 6-2 —TS-FO connector modularity specifications

Characteristic	Specification
Modularity	Connector modules shall be placed on a 14 mm pitch, or their centerlines separated by more than 28 mm
Connector width	13.9 mm maximum
Overall connector length (to end of boot)	55 mm maximum

The plug at either end of the cable shall be connected to the fibers in the cable in such a way as to connect ferrule 1 in one plug with ferrule 2 in the other plug, and vice versa, as shown in figure 6-1.

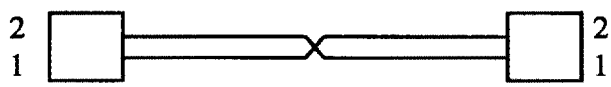

Figure 6-1 —TS-FO cable fibers/plugs wiring

Note that the effect of the cable/plugs assembly is to provide a single twist. Any extension adapters allowing multiple segments of cables to be used shall also provide such a twist, so that the effect of any such cable/adapter/cable combination is to provide a single twist, as illustrated in figure 6-2.

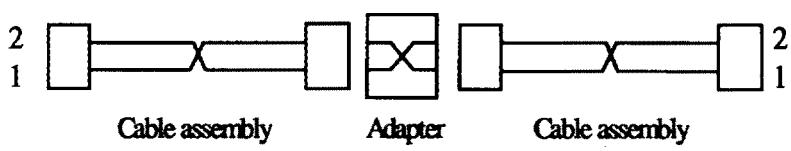

Figure 6-2 —TS-FO extension adapter

The allocation of TS-FO signals to the plug ferrules and adapter shall he as given in table 6-3 (which is oriented to correspond to the external view of the through-panel (fixed) adapter when mounted on the upper surface of a horizontal PCB; see figure 6-3). The direction of the signals is relative to the fixed adapter.

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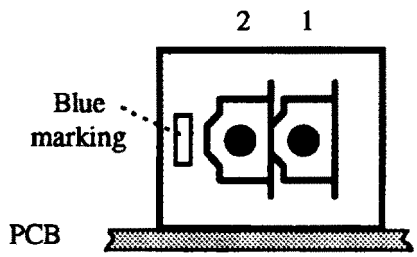

Figure 6-3 —TS-FO fixed adaptor, external view and ferrule allocation

Table 6-3 —TS-FO signal allocation

Ferrule	2	1
Signal	TS_FO_in	TS_FO_out

6.1.3 Environmental constraints

The environmental requirements for the TS-FO link cables and connectors are application dependent. However, as a minimum, the cables and connectors shall meet the constraints in table 6-4. Note that specific applications may have requirements for extended temperature range or other environmental parameters.

Table 6-4 —TS-FO environmental constraints

Parameter	Value
Operating temperature	–10 °C to +6 °C
Non-operating temperature	–40 °C to +85 °C

Further environmental specifications are given in table C.2 (annex C).

6.2 Signal level

6.2.1 Transmitter and receiver characteristics

Launch power and sensitivity are strongly dependent on the kind of optical components used and on the configuration of the LED/laser modulation and of the photodiode amplifier. Table 6-5 gives the recommended transceiver characteristics for an LED-based system.

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Table 6-5 —TS-FO recommended transceiver characteristics

Parameter	Units	Value		
		Minimum	Typ	Maximum
Operating speed	MBd	—	—	250
TS-FO transmitter	—	—	—	—
(LED into 62.5 µm fiber)	—	—	—	—
Launch power	dBm	–13	—	–10
Wavelength	nm	760	—	900
Spectral width (FWHM)	nm	—	60	—
TS-FO receiver	—	—	—	—
Sensitivity atBER 10^{-12}	dBm	–22	—	—
Dynamic range	dB	12	—	—

6.2.2 TS-FO link timing

The TS-FO link shall operate at 250 MBd ± 100 ppm.

6.2.3 TS-FO reference link

A link comprises of two link interfaces connected by appropriate media, and transmits information bidirectionally. For specification and test purposes, a TS-FO Reference Link is defined as a transceiver (the link interface), connected by a pair of fibers to an adapter, connected by a plug-cable-plug assembly to another adapter, connected to another transceiver by a pair of fibers, as shown in figure 6-4. This figure also shows reference test points TP1–TP4 (where TPx are at the extremities of the optical cable).

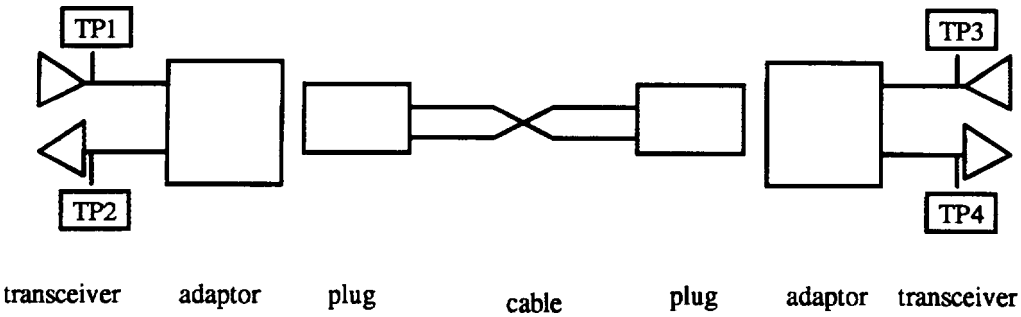

Figure 6-4 —TS-FO reference list

6.2.4 Link performance

The performance of the various components of the link system shall be as in table 6-6. The standard specifies a power budget for a link, i.e., the maximum loss. A “loopback” plug is defined as a single plug with a minimum length of fiber that connects ferrule 1 to ferrule 2. This is used to provide the specification of the loss of a connector system and a reference specification for the power budget for the cable assembly. The performance of a minimum length reference cable is assumed to be equivalent to the performance of the loopback system. Note that this provides a high degree of confidence of interoperability within a practical test environment, but does not provide a guarantee of interoperability.

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