
**Information technology —
Telecommunications and information
exchange between systems — Local
and metropolitan area networks —
Specific requirements —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 10: Media access control
parameters, physical layers, and
management parameters for 200 Gb/s
and 400 Gb/s operation**

*Technologies de l'information — Télécommunications et échange
d'information entre systèmes — Réseaux locaux et métropolitains —
Prescriptions spécifiques —*

Partie 3: Norme pour Ethernet

*AMENDEMENT 10: Paramètres de commande d'accès aux supports,
couches physiques et paramètres de gestion pour le fonctionnement
en 200 Gb/s et 400 Gb/s*



Reference number
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CH-1214 Vernier, Geneva
Phone: +41 22 749 01 11
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Email: copyright@iso.org
Website: www.iso.org

Published in Switzerland

Institute of Electrical and Electronics Engineers, Inc
3 Park Avenue, New York
NY 10016-5997, USA

Email: stds.ipr@ieee.org
Website: www.ieee.org

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IEEE Std 802.3bs™-2017
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
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IEEE Std 802.3bv™-2017, and
IEEE Std 802.3-2015/Cor 1-2017)

IEEE Standard for Ethernet

Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation

**LAN/MAN Standards Committee
of the
IEEE Computer Society**

**Approved 6 December 2017
of the
IEEE-SA Standards Board**

Abstract: Clause 116 through Clause 124 and Annex 119A through Annex 120E are added by this amendment to IEEE Std 802.3-2015. This amendment includes IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

Keywords: 200 Gb/s Ethernet, 200GAUI-4, 200GAUI-8, 200GBASE-DR4, 200GBASE-FR4, 200GBASE-LR4, 200GBASE-R, 200GMII, 200GXS, 400 Gb/s Ethernet, 400GAUI-8, 400GAUI-16, 400GBASE-DR4, 400GBASE-FR8, 400GBASE-LR8, 400GBASE-SR16, 400GBASE-R, 400GMII, 400GXS, EEE, Energy Efficient Ethernet, Ethernet, FEC, forward error correction, IEEE 802.3™, IEEE 802.3bs™, MMF, PAM4, Physical Medium Dependent sublayer, PMD, SMF

The Institute of Electrical and Electronics Engineers, Inc.
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Adam Healey, *IEEE 802.3 Working Group Vice-Chair*
Pete Anslow, *IEEE 802.3 Working Group Secretary*
Steven B. Carlson, *IEEE 802.3 Working Group Executive Secretary*
Valerie Maguire, *IEEE 802.3 Working Group Treasurer*

John D'Ambrosia, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Chair*
Pete Anslow, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor-in-Chief*
Mark Gustlin, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor*
for Clauses 117, 118, 119, Annex 119A
Steve Trowbridge, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor*
for Clause 120, Annex 120A
Peter Stassar, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor*
for Clauses 121, 122, 124
Jonathan King,¹ *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor*
for Clause 123
Andre Szczepanek, *IEEE P802.3bs 200 Gb/s and 400 Gb/s Ethernet Task Force Editor*
for Annexes 120D, 120E

Justin Abbott	David Chalupsky	Andrew Gardner
David Abramson	Jacky Chang	Claude Gauthier
Shadi Abughazaleh	Xin Chang	Ali Ghiasi
Mohammad Ahmed	Ahmad Chini	Joel Goergen
Eric Baden	Keng Hua Chuang	Volker Goetzfried
Amrik Bains	Christopher R. Cole	Zhigang Gong
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Denis Beaudoin	Piers Dawe	Robert Grow
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Michael Bennett	Wael Diab	Takehiro Hayashi
Vipul Bhatt	Eric DiBiaso	Yasuo Hidaka
William Bliss	John Dillard	Rita Horner
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Martin Bouda	Thuyen Dinh	Victor Hou
Ralf-Peter Braun	Curtis Donahue	Yasuhiro Hyakutake
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Clark Carty	James Fife	Yasuaki Kawatsu
Craig Chabot	Alan Flatman	Michael Kelsen
Geoffrey Chacon Simon	Matthias Fritsche	Scott Kipp
Mandeep Chadha	Richard Frosch	Michael Klempa

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Curtis Knittle
Shigeru Kobayashi
Daniel Koehler
Paul Kolesar
Tom Kolze
Glen Kramer
Hans Lackner
Jeffrey Lapak
Mark Laubach
Han Hyub Lee
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Dekun Liu
Hai-Feng Liu
William Lo
Miklos Lukacs
Kent Lusted
Jeffery Maki
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Introduction

This introduction is not part of IEEE Std 802.3bs-2017, IEEE Standard for Ethernet—Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the publication date of IEEE Std 802.3bs-2017, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between

stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw™-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by™-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq™-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp™-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br™-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn™-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

IEEE Std 802.3bz™-2016

Amendment 7—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bu™-2016

Amendment 8—This amendment includes changes to IEEE Std 802.3-2015 to define a methodology for the provision of power via a single twisted pair to connected Data Terminal Equipment (DTE) with IEEE 802.3 single twisted-pair interfaces.

IEEE Std 802.3bv™-2017

Amendment 9—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 115 and Annex 115A. This amendment adds point-to-point 1000 Mb/s Physical Layer (PHY) specifications and management parameters for operation on duplex plastic optical fiber (POF) targeting use in automotive, industrial, home-network, and other applications.

IEEE Std 802.3™-2015/Cor 1-2017

This corrigendum clarifies which lane of the media dependent interface (MDI) of a multi-lane Physical Layer entity (PHY) is used as the timestamping reference point.

IEEE Std 802.3bs™-2017

Amendment 10—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 116 through Clause 124 and Annex 119A through Annex 120E. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 200 Gb/s and 400 Gb/s.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 10: Media Access Control Parameters, Physical Layers, and Management Parameters for 200 Gb/s and 400 Gb/s Operation

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~striketrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following compatibility interfaces after “100 Gb/s Parallel Physical Interface (CPPI)”:

- q) ***200 Gb/s Media Independent Interface (200GMII)***. The 200GMII is designed to connect a 200 Gb/s capable MAC to a 200 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 200 Gb/s speeds. The 200GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 200GMII. The 200GMII is optional.

- r) *200 Gb/s Attachment Unit Interface (200GAUI-n)*. The 200GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 200 Gb/s speeds. The 200GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8) in Annex 120B and Annex 120C, and a four-lane version (200GAUI-4) in Annex 120D and Annex 120E. No mechanical connector is specified for use with the 200GAUI-n. The 200GAUI-n is optional.
- s) *400 Gb/s Media Independent Interface (400GMII)*. The 400GMII is designed to connect a 400 Gb/s capable MAC to a 400 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 400 Gb/s speeds. The 400GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 400GMII. The 400GMII is optional.
- t) *400 Gb/s Attachment Unit Interface (400GAUI-n)*. The 400GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 400 Gb/s speeds. The 400GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16) in Annex 120B and Annex 120C, and an eight-lane version (400GAUI-8) in Annex 120D and Annex 120E. No mechanical connector is specified for use with the 400GAUI-n. The 400GAUI-n is optional.

1.3 Normative references

Insert the following references in alphanumeric order:

ANSI/TIA-604-18:2015, FOCIS 18—Fiber Optic Connector Intermateability Standard—Type MPO-16

IEC 61753-021-2:2007, Fibre optic interconnecting devices and passive components performance standard—Part 021-2: Grade C/3 single-mode fibre optic connectors for category C—Controlled environment.

Change the reference for IEC 60793-2-10 as follows:

IEC 60793-2-10:2014, Optical fibres—Part 2-10: Product specifications—Sectional specification for category A1 multimode fibres.

1.4 Definitions

Insert the following 17 new definitions into the list after 1.4.72a 40GBASE-T (as inserted by IEEE Std 802.3bq-2016):

1.4.72b 200GBASE-DR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 121.)

1.4.72c 200GBASE-FR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 122.)

1.4.72d 200GBASE-LR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding and 4-level pulse amplitude modulation over four WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 122.)

1.4.72e 200GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 119 for 200 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

1.4.72f 200 Gb/s Attachment Unit Interface (200GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 200 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of 200GAUI-n are defined: an eight-lane version (200GAUI-8), and a four-lane version (200GAUI-4). (See IEEE Std 802.3, Annex 120B and Annex 120C for 200GAUI-8, or Annex 120D and Annex 120E for 200GAUI-4.)

1.4.72g 200 Gb/s Media Independent Interface (200GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 200 Gb/s operation. (See IEEE Std 802.3, Clause 117.)

1.4.72h 200GMII Extender: The 200 Gb/s Media Independent Interface Extender extends the reach of the 200GMII and consists of two 200GXS sublayers with a 200GAUI-n between them. (See IEEE Std 802.3, Clause 118.)

1.4.72i 200GXS: The 200 Gb/s Extender Sublayer (200GXS) is part of the 200GMII Extender. In functionality, it is almost identical to the 200GBASE-R PCS Sublayer defined in Clause 119. Two types of 200GXS are defined: the DTE 200GXS adjacent to the RS sublayer and the PHY 200GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 118.)

1.4.72j 400GBASE-DR4: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over four lanes of single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 124.)

1.4.72k 400GBASE-FR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over eight WDM lanes on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 122.)

1.4.72l 400GBASE-LR8: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding and 4-level pulse amplitude modulation over eight WDM lanes on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 122.)

1.4.72m 400GBASE-R: An IEEE 802.3 family of Physical Layer devices using the physical coding sublayer defined in Clause 119 for 400 Gb/s operation. (See IEEE Std 802.3, Clause 119.)

1.4.72n 400GBASE-SR16: IEEE 802.3 Physical Layer specification for 400 Gb/s using 400GBASE-R encoding over sixteen lanes of multimode fiber, with reach up to at least 100 m. (See IEEE Std 802.3, Clause 123.)

1.4.72o 400 Gb/s Attachment Unit Interface (400GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 400 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Two widths of 400GAUI-n are defined: a sixteen-lane version (400GAUI-16), and an eight-lane version (400GAUI-8). (See IEEE Std 802.3, Annex 120B and Annex 120C for 400GAUI-16, or Annex 120D and Annex 120E for 400GAUI-8.)

1.4.72p 400 Gb/s Media Independent Interface (400GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 400 Gb/s operation. (See IEEE Std 802.3, Clause 117.)

1.4.72q 400GMII Extender: The 400 Gb/s Media Independent Interface Extender extends the reach of the 400GMII and consists of two 400GXS sublayers with a 400GAUI-n between them. (See IEEE Std 802.3, Clause 118.)

1.4.72r 400GXS: The 400 Gb/s Extender Sublayer (400GXS) is part of the 400GMII Extender. In functionality, it is almost identical to the 400GBASE-R PCS Sublayer defined in Clause 119. Two types of 400GXS are defined: the DTE 400GXS adjacent to the RS sublayer and the PHY 400GXS adjacent to the PHY. (See IEEE Std 802.3, Clause 118.)

Change 1.4.107 (as modified by IEEE Std 802.3by-2016) as follows:

1.4.107 BASE-R: An IEEE 802.3 family of Physical Layer devices using the 64B/66B encoding defined in Clause 49, Clause 82, ~~or~~ Clause 107, or Clause 119. (See IEEE Std 802.3, Clause 49, Clause 82, ~~or~~ Clause 107, or Clause 119.)

Change 1.4.325 as follows:

1.4.325 PCS lane (PCSL): In 40GBASE-R, ~~and~~ 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes, these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83 and Clause 120.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

200GAUI-n	200 Gb/s Attachment Unit Interface over n lanes
200GMII	200 Gb/s Media Independent Interface
200GXS	200GMII Extender Sublayer
400GAUI-n	400 Gb/s Attachment Unit Interface over n lanes
400GMII	400 Gb/s Media Independent Interface
400GXS	400GMII Extender Sublayer
SER	symbol error ratio

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4-2 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bz-2016) as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, and 100 Gb/s, <u>200 Gb/s, and 400 Gb/s</u>	10 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap ^a	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

^a References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 below Table 4-2 as follows:

NOTE 7—For 40 Gb/s, ~~and 100 Gb/s, 200 Gb/s, and 400 Gb/s~~ operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, ~~or CGMII, 200GMII, or 400GMII~~ receive signals at the DTE due to clock tolerance and lane alignment requirements.

30. Management

30.2 Managed objects

30.2.5 Capabilities

Insert two new rows between the rows for `aRSFECIndicationEnable` and `aSNROpMarginChnlA` in Table 30-1e (as modified by IEEE Std 802.3bq-2016) as follows (unchanged rows not shown):

Table 30-1e—Capabilities

			DTE	Repeater	MAU	
			Basic Package (mandatory)			
			Mandatory Package (mandatory)			
			Recommended Package (optional)			
			Optional Package (optional)			
			Array Package (optional)			
			Excessive Deferral Package (optional)			
			Multiple PHY Package (optional)			
			PHY Error Monitor Capability (optional)			
			Basic Control Capability (mandatory)			
			Performance Monitor Capability (optional)			
			Address Tracking Capability (optional)			
			100/1000 Mb/s Monitor Capability (optional)			
			1000 Mb/s Burst Monitor Capability (optional)			
			Basic Package (mandatory)			
			MAU Control Package (optional)			
			Media Loss Tracking Package (conditional)			
			Broadband DTE MAU Package (conditional)			
			MLT Capability (conditional)			
			PHY Error Monitor Capability (optional)			
			Multigigabit-T Operating Margin package (conditional)			
			Forward Error Correction Package (conditional)			
			Energy-Efficient Ethernet (optional)			
			Auto-Negotiation Package (mandatory)			
...						
<code>aPCSFECIndicationAbility</code>	ATTRIBUTE	GET				X
<code>aPCSFECIndicationEnable</code>	ATTRIBUTE	GET-SET				X
...						

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert 200GBASE-R and 400GBASE-R PHY types at the end of “APPROPRIATE SYNTAX” section of 30.3.2.1.2 as follows:

APPROPRIATE SYNTAX:

...	
200GBASE-R	Clause 119 200 Gb/s multi-PCS lane 64B/66B
400GBASE-R	Clause 119 400 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert 200GBASE-R and 400GBASE-R PHY types at the end of “APPROPRIATE SYNTAX” section of 30.3.2.1.3 as follows:

APPROPRIATE SYNTAX:

...	
200GBASE-R	Clause 119 200 Gb/s multi-PCS lane 64B/66B
400GBASE-R	Clause 119 400 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph of the “BEHAVIOUR DEFINED AS” section of 30.3.2.1.5 (as modified by IEEE Std 802.3by-2016) as follows:

BEHAVIOUR DEFINED AS:

For operation at 10 Gb/s, 25 Gb/s, 40 Gb/s, ~~and 100 Gb/s, 200 Gb/s, and 400 Gb/s~~, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the media independent interface (see Table 46–4 and Table 81–3).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert new MAU types immediately above 802.9a in “APPROPRIATE SYNTAX” section of 30.5.1.1.2 as follows:

APPROPRIATE SYNTAX:

...	
200GBASE-R	Multi-lane PCS as specified in Clause 119 over undefined PMA/PMD
200GBASE-DR4	200GBASE-R PCS/PMA over 4-lane single-mode fiber PMD as specified in Clause 121
200GBASE-FR4	200GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 122
200GBASE-LR4	200GBASE-R PCS/PMA over 4 WDM lane single-mode fiber PMD with reach up to at least 10 km as specified in Clause 122
400GBASE-R	Multi-lane PCS as specified in Clause 119 over undefined PMA/PMD
400GBASE-SR16	400GBASE-R PCS/PMA over 16-lane multimode fiber PMD as specified in Clause 123
400GBASE-DR4	400GBASE-R PCS/PMA over 4-lane single-mode fiber PMD as specified in Clause 124
400GBASE-FR8	400GBASE-R PCS/PMA over 8 WDM lane single-mode fiber PMD with reach up to at least 2 km as specified in Clause 122
400GBASE-LR8	400GBASE-R PCS/PMA over 8 WDM lane single-mode fiber PMD with reach up to at least 10 km as specified in Clause 122
...	

Change the last paragraph of the “BEHAVIOUR DEFINED AS” section of 30.5.1.1.2 (as modified by IEEE Std 802.3by-2016) as follows:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, ~~and 100GBASE-R, 200GBASE-R, and 400GBASE-R~~ shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of the “BEHAVIOUR DEFINED AS” section of 30.5.1.1.4 (as modified by IEEE Std 802.3bq-2016) as follows:

For 40 Gb/s, ~~and 100 Gb/s, 200 Gb/s, and 400 Gb/s~~, the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault.”

30.5.1.1.12 aLaneMapping

Change 30.5.1.1.12 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of INTEGERS.

BEHAVIOUR DEFINED AS:

For 40/100/~~200/400~~GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers. The indices of this array (0 to n – 1) denote the service interface lane number where n is the number of PCS lanes in use. Each element of this array contains the PCS lane number for the PCS lane that has been detected in the corresponding service interface lane.

If a Clause 45 MDIO Interface to the PCS is present, then this attribute will map to the Lane mapping registers (see 45.2.3.46 and 45.2.3.47).;

30.5.1.1.15 aFECAbility

Change 30.5.1.1.15 (as modified by IEEE Std 802.3by-2016) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below

unknown	initializing, true state not yet known
supported	FEC supported
not supported	FEC not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports ~~a FEC sublayer for~~ forward error correction (see 65.2, Clause 74, Clause 91, ~~and~~ Clause 108, and Clause 119).

If a Clause 45 MDIO Interface is present and support for FEC is optional, then this attribute maps to the FEC capability register (see 45.2.8.2 or 45.2.1.92).;

30.5.1.1.17 aFECCorrectedBlocks

Change 30.5.1.1.17 (as modified by IEEE Std 802.3by-2016) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, ~~and 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.~~

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for ~~all multiple FEC lanes.~~ Each element of this array contains a count of corrected FEC blocks for that FEC sublayer instance.

Increment the counter by one for each received block that is corrected by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC corrected blocks counter(s) (see 45.2.8.5 and 45.2.1.94 for 10GBASE-R, 45.2.3.39 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.116 for BASE-R, ~~and 45.2.1.103 for RS-FEC, and 45.2.3.471 for PCS FEC).~~;

30.5.1.1.18 aFECUncorrectableBlocks

Change 30.5.1.1.18 (as modified by IEEE Std 802.3by-2016) as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, ~~and 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.~~

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters. The counters do not increment for other PHY types. The indices of this array (0 to N – 1) denote the FEC sublayer instance number where N is the number of FEC sublayer instances in use. The number of FEC sublayer instances in use is set to one for PHYs that do not use PCS lanes or use a single FEC instance for ~~all multiple FEC lanes.~~ Each element of this array contains a count of uncorrectable ~~corrected~~ FEC blocks for that FEC sublayer instance.

Increment the counter by one for each FEC block that is determined to be uncorrectable by the FEC function in the PHY for the corresponding lane or FEC sublayer instance.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC uncorrectable blocks counter(s) (see 45.2.8.6 and 45.2.1.95 for 10GBASE-R, 45.2.3.40 for 10GBASE-PR and 10/1GBASE-PRX, 45.2.1.117 for BASE-R, ~~and 45.2.1.104 for RS-FEC,~~ and 45.2.3.47m for PCS FEC).;

Insert 30.5.1.1.32 and 30.5.1.1.33 after 30.5.1.1.31 as follows:

30.5.1.1.32 aPCSFECIndicationAbility

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
supported	PCS FEC error indication bypass ability supported
not supported	PCS FEC error indication bypass ability not supported

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional PCS FEC error indication bypass ability (see 119.2.5.3).

If a Clause 45 MDIO Interface is present, then this attribute maps to the PCS FEC status register (see 45.2.3.47k).;

30.5.1.1.33 aPCSFECIndicationEnable

ATTRIBUTE

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the following description:

unknown	initializing, true state not yet known
disabled	PCS FEC error indication bypass disabled
enabled	PCS FEC error indication bypass enabled

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the PCS FEC error indication bypass function (see 119.2.5.3).

A GET operation returns the current mode of operation of the PCS FEC. A SET operation changes the mode of operation of the PCS FEC to the indicated value.

If a Clause 45 MDIO Interface is present, then this attribute maps to the RS-FEC control register (see 45.2.3.47j).;

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the first sentence of 45.2.1 (as modified by IEEE Std 802.3by-2016) as follows:

For devices operating at 25 Gb/s or higher speeds, the PMA may be instantiated as multiple sublayers (see 83.1.4, ~~and 109.1.4,~~ and 120.1.4 for how MMD addresses are allocated to multiple PMA sublayers for the respective speeds).

Change the reserved row for 1.23 through 1.29 in Table 45-3 (as modified by IEEE Std 802.3bv-2017) as follows (unchanged rows not shown):

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
...		
<u>1.23</u>	<u>200G PMA/PMD extended ability</u>	<u>45.2.1.14e</u>
<u>1.24</u>	<u>400G PMA/PMD extended ability</u>	<u>45.2.1.14f</u>
<u>1.25, 1.26</u>	<u>Reserved</u>	
<u>1.27</u>	<u>PMD transmit disable extension</u>	<u>45.2.1.14g</u>
<u>1.28</u>	<u>PMD receive signal detect extension</u>	<u>45.2.1.14h</u>
1.23 through 1.29	Reserved	
...		

Change the reserved row for 1.340 through 1.699 in Table 45-3 as follows (unchanged rows not shown):

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.340 through 1.399 699	Reserved	
1.400 through 1.407	<u>200GAUI-8 and 400GAUI-16 chip-to-module recommended CTLE, lane 0 through lane 7</u>	<u>45.2.1.116a</u> , <u>45.2.1.116b</u>
1.408 through 1.415	<u>400GAUI-16 chip-to-module recommended CTLE, lane 8 through lane 15</u>	<u>45.2.1.116c</u>
1.416 through 1.499	Reserved	
1.500 through 1.515	<u>200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15</u>	<u>45.2.1.116d</u> , <u>45.2.1.116e</u>
1.516 through 1.531	<u>200GAUI-n and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15</u>	<u>45.2.1.116f</u> , <u>45.2.1.116g</u>
1.532 through 1.699	Reserved	
...		

Change the reserved row for 1.1511 through 1.1599 in Table 45-3 as follows (unchanged rows not shown):

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.1511 through 1.1599	Reserved	
1.1512	<u>PRBS13Q testing control</u>	<u>45.2.1.125a</u>
1.1513 through 1.1599	Reserved	
...		

Change the rows for 1.1600 through 1.1799 in Table 45-3 as follows (unchanged rows not shown):

Table 45-3—PMA/PMD registers

Register address	Register name	Subclause
...		
1.1600 through 1.161 509	PRBS Tx error counters, lane 0 through lane 159	45.2.1.126
1.161 60 through 1.1699	Reserved	
1.1700 through 1.171 509	PRBS Rx error counters, lane 0 through lane 159	45.2.1.127
1.171 60 through 1.1799	Reserved	
...		

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the row for bits 1.0.5:2 in Table 45-4 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45-4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.0.5:2	Speed selection	5 4 3 2 1 * * * = Reserved 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = Reserved 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
...			

^a R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bz-2016) as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

45.2.1.1.4 PMA remote loopback (1.0.1)

Change the last two sentences of the second paragraph of 45.2.1.1.4 as follows:

~~For 40/100 Gb/s operation, the remote loopback functionality is detailed in 83.5.9. For 25/40/100 Gb/s operation, the remote loopback ability bit is specified in register 1.13 the 40G/100G PMA/PMD extended ability register. For 200 Gb/s and 400 Gb/s operation, the remote loopback ability bit is specified in registers 1.23 and 1.24, respectively.~~

45.2.1.1.5 PMA local loopback (1.0.0)

Change the second paragraph of 45.2.1.1.5 as follows:

The local loopback function is mandatory for the 1000BASE-KX, 10GBASE-KR, 10GBASE-X, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 port type and optional for all other port types, except 2BASE-TL, 10PASS-TS, and 10/1GBASE-PRX, which do not support loopback. ~~A device's ability to perform the local loopback function is advertised in the local loopback ability bit of the related speed-dependent status register. A PMA that is unable to perform the local loopback function shall ignore writes to this bit and shall return a value of zero when read. For 10 Gb/s operation, the~~ The local loopback functionality is detailed in the relevant PMA clause 48.3.3 and 51.8. For 40/100 Gb/s operation, the local loopback functionality is detailed in 83.5.8. For 10/25/40/100/200/400 Gb/s operation, the local loopback ability bit is specified in the PMA/PMD status 2 register.

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 (as modified by IEEE Std 802.3by-2016) as follows:

For 10/25/40/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the reserved rows of Table 45–6 (as modified by IEEE Std 802.3bz-2016) as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.4.15	Reserved for future speeds- 400G capable	Value always 0 1 = PMA/PMD is capable of operating at 400 Gb/s 0 = PMA/PMD is not capable of operating at 400 Gb/s	RO
...			
1.4.12	Reserved for future speeds- 200G capable	Value always 0 1 = PMA/PMD is capable of operating at 200 Gb/s 0 = PMA/PMD is not capable of operating at 200 Gb/s	RO
...			

^a RO = Read only

Insert 45.2.1.4.aaa before 45.2.1.4.aa (as inserted by IEEE Std 802.3bz-2016) as follows:

45.2.1.4.aaa 400G capable (1.4.15)

When read as a one, bit 1.4.15 indicates that the PMA/PMD is able to operate at a data rate of 400 Gb/s. When read as a zero, bit 1.4.15 indicates that the PMA/PMD is not able to operate at a data rate of 400 Gb/s.

Insert 45.2.1.4.ac after 45.2.1.4.ab (as inserted by IEEE Std 802.3bz-2016) and before 45.2.1.4.a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.4.ac 200G capable (1.4.12)

When read as a one, bit 1.4.12 indicates that the PMA/PMD is able to operate at a data rate of 200 Gb/s. When read as a zero, bit 1.4.12 indicates that the PMA/PMD is not able to operate at a data rate of 200 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45–7 (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, IEEE Std 802.3bp-2016, IEEE Std 802.3bn-2016, IEEE Std 802.3bz-2016, and IEEE Std 802.3bv-2017) as follows:

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.15:10	Reserved	Value always 0	RO
1.7.9	PIASE	PMA ingress AUI stop enable	R/W
1.7.8	PEASE	PMA egress AUI stop enable	R/W

Table 45–7—PMA/PMD control 2 register bit definitions (*continued*)

Bit(s)	Name	Description	R/W ^a
1.7.7:6 <u>1.7.7</u>	Reserved	Value always 0	RO
1.7.5:0 <u>1.7.6:0</u>	PMA/PMD type selection	<u>6 5 4 3 2 1 0</u> <u>1 1 x x x x = reserved</u> <u>1 0 1 1 1 1 x = reserved</u> <u>1 0 1 1 1 0 1 = reserved</u> <u>1 0 1 1 1 0 0 = 400GBASE-LR8 PMA/PMD</u> <u>1 0 1 1 0 1 1 = 400GBASE-FR8 PMA/PMD</u> <u>1 0 1 1 0 1 0 = 400GBASE-DR4 PMA/PMD</u> <u>1 0 1 1 0 0 1 = 400GBASE-SR16 PMA/PMD</u> <u>1 0 1 1 0 0 0 = reserved</u> <u>1 0 1 0 1 1 x = reserved</u> <u>1 0 1 0 1 0 1 = 200GBASE-LR4 PMA/PMD</u> <u>1 0 1 0 1 0 0 = 200GBASE-FR4 PMA/PMD</u> <u>1 0 1 0 0 1 1 = 200GBASE-DR4 PMA/PMD</u> <u>1 0 1 0 0 1 0 = reserved</u> <u>1 0 1 0 0 0 x = reserved</u> <u>1 0 0 x x x x = reserved</u> <u>0 1 1 1 1 1 x = reserved</u> <u>0 1 1 1 1 0 1 = BASE-T1 PMA/PMD^b</u> <u>0 1 1 1 1 0 0 = reserved</u> <u>0 1 1 1 0 1 1 = reserved</u> <u>0 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD</u> <u>0 1 1 1 0 0 1 = 25GBASE-KR or 25GBASE-KR-S PMA/PMD</u> <u>0 1 1 1 0 0 0 = 25GBASE-CR or 25GBASE-CR-S PMA/PMD</u> <u>0 1 1 0 1 1 1 = 25GBASE-T PMA</u> <u>0 1 1 0 1 1 0 = reserved</u> <u>0 1 1 0 1 0 1 = reserved</u> <u>0 1 1 0 1 0 0 = BASE-H PMA/PMD^c</u> <u>0 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD</u> <u>0 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD</u> <u>0 1 1 0 0 0 1 = 5GBASE-T PMA</u> <u>0 1 1 0 0 0 0 = 2.5GBASE-T PMA</u> <u>0 1 0 1 1 1 1 = 100GBASE-SR4 PMA/PMD</u> <u>0 1 0 1 1 1 0 = 100GBASE-CR4 PMA/PMD</u> <u>0 1 0 1 1 0 1 = 100GBASE-KR4 PMA/PMD</u> <u>0 1 0 1 1 0 0 = 100GBASE-KP4 PMA/PMD</u> <u>0 1 0 1 0 1 1 = 100GBASE-ER4 PMA/PMD</u> <u>0 1 0 1 0 1 0 = 100GBASE-LR4 PMA/PMD</u> <u>0 1 0 1 0 0 1 = 100GBASE-SR10 PMA/PMD</u> <u>0 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD</u> <u>0 1 0 0 1 1 1 = reserved</u>	R/W