
**Information technology —
Telecommunications and information
exchange between systems — Local
and metropolitan area networks —
Specific requirements —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 2: Media access control
parameters, physical layers, and
management parameters for 25 Gb/s
operation**

*Technologies de l'information — Télécommunications et échange
d'information entre systèmes — Réseaux locaux et métropolitains —
Prescriptions spécifiques —*

Partie 3: Norme pour Ethernet

*AMENDEMENT 2: Paramètres de contrôle d'accès au support, couches
physiques et paramètres de gestion pour l'exploitation des interfaces
à 25 Go/s*



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IEEE 802.3by™-2016
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015)

IEEE Standard for Ethernet

Amendment 2: Media Access Control Parameters, Physical Layers, and Management Parameters for 25 Gb/s Operation

Sponsor

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 30 June 2016

IEEE-SA Standards Board

Abstract: This amendment to IEEE Std 802.3-2015 adds Physical Layer (PHY) specifications and management parameters for 25 Gb/s operation over twinaxial copper cabling (25GBASE-CR and 25GBASE-CR-S), electrical backplanes (25GBASE-KR and 25GBASE-KR-S), and multimode fiber (25GBASE-SR). This amendment also specifies a 25 Gigabit Attachment Unit Interface (25GAUI) and optional Energy Efficient Ethernet (EEE).

Keywords: 25 Gigabit Ethernet, 25GAUI, 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, 25GBASE-KR-S, 25GBASE-SR, 25GMII, Auto-Negotiation (AN), Backplane Ethernet, Energy Efficient Ethernet (EEE), Ethernet, Forward Error Correction (FEC), IEEE 802®, IEEE 802.3™, IEEE 802.3by™, multimode fiber (MMF), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, Physical Medium Dependent (PMD) sublayer, Reconciliation Sublayer (RS)

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Introduction

This introduction is not part of IEEE Std 802.3by™-2016, IEEE Standard for Ethernet—Amendment 2: Media Access Control Parameters, Physical Layers, and Management Parameters for 25 Gb/s Operation.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel, and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile), and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3by-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats, and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted-pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 2: Media Access Control Parameters, Physical Layers, and Management Parameters for 25 Gb/s Operation

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(This amendment is based on IEEE Std 802.3™-2015 as amended by IEEE 802.3bw™-2015.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in **bold italic**. Four editing instructions are used: change, delete, insert, and replace. **Change** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underline (to add new material). **Delete** removes existing material. **Insert** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. **Replace** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.¹

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in **green**.

¹Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following compatibility interface definitions after item h) in the lettered list:

- i) **25 Gigabit Media Independent Interface (25GMII).** The 25GMII is designed to connect a 25 Gb/s capable MAC to a 25 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 25 Gb/s speeds. The 25GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 25GMII. The 25GMII is optional.
- j) **25 Gigabit Attachment Unit Interface (25GAUI).** The 25GAUI is a physical instantiation of the PMA service interface to extend the connection between 25 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 25 Gb/s speeds. The 25GAUI is intended for use as a chip-to-chip or a chip-to-module interface. No mechanical connector is specified for use with the 25GAUI. The 25GAUI is optional.

1.3 Normative references

Insert the following references in alphanumeric order:

SFF-8402, Rev 1.1, September 13, 2014, Specification for SFP+ 1X 28 Gb/s Pluggable Transceiver Solution (SFP28).²

SFF-8432, Rev 5.1, August 8, 2012, Specification for SFP+ Module and Cage.

SFF-8665, Rev 1.9, June 29, 2015, Specification for QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28).

Remove the footnote number from the SFF-8436 reference as shown:

SFF-8436, Rev 4.1, August 24, 2011, Specification for QSFP+ 10 Gbs 4X Pluggable Transceiver.¹⁹

1.4 Definitions

Insert the following new definitions into the list after 1.4.64 10/10G-EPON:

1.4.64a 25GBASE: A family of Physical Layer entities for 25 Gb/s operation. (See IEEE Std 802.3, Clause 105.)

1.4.64b 25GBASE-CR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over one lane of twinaxial copper cable. (See IEEE Std 802.3, Clause 110.)

²SFF specifications are available at <ftp://ftp.seagate.com/sff>.

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1.4.64c 25GBASE-CR-S: IEEE 802.3 Physical Layer specification equivalent to 25GBASE-CR without support for the RS-FEC sublayer specified in Clause 108. (See IEEE Std 802.3, Clause 110.)

1.4.64d 25GBASE-KR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 111.)

1.4.64e 25GBASE-KR-S: IEEE 802.3 Physical Layer specification equivalent to 25GBASE-KR without support for the RS-FEC sublayer specified in Clause 108. (See IEEE Std 802.3, Clause 111.)

1.4.64f 25GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 25 Gb/s operation. (See IEEE Std 802.3, Clause 107.)

1.4.64g 25GBASE-SR: IEEE 802.3 Physical Layer specification for 25 Gb/s using 25GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 112.)

Insert the following new definitions into the list after 1.4.77 10 Gigabit Sixteen-Bit Interface (XSBI):

1.4.77a 25 Gigabit Attachment Unit Interface (25GAUI): A physical instantiation of the Physical Medium Attachment (PMA) service interface to extend the connection between 25 Gb/s capable PMAs over one lane, used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Annex 109A and Annex 109B.)

1.4.77b 25 Gigabit Media Independent Interface (25GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 25 Gb/s operation. (See IEEE Std 802.3, Clause 106.)

Change 1.4.107 as follows.

1.4.107 BASE-R: An IEEE 802.3 family of Physical Layer devices using the 64B/66B encoding defined in Clause 49, or Clause 82, or Clause 107. (See IEEE Std 802.3, Clause 49, and Clause 82, or Clause 107.)

Change 1.4.134 as follows:

1.4.134 channel: In 10BROAD36, a band of frequencies dedicated to a certain service transmitted on the broadband medium. Otherwise, a defined path along which data in the form of an electrical or optical signal passes. (For 10BROAD36, See IEEE Std 802.3, Clause 11.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

25GAUI	25 Gigabit Attachment Unit Interface
25GMII	25 Gigabit Media Independent Interface
C2C	chip-to-chip
C2M	chip-to-module

4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 to add 25 Gb/s as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	1 Gb/s	10 Gb/s	25 Gb/s, 40 Gb/s, and 100 Gb/s
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap ^a	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	104 bits	not applicable

^aReferences to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 4 as follows:

NOTE 4—For 10 Gb/s and 25 Gb/s operation, the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 40 BT (bit times), as measured at the XGMII or 25GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays and clock tolerances.

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in APPROPRIATE SYNTAX before the entry for 40GBASE-R in 30.3.2.1.2:

APPROPRIATE SYNTAX:

...
 25GBASE-R Clause 107 25 Gb/s 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry in APPROPRIATE SYNTAX before the entry for 40GBASE-R in 30.3.2.1.3:

APPROPRIATE SYNTAX:

...
 25GBASE-R Clause 107 25 Gb/s 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph in BEHAVIOUR DEFINED AS in 30.3.2.1.5 as follows:

BEHAVIOUR DEFINED AS:

For operation at 10 Gb/s, 25 Gb/s, 40 Gb/s, and 100 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate “Receive Error” on the media independent interface XGMII (see Table 46-4 and Table 81-3), the XLGMII, or the CGMII (see Table 81-3).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in APPROPRIATE SYNTAX before the entry for 40GBASE-R in 30.5.1.1.2:

APPROPRIATE SYNTAX:

...

25GBASE-R	PCS as specified in Clause 107 with PMA as specified in Clause 109 over undefined PMD
25GBASE-CR	25GBASE-R PCS/PMA over shielded balanced copper cable PMD as specified in Clause 110
25GBASE-CR-S	25GBASE-R PCS/PMA over shielded balanced copper cable PMD as specified in Clause 110 without support for RS-FEC
25GBASE-KR	25GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 111
25GBASE-KR-S	25GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 111 without support for RS-FEC
25GBASE-SR	25GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 112

...

Change BEHAVIOUR DEFINED AS in 30.5.1.1.2 as follows:

BEHAVIOUR DEFINED AS:

Returns a value that identifies the internal MAU type. If an AUI is to be identified to access an external MAU, the type “AUI” is returned. A SET operation to one of the possible enumerations indicated by aMAUTypeList will force the MAU into the new operating mode. If a [Clause 22](#) MII or [Clause 35](#) GMII is present, then this will map to the mode force bits specified in [22.2.4.1](#). If a [Clause 45](#) MDIO Interface is present, then this will map to the PCS type selection bit(s) in the 10G WIS Control 2 register specified in [45.2.2.6.6](#), the PCS Control 2 register specified in [45.2.3.6.1](#), the PMA/PMD type selection bits in the PMA/PMD Control 2 register specified in [45.2.1.6](#), the PMA/PMD control 1 register specified in [45.2.1.1](#), the 25G RS-FEC Enable bit in the RS-FEC control register specified in [45.2.1.101.a](#), and the PCS control 1 register [45.2.3.1](#). If [Clause 28](#), [Clause 37](#), or [Clause 73](#) Auto-Negotiation is operational, then this will change the advertised ability to the single enumeration specified in the SET operation, and cause an immediate link renegotiation. A change in the MAU type will also be reflected in aPHYType.

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, and 100GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable**Change the first sentence of the eighth paragraph in BEHAVIOUR DEFINED AS in 30.5.1.1.4 as follows:**

BEHAVIOUR DEFINED AS:

For 10 Gb/s and 25 Gb/s the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram ([Figure 46–11](#)) as follows: the value OK maps to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”.

30.5.1.1.15 aFECAbility**Change the first sentence of BEHAVIOUR DEFINED AS in 30.5.1.1.15 as follows:**

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an ~~optional~~ FEC sublayer for forward error correction (see ~~65.2, and Clause 74, Clause 91, and Clause 108~~) ~~or supports the Clause 91-mandatory RS-FEC.~~

30.5.1.1.16 aFECMode

Change APPROPRIATE SYNTAX in 30.5.1.1.16 as follows:

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that meets the requirement of the description below	
unknown	initializing, true state not yet known
disabled	FEC disabled
<u>BASE-R enabled</u>	<u>BASE-R FEC enabled</u>
<u>RS-FEC enabled</u>	<u>RS-FEC enabled</u>
enabled	FEC enabled

Change BEHAVIOUR DEFINED AS in 30.5.1.1.16 as follows:

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the ~~optional~~ FEC sublayer for forward error correction (see ~~65.2, and Clause 74, Clause 91, and Clause 108~~).

A GET operation returns the current mode of operation of the PHY. A SET operation changes the mode of operation of the PHY to the indicated value. The enumerations “BASE-R enabled” and “RS-FEC enabled” are only used for 25GBASE-CR, 25GBASE-CR-S, 25GBASE-KR, and 25GBASE-KR-S PHYs where operation in the no-FEC mode maps to the enumerations “disabled”, operation in the BASE-R FEC mode maps to the enumerations “BASE-R enabled”, and operation in the RS-FEC mode maps to the enumerations “RS-FEC enabled” (see 110.6 and 111.6).

When Clause 73 Auto-Negotiation is enabled for a 25GBASE-R PHY, a SET operation is not allowed and a GET operation maps to the variables FEC_enable in Clause 74 and FEC_enable in Clause 108. When Clause 73 Auto-Negotiation is enabled for a non-25GBASE-R PHY supporting Clause 74 FEC a SET operation is not allowed and a GET operation maps to the variable FEC_enable in Clause 74.

If a Clause 45 MDIO Interface is present, then this attribute maps to the FEC control register (see 45.2.8.3) for 1000BASE-PX, to the BASE-R FEC control register (see 45.2.1.93) and the 25G RS-FEC Enable bit in the RS-FEC control register (see 45.2.1.101) for 25GBASE-R, or FEC enable bit in BASE-R FEC control register (see 45.2.1.93).;

30.5.1.1.17 aFECCorrectedBlocks

Change APPROPRIATE SYNTAX in 30.5.1.1.17 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

Change the first sentence of BEHAVIOUR DEFINED AS in 30.5.1.1.17 as follows:

BEHAVIOUR DEFINED AS:

IEEE Std 802.3by-2016
IEEE Standard for Ethernet—Amendment 2: Media Access Control Parameters,
Physical Layers, and Management Parameters for 25 Gb/s Operation

For 1000BASE-PX, 10/25/40/100GBASE-R, 100GBASE-P, 10GBASE-PR, or
10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change APPROPRIATE SYNTAX in 30.5.1.1.18 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, and 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, and 2 500 000 counts per second for 100 Gb/s implementations.

Change the first sentence of BEHAVIOUR DEFINED AS in 30.5.1.1.18 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/100GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert 25GR-S and 25GR after 10GBASE-KRFD, and RS-FEC25G Req and BASE-RFEC25G Req after FEC Requested in APPROPRIATE SYNTAX, in 30.6.1.1.5 as follows:

APPROPRIATE SYNTAX:

25GR-S	25GBASE-CR-S as specified in Clause 110 or 25GBASE-KR-S as specified in Clause 111
25GR	25GBASE-CR as specified in Clause 110 or 25GBASE-KR as specified in Clause 111
RS-FEC25G Req	25G RS-FEC requested as specified in Clause 73 (see 73.6.5) and Clause 108
BASE-RFEC25G Req	25G BASE-R FEC requested as specified in Clause 73 (see 73.6.5) and Clause 74

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the first sentence of 45.2.1 as follows:

For devices operating at 25 ~~40~~-Gb/s or higher speeds, the PMA may be instantiated as multiple sublayers (see 83.1.4 ~~and~~ 109.1.4 for how MMD addresses are allocated to multiple PMA sublayers).

Change the identified reserved row in Table 45–3 (as modified by IEEE Std 802.3bw-2015) and insert a new row immediately above the changed row as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
<u>1.19</u>	<u>25G PMA/PMD extended ability</u>	45.2.1.14b
1.19 <u>20</u> through 1.29	Reserved	

Change the rows in Table 45–3 for registers 1.172 through 1.175 and 1.179 through 1.187 (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.172 through 1.173	<u>Single-lane PHY 40GBASE-R FEC corrected blocks counter</u>	45.2.1.94
1.174 through 1.175	<u>Single-lane PHY 40GBASE-R FEC uncorrected blocks counter</u>	45.2.1.95
1.179	CAUI-4 chip-to-module C2M and 25GAUI C2M recommended CTLE	45.2.1.96
<u>1.180</u>	<u>25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, receive direction</u>	<u>45.2.1.97</u>
1.180 <u>181</u> through 1.183	CAUI-4 chip-to-chip transmitter equalization, receive direction, lane <u>0</u> 1 through lane 3	45.2.1.97 <u>45.2.1.98</u>
<u>1.184</u>	<u>25GAUI C2C and lane 0 CAUI-4 C2C transmitter equalization, transmit direction</u>	45.2.1.99
1.184 <u>185</u> through 1.187	CAUI-4 chip-to-chip transmitter equalization, transmit direction, lane <u>0</u> 1 through lane 3	45.2.1.99 <u>45.2.1.100</u>

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the indicated row of Table 45–4 for 25 Gb/s speed selection as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved x 1 x x = Reserved 0 1 1 x = Reserved 0 1 0 1 = Reserved <u>0 1 0 0 = 25 Gb/s</u> 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

^aR/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the first sentence of the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected.

45.2.1.2 PMA/PMD status 1 register (Register 1.1)**45.2.1.2.3 Fault (1.1.7)**

Change 45.2.1.2.3 as follows:

Fault is a global PMA/PMD variable. When read as a one, bit 1.1.7 indicates that either (or both) the PMA or the PMD has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 1.1.7 indicates that neither the PMA nor the PMD has detected a fault condition. For 10/25/40/100 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one. For 10PASS-TS or 2BASE-TL operations, when read as a one, a fault has been detected and more detailed information is conveyed in [45.2.1.19](#), [45.2.1.42](#), [45.2.1.43](#), and [45.2.1.58](#).

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the row for 1.4.15:10 in Table 45-6 as follows (unchanged rows not shown):

Table 45-6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.4.15:10 <u>1.4.15:12</u>	Reserved for future speeds	Value always 0	RO
<u>1.4.11</u>	<u>25G capable</u>	<u>1 = PMA/PMD is capable of operating at 25 Gb/s</u> <u>0 = PMA/PMD is not capable of operating at 25 Gb/s</u>	<u>RO</u>
<u>1.4.10</u>	<u>Reserved</u>	<u>Value always 0</u>	<u>RO</u>

^aRO = Read only

Insert new subclause 45.2.1.4.a before 45.2.1.4.1 as follows:

45.2.1.4.a 25G capable (1.4.11)

When read as a one, bit 1.4.11 indicates that the PMA/PMD is able to operate at a data rate of 25 Gb/s. When read as a zero, bit 1.4.11 indicates that the PMA/PMD is not able to operate at a data rate of 25 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the indicated row of Table 45-7 (as modified by IEEE Std 802.3bw-2015) for 25G PMA/PMD selection as follows (unchanged rows not shown):

Table 45-7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 1 0 x x = reserved for future use <u>1 1 1 0 1 1</u> = reserved <u>1 1 1 0 1 0</u> = 25GBASE-SR PMA/PMD <u>1 1 1 0 0 1</u> = 25GBASE-KR or 25GBASE-KR-S PMA/PMD <u>1 1 1 0 0 0</u> = 25GBASE-CR or 25GBASE-CR-S PMA/PMD	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.7 PMA/PMD status 2 register (Register 1.8)**45.2.1.7.4 Transmit fault (1.8.11)**

Insert the following rows between 10GBASE-KX4 and 40GBASE-KR4 in Table 45–9 (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
25GBASE-KR, 25GBASE-KR-S	111.7.8
25GBASE-CR, 25GBASE-CR-S	110.7.8
25GBASE-SR	112.5.8

45.2.1.7.5 Receive fault (1.8.10)

Insert the following rows between 10GBASE-KX4 and 40GBASE-KR4 in Table 45–10 (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
25GBASE-KR, 25GBASE-KR-S	111.7.9
25GBASE-CR, 25GBASE-CR-S	110.7.9
25GBASE-SR	112.5.9

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert the following rows between 10GBASE-KX4 and 40GBASE-KR4 in Table 45–12 (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
25GBASE-KR and 25GBASE-KR-S	111.7.5
25GBASE-CR and 25GBASE-CR-S	110.7.5
25GBASE-SR	112.5.6

IEEE Std 802.3by-2016
IEEE Standard for Ethernet—Amendment 2: Media Access Control Parameters,
Physical Layers, and Management Parameters for 25 Gb/s Operation

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change the row for 1.11.15:12 of Table 45–14 (as modified by IEEE Std 802.3bw-2015) as follows (unchanged rows not shown):

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.11.15:12 <u>1.11.15:13</u>	Reserved	Value always 0	RO
<u>1.11.12</u>	<u>25G extended abilities</u>	<u>1 = PMA/PMD has 25G extended abilities listed in register 1.19</u> <u>0 = PMA/PMD does not have 25G extended abilities</u>	<u>RO</u>

^aRO = Read only

Insert a new subclause 45.2.1.10.aa before 45.2.1.10.a (as inserted by IEEE Std 802.3bw-2015) as follows:

45.2.1.10.aa 25G extended abilities (1.11.12)

When read as a one, bit 1.11.12 indicates that the PMA/PMD has 25G extended abilities listed in register 1.19. When read as a zero, bit 1.11.12 indicates that the PMA/PMD does not have 25G extended abilities.

45.2.1.14 EEE capability (Register 1.16)

Change the row for 1.16.7:2 of Table 45–17 as follows (unchanged rows not shown):

Table 45–17—EEE capability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.16.7:2 <u>1.16.7:3</u>	Reserved	Value always 0	RO
<u>1.16.2</u>	<u>25GBASE-R deep sleep</u>	<u>1 = EEE deep sleep is supported for 25GBASE-R</u> <u>0 = EEE deep sleep is not supported for 25GBASE-R</u>	<u>RO</u>

^aRO = Read only

Insert new subclause 45.2.1.14.4a before 45.2.1.14.5 as follows:

45.2.1.14.4a 25GBASE-R deep sleep (1.16.2)

If the device supports EEE deep sleep operation for 25GBASE-R, bit 1.16.2 shall be set to a one; otherwise this bit is set to a zero.

Insert 45.2.1.14b and 45.2.1.14b.1 through 45.2.1.14b.5 after 45.2.1.14a as inserted by IEEE Std 802.3bw-2015 as follows:

45.2.1.14b 25G PMA/PMD extended ability register (Register 1.19)

The assignment of bits in the 25G PMA/PMD extended ability register is shown in Table 45–17b.

Table 45–17b—25G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.19.15:5	Reserved	Value always 0	RO
1.19.4	25GBASE-SR ability	1 = PMA/PMD is able to perform 25GBASE-SR 0 = PMA/PMD is not able to perform 25GBASE-SR	RO
1.19.3	25GBASE-CR ability	1 = PMA/PMD is able to perform 25GBASE-CR 0 = PMA/PMD is not able to perform 25GBASE-CR	RO
1.19.2	25GBASE-CR-S ability	1 = PMA/PMD is able to perform 25GBASE-CR-S 0 = PMA/PMD is not able to perform 25GBASE-CR-S	RO
1.19.1	25GBASE-KR ability	1 = PMA/PMD is able to perform 25GBASE-KR 0 = PMA/PMD is not able to perform 25GBASE-KR	RO
1.19.0	25GBASE-KR-S ability	1 = PMA/PMD is able to perform 25GBASE-KR-S 0 = PMA/PMD is not able to perform 25GBASE-KR-S	RO

^aRO = Read only

45.2.1.14b.1 25GBASE-SR ability (1.19.4)

When read as a one, bit 1.19.4 indicates that the PMA/PMD is able to operate as a 25GBASE-SR PMA/PMD type. When read as a zero, bit 1.19.4 indicates that the PMA/PMD is not able to operate as a 25GBASE-SR PMA/PMD type.

45.2.1.14b.2 25GBASE-CR ability (1.19.3)

When read as a one, bit 1.19.3 indicates that the PMA/PMD is able to operate as a 25GBASE-CR PMA/PMD type. When read as a zero, bit 1.19.3 indicates that the PMA/PMD is not able to operate as a 25GBASE-CR PMA/PMD type.

45.2.1.14b.3 25GBASE-CR-S ability (1.19.2)

When read as a one, bit 1.19.2 indicates that the PMA/PMD is able to operate as a 25GBASE-CR-S PMA/PMD type. When read as a zero, bit 1.19.2 indicates that the PMA/PMD is not able to operate as a 25GBASE-CR-S PMA/PMD type.

45.2.1.14b.4 25GBASE-KR ability (1.19.1)

When read as a one, bit 1.19.1 indicates that the PMA/PMD is able to operate as a 25GBASE-KR PMA/PMD type. When read as a zero, bit 1.19.1 indicates that the PMA/PMD is not able to operate as a 25GBASE-KR PMA/PMD type.

45.2.1.14b.5 25GBASE-KR-S ability (1.19.0)

When read as a one, bit 1.19.0 indicates that the PMA/PMD is able to operate as a 25GBASE-KR-S PMA/PMD type. When read as a zero, bit 1.19.0 indicates that the PMA/PMD is not able to operate as a 25GBASE-KR-S PMA/PMD type.

45.2.1.80 BASE-R PMD control register (Register 1.150)

Change the first sentence of 45.2.1.80 as follows:

The BASE-R PMD control register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

45.2.1.81 BASE-R PMD status register (Register 1.151)

Change the first sentence of 45.2.1.81 as follows:

The BASE-R PMD status register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

45.2.1.82 BASE-R LP coefficient update, lane 0 register (Register 1.152)

Change the first sentence of 45.2.1.82 as follows:

The BASE-R LP coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

45.2.1.83 BASE-R LP status report, lane 0 register (Register 1.153)

Change the first sentence of 45.2.1.83 as follows:

The BASE-R LP status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

45.2.1.84 BASE-R LD coefficient update, lane 0 register (Register 1.154)

Change the first sentence of 45.2.1.84 as follows:

The BASE-R LD coefficient update, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

45.2.1.85 BASE-R LD status report, lane 0 register (Register 1.155)

Change the first sentence of 45.2.1.85 as follows:

The BASE-R LD status report, lane 0 register is used for 10GBASE-KR and other PHY types using the PMDs described in [Clause 72](#), [Clause 84](#), [Clause 85](#), [Clause 92](#), [Clause 93](#), ~~or Clause 94~~, [Clause 110](#), or [Clause 111](#).

Change the subclause title, the first sentence of 45.2.1.94, and the title of Table 45-74 as follows:

45.2.1.94 Single-lane PHY 40GBASE-R FEC corrected blocks counter (Register 1.172, 1.173)

The assignment of bits in the single-lane PHY 40GBASE-R FEC corrected blocks counter register is shown in Table 45-74.

Table 45-74—Single-lane PHY 40GBASE-R FEC corrected blocks counter register bit definitions

Change the subclause title, the first sentence of 45.2.1.95, and the title of Table 45-75 as follows:

45.2.1.95 Single-lane PHY 40GBASE-R FEC uncorrected blocks counter (Register 1.174, 1.175)

The assignment of bits in the single-lane PHY 40GBASE-R FEC uncorrected blocks counter register is shown in Table 45-75.

Table 45-75—Single-lane PHY 40GBASE-R FEC uncorrected blocks counter register bit definitions

Change the subclause title, the first sentence of 45.2.1.96, and the title of Table 45-76 as follows:

45.2.1.96 CAUI-4 chip-to-module C2M and 25GAUI C2M recommended CTLE register (Register 1.179)

The assignment of bits in the CAUI-4 chip-to-module C2M and 25GAUI C2M recommended CTLE register is shown in Table 45-76.

Table 45-76—CAUI-4 chip-to-module C2M and 25GAUI C2M recommended CTLE register bit definitions

45.2.1.96.1 Recommended CTLE peaking (1.179.4:1)

Change the first sentence of 45.2.1.96.1 as follows:

The value of these bits sets the CTLE peaking value recommended by a host that implements the optional CAUI-4 chip-to-module C2M and 25GAUI C2M interface defined in [Annex 83E](#) and [Annex 109B](#), respectively (see [83E.3.1.6](#)).

Change the subclause title, the first sentence of 45.2.1.97, the title of Table 45-77 and the subclauses of 45.2.1.97 as follows:

45.2.1.97 25GAUI C2C and lane 0 CAUI-4 chip-to-chip C2C transmitter equalization, receive direction, lane 0 register (Register 1.180)

The assignment of bits in the 25GAUI C2C and lane 0 CAUI-4 chip-to-chip C2C transmitter equalization, receive direction, lane 0 register is shown in Table 45-77.

Table 45-77—25GAUI C2C and lane 0 CAUI-4 chip-to-chip C2C transmitter equalization, receive direction, lane 0 register bit definitions

45.2.1.97.1 Request flag (1.180.15)

The value of this bit indicates the value of the variable *Request_flag* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This indicates whether the 25GAUI or CAUI-4 chip-to-chip C2C device is issuing a request to change the remote transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the receive direction. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.97.2 Post-cursor request (1.180.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient $c(1)$, which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the receive direction.

45.2.1.97.3 Pre-cursor request (1.180.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient $c(-1)$, which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the receive direction.

45.2.1.97.4 Post-cursor remote setting (1.180.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient $c(1)$ being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.97.5 Pre-cursor remote setting (1.180.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the 25GAUI or lane 0 CAUI-4 receiver in the receive direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient $c(-1)$ being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the receive direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the receive direction is not present in the package, then these bits have no effect.

45.2.1.97.6 Post-cursor local setting (1.180.4:2)

The value of these bits sets the variable *Local_eq_c1* for the 25GAUI or lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D-3), which controls the weight of the transmitter equalization post-cursor coefficient $c(1)$. If a 25GAUI or lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

45.2.1.97.7 Pre-cursor local setting (1.180.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the 25GAUI or lane 0 CAUI-4 transmitter in the receive direction (see 83D.3.1.1 and Table 83D-2), which controls the weight of the transmitter equalization precursor coefficient $c(-1)$. If a 25GAUI or lane 0 CAUI-4 transmitter in the receive direction is not present in the package, then these bits have no effect.

Change the subclause title, the first sentence of 45.2.1.99, the title of Table 45-78, and 45.2.1.99.1 through 45.2.1.99.7 as follows:

45.2.1.99 25GAUI C2C and lane 0 CAUI-4 chip-to-chipC2C transmitter equalization, transmit direction, ~~lane 0~~ register (Register 1.184)

The assignment of bits in the 25GAUI C2C and lane 0 CAUI-4 chip-to-chipC2C transmitter equalization, transmit direction, ~~lane 0~~ register is shown in Table 45-78.

Table 45-78—25GAUI C2C and lane 0 CAUI-4 chip-to-chipC2C transmitter equalization, transmit direction, ~~lane 0~~ register bit definitions

45.2.1.99.1 Request flag (1.184.15)

The value of this bit indicates the value of the variable *Request_flag* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This indicates whether the 25GAUI or CAUI-4 chip-to-chipC2C device is issuing a request to change the remote transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the transmit direction. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then the value returned for this bit should be zero.

45.2.1.99.2 Post-cursor request (1.184.14:12)

The value of these bits indicates the value of the variable *Requested_eq_c1* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the post-cursor coefficient *c*(1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the transmit direction.

45.2.1.99.3 Pre-cursor request (1.184.11:10)

The value of these bits indicates the value of the variable *Requested_eq_cm1* in the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). When *Request_flag* is equal to 1, this value indicates the ratio of the pre-cursor coefficient *c*(-1), which is requested for the transmitter equalization in the 25GAUI or lane 0 CAUI-4 chip-to-chip lane 0 C2C transmitter in the transmit direction.

45.2.1.99.4 Post-cursor remote setting (1.184.9:7)

The value of these bits sets the variable *Remote_eq_c1* for the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the post-cursor coefficient *c*(1) being used in the 25GAUI or lane 0 of the CAUI-4 or transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.99.5 Pre-cursor remote setting (1.184.6:5)

The value of these bits sets the variable *Remote_eq_cm1* for the 25GAUI or lane 0 CAUI-4 receiver in the transmit direction (see 83D.3.3.2). This is used by a 25GAUI or CAUI-4 receiver that implements the optional transmitter equalization feedback as an indication of the ratio of the pre-cursor coefficient *c*(-1) being used in the 25GAUI or lane 0 of the CAUI-4 transmitter in the transmit direction (see 83D.3.1.1). It may be used to generate values for the request flag and the request bits. If a 25GAUI or lane 0 CAUI-4 receiver in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.99.6 Post-cursor local setting (1.184.4:2)

The value of these bits sets the variable *Local_eq_c1* for the 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D-3), which controls the weight of the transmitter equalization post-cursor coefficient *c*(1). If a 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.99.7 Pre-cursor local setting (1.184.1:0)

The value of these bits sets the variable *Local_eq_cm1* for the 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction (see 83D.3.1.1 and Table 83D-2), which controls the weight of the transmitter equalization precursor coefficient *c*(-1). If a 25GAUI or lane 0 CAUI-4 transmitter in the transmit direction is not present in the package, then these bits have no effect.

45.2.1.101 RS-FEC control register (Register 1.200)

Change row for 1.200.15:2 of Table 45-79 as follows (unchanged rows not shown):

Table 45-79—RS-FEC control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.200.15:2 <u>1.200.15:3</u>	Reserved	Value always 0	RO
<u>1.200.2</u>	<u>25G RS-FEC Enable</u>	<u>1 = The 25GBASE-R Reed-Solomon FEC is enabled</u> <u>0 = The 25GBASE-R Reed-Solomon FEC is disabled</u>	<u>R/W</u>

^aR/W = Read/Write, RO = Read only

Insert new subclause 45.2.1.101.a before 45.2.1.101.1 as follows:

45.2.1.101.a 25G RS-FEC enable (1.200.2)

Bit 1.200.2 enables the 25GBASE-R Reed-Solomon FEC described in Clause 108. When set to a one, this bit enables the 25GBASE-R Reed-Solomon FEC. When set to a zero, bit 1.200.2 disables the 25GBASE-R Reed-Solomon FEC (see 108.6.3).

45.2.1.101.1 FEC bypass indication enable (1.200.1)

Change the last sentence as follows:

Writes to ~~this~~ bit 1.200.1 are ignored and reads return a zero if the RS-FEC does not have the ability to bypass indicating decoding errors to the PCS layer (see 91.5.3.3 and 108.5.3.2).

45.2.1.101.2 FEC bypass correction enable (1.200.0)

Change as follows:

When ~~this~~ bit 1.200.0 is set to one the Reed-Solomon decoder performs error detection without error correction (see 91.5.3.3 and 108.5.3.2). When this bit is set to zero, the decoder also performs error correction. Writes to this bit are ignored and reads return a zero if the RS-FEC does not have the ability to bypass correction.

45.2.1.102 RS-FEC status register (Register 1.201)

45.2.1.102.1 PCS align status (1.201.15)

Change 45.2.1.102.1 as follows:

Bit 1.201.15 indicates the PCS alignment status of the RS-FEC. For the RS-FEC described in [Clause 91](#), PCS alignment is defined as block lock, alignment marker lock, and deskew of all 20 transmit PCS lanes. For the RS-FEC described in [Clause 108](#), PCS alignment is defined as block lock of the transmit PCS signal. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not obtained PCS alignment. When read as a one, bit 1.201.15 indicates that the RS-FEC has obtained PCS alignment.

~~When read as a one, bit 1.201.15 indicates that the RS-FEC described in [Clause 91](#) has locked and aligned all transmit PCS lanes. When read as a zero, bit 1.201.15 indicates that the RS-FEC has not locked and aligned all transmit PCS lanes. A device that implements the RS-FEC status register but does not implement a separated RS-FEC shall return a one for bit 1.201.15.~~

45.2.1.102.2 RS-FEC align status (1.201.14)

Change 45.2.1.102.2 as follows:

Bit 1.201.14 indicates the PMA alignment status of the RS-FEC. For the RS-FEC described in [Clause 91](#), PMA alignment is defined as alignment marker lock and deskew of all four lanes on the PMA service interface. For the RS-FEC described in [Clause 108](#), PMA alignment is defined as codeword marker lock on the PMA service interface. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not obtained PMA alignment. When read as a one, bit 1.201.14 indicates that the RS-FEC has obtained PMA alignment.

~~When read as a one, bit 1.201.14 indicates that the RS-FEC described in [Clause 91](#) has locked and aligned all receive RS-FEC lanes. When read as a zero, bit 1.201.14 indicates that the RS-FEC has not locked and aligned all receive RS-FEC lanes.~~

45.2.1.102.7 RS-FEC high SER (1.201.2)

Change the first sentence of 45.2.1.102.7 as follows:

When FEC_bypass_indication_enable is set to one, ~~this~~ bit 1.201.2 is set to one if the number of RS-FEC symbol errors in a window of 8192 codewords exceeds the threshold (see [91.5.3.3](#) and [108.5.3.2](#)) and is set to zero otherwise.

45.2.1.102.8 FEC bypass indication ability (1.201.1)

Change the first sentence of 45.2.1.102.8 as follows:

The Reed-Solomon decoder may have the option to perform error detection without error indication (see [91.5.3.3](#) and [108.5.3.2](#)) to reduce the delay contributed by the RS-FEC sublayer.

45.2.1.102.9 FEC bypass correction ability (1.201.0)

Change the first sentence of 45.2.1.102.9 as follows:

The Reed-Solomon decoder may have the option to perform error detection without error correction (see [91.5.3.3](#) and [108.5.3.2](#)) to reduce the delay contributed by the RS-FEC sublayer.