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ISO/IEC/IEEE 8802-3

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AMENDMENT 4
2017-11

Information technology — Telecommunications and information exchange between systems — Local and metropolitan area networks — Specific requirements —

Part 3: Standard for Ethernet

AMENDMENT 4: Physical layer specifications and management parameters for 1 Gb/s operation over a single twisted-pair copper cable

Technologies de l'information — Télécommunications et échange d'information entre systèmes — Réseaux locaux et métropolitains — Prescriptions spécifiques —

Partie 3: Norme pour Ethernet

AMENDEMENT 4: Spécifications des couches physiques et paramètres de gestion pour l'exploitation des interfaces à 1 Go/s sur un seul câble de cuivre à paires torsadées

Reference number
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IEEE Std 802.3bp™-2016
(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016, and
IEEE Std 802.3bq™-2016)

IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable

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Approved 30 June 2016

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Abstract: This amendment to IEEE Std 802.3-2015 adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single twisted-pair copper cable in an automotive application.

Keywords: 1000BASE-T1, Ethernet, IEEE 802®, IEEE 802.3™, IEEE 802.3bp™

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Introduction

This introduction is not part of IEEE Std 802.3bp™-2016, IEEE Standard for Ethernet—Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable.

IEEE Std 802.3 was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half-duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel, and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile), and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bp-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats, and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted-pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

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Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 109C, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable

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(This amendment is based on IEEE Std 802.3™-2015 as amended by IEEE Std 802.3bw™-2015, IEEE Std 802.3by™-2016, and IEEE Std 802.3bq™-2016.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.[1]

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

[1]Notes in text, tables, and figures are given for information only, and do not contain requirements needed to implement the standard.

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1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

IEC 62153-4-14:2012, Metallic communication cable test methods—Part 4-14: Electromagnetic compatibility (EMC)—Coupling attenuation of cable assemblies (Field conditions) absorbing clamp method.

SAE J1292, Automobile and Motor Coach Wiring.

Change CISPR 25 reference, added in IEEE Std 802.3bw-2015, as follows:

IEC CISPR 25 ~~Edition 3.0 2008-03~~: Vehicles, boats and internal combustion engines—Radio disturbance characteristics—Limits and methods of measurement for the protection of on-board receivers.

1.4 Definitions

Insert the following new definition after 1.4.28 1000BASE-T:

1.4.28a 1000BASE-T1: IEEE 802.3 Physical Layer specification for 1000 Mb/s Ethernet using a single twisted-pair copper cable. (See IEEE Std 802.3, Clause 97.)

Insert the following new definition after 1.4.99 anomaly:

1.4.99a AN half-duplex function: The ability to exchange Auto-Negotiation DME pages over a single differential-pair medium. (See IEEE Std 802.3, Clause 98.)

Insert the following new definition after 1.4.107 BASE-R:

1.4.107a BASE-T1: PHYs that belong to the set of specific Ethernet PCS/PMA/PMDs that operate on a single twisted-pair copper cable, including 100BASE-T1 and 1000BASE-T1. (See IEEE Std 802.3, Clause 96 and Clause 97.)

Insert the following new definition after 1.4.381 single-port device:

1.4.381a single twisted-pair copper cable: Two insulated conductors twisted together in a regular fashion to form a balanced transmission line.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

MDAFEXT	multiple disturber alien far-end crosstalk
MDANEXT	multiple disturber alien near-end crosstalk

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30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the entry for 1000BASE-T:

1000BASE-T1 Clause 97 1000 Mb/s PAM3

30.3.2.1.3 aPhyTypeList

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the entry for 1000BASE-T:

1000BASE-T1 Clause 97 1000 Mb/s PAM3

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016. and IEEE Std 802.3bq-2016) after the entry for 1000BASE-TFD:

1000BASE-T1 single twisted-pair copper cable PHY as specified in Clause 97

30.5.1.1.4 aMediaAvailable

Insert the following new text into the third paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) after the third sentence inserted by IEEE Std 802.3bw:

For 1000BASE-T1, a link_status of OK maps to the enumeration “available”. All other states of link_status map to the enumeration “not available”.;

Change the fourth sentence of the third paragraph of BEHAVIOUR DEFINED AS (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) as follows:

Any MAU that implements management of Clause 28, ~~or~~ Clause 73, or Clause 98 Auto-Negotiation will map remote fault indication to MediaAvailable “remote fault.”

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30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.3 aAutoNegRemoteSignaling

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

The value indicates whether the remote end of the link is operating Auto-Negotiation signaling or not. It shall take the value detected if, during the previous link negotiation, FLP Bursts, /C/ ordered sets (see 36.2.4.10) or DME signals (see 73.5 and 98.2.1.1) were received from the remote end.;

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) after the entry for 1000BASE-TFD:

1000BASE-T1	1000BASE-T1 as specified in Clause 97

Change the following entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) as follows:

Rem Fault	Remote fault bit (RF) as specified in Clause 73 and Clause 98

Insert the following new entry in APPROPRIATE SYNTAX (as modified by IEEE Std 802.3by-2016) after the entry for BASE-RFEC25G Req inserted by IEEE Std 802.3by-2016:

Force MS	Force MASTER-SLAVE as specified in Clause 98 (see 98.2.1.2.5)

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This indicates the technology ability of the local device, as defined in Clause 28, Clause 37, ~~and~~ Clause 73, and Clause 98.;

30.6.1.1.6 aAutoNegAdvertisedTechnologyAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This GET-SET attribute maps to the technology ability of the local device, as defined in Clause 28, ~~and~~ Clause 37, and Clause 98.

30.6.1.1.7 aAutoNegReceivedTechnologyAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

Indicates the advertised technology ability of the remote hardware. For Clause 28 Auto-Negotiation, this attribute maps to the Technology Ability Field of the last received

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Auto- Negotiation link codeword(s). For Clause 37 Auto-Negotiation, this attribute maps to bits D0-D13 of the received Config_Reg Base Page (see 37.2.1). For Clause 73 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 73.6). For Clause 98 Auto-Negotiation, this attribute maps to bits D10-D13 and D21-D47 of the last received link codeword Base Page (see 98.2.1.2).;

30.6.1.1.8 aAutoNegLocalSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

This indicates the value of the selector field of the local hardware. The Selector Field is defined in 28.2.1.2.1 for Clause 28 Auto-Negotiation, in ~~and~~ 73.6.1 for Clause 73 Auto-Negotiation, and in 98.2.1.2.1 for Clause 98 Auto-Negotiation. The enumeration of the Selector Field indicates the standard that defines the remaining encodings for Auto-Negotiation using that value of enumeration. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".;

30.6.1.1.9 aAutoNegAdvertisedSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this GET-SET attribute maps to the Message Selector Field of the Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute maps to the Selector Field of the Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). A SET operation to a value not available in aAutoNegLocalSelectorAbility will be rejected. A successful SET operation will result in immediate link renegotiation if aAutoNegAdminState is enabled. For Clause 37 Auto-Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".

30.6.1.1.10 aAutoNegReceivedSelectorAbility

Change the BEHAVIOUR DEFINED AS for the attribute as follows:

BEHAVIOUR DEFINED AS:

In the case of Clause 28 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware. It maps to the Message Selector Field of the last received Auto-Negotiation link codeword. For Clause 73 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 73 Auto-Negotiation link codeword (see 73.6.1). For Clause 98 Auto-Negotiation, this attribute indicates the advertised message transmission ability of the remote hardware and maps to the Selector Field of the last received Clause 98 Auto-Negotiation link codeword (see 98.2.1.2.1). For Clause 37 Auto- Negotiation devices, a SET of this attribute will have no effect, and a GET will return the enumeration "ethernet".;

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34. Introduction to 1000 Mb/s baseband network

34.1 Overview

Insert a new subclause 34.1.5a after 34.1.5, with text on the support of Auto-Negotiation capability in 1000BASE-T1 PHY:

34.1.5a Auto-Negotiation, type 1000BASE-T1

Auto-Negotiation (Clause 98) may be used by 1000BASE-T1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for joint operation. Auto-Negotiation is performed upon link start-up through the use of half-duplex differential Manchester encoding.

The use of Clause 98 Auto-Negotiation is optional for a 1000BASE-T1 PHY.

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the row for 1.2103 through 1.32767 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bw-2015) in Table 45-3 as follows (unchanged rows not shown)

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.2103 through 1.~~32767~~2303	Reserved	
1.2304	1000BASE-T1 PMA control	45.2.1.133
1.2305	1000BASE-T1 PMA status	45.2.1.134
1.2306	1000BASE-T1 training	45.2.1.135
1.2307	1000BASE-T1 link partner training	45.2.1.136
1.2308	1000BASE-T1 test mode control	45.2.1.137
1.2309 through 32767	Reserved	

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

45.2.1.6.3 PMA/PMD type selection (1.7.5:0)

Change definition of value 1 1 1 1 0 1 for bits 1.7.5:0 in Table 45–7 (as added by IEEE Std 802.3bw-2015) as follows (unchanged rows not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 1 1 0 1 = ~~100~~BASE-T1 PMA/PMD[b]	R/W

[a]R/W = Read/Write, RO = Read only
[b]If BASE-T1 is selected, bits 1.2100.3:0 are used to differentiate which BASE-T1 PMA/PMD is selected.

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45.2.1.14a BASE-T1 PMA/PMD extended ability register (1.18)

Change Table 45–17a (as added by IEEE Std 802.3bw-2015) as follows:

Table 45–17a—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~1~~2	Reserved	Value always 0	RO
1.18.1	1000BASE-T1 ability	1 = PMA/PMD is able to perform 1000BASE-T1 0 = PMA/PMD is not able to perform 1000BASE-T1	RO
1.18.0	100BASE-T1 ability	1 = PMA/PMD is able to perform 100BASE-T1 0 = PMA/PMD is not able to perform 100BASE-T1	RO

[a]RO = Read only

45.2.1.131 BASE-T1 PMA/PMD control register (Register 1.2100)

Change 45.2.1.131 (added by IEEE Std 802.3bw-2015) as follows:

The assignment of bits in the BASE-T1 PMA/PMD control register is shown in Table 45–98a.

Table 45–98a—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2100.15	~~MASTER-SLAVE manual config enable~~Reserved	Value always 1	RO
1.2100.14	MASTER-SLAVE config value	1 = Configure PHY as MASTER 0 = Configure PHY as SLAVE	R/W
1.2100.13:4	Reserved	Value always 0	RO
1.2100.3:0	Type s~~S~~election	3 2 1 0 1 x x x = Reserved~~ for future use~~ 0 1 x x = Reserved~~ for future use~~ 0 0 1 x = Reserved~~ for future use~~ 0 0 0 1 = ~~Reserved for future use~~1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

Delete 45.2.1.131.1 and renumber 45.2.1.131.2 and 45.2.1.131.3 to 45.2.1.131.1 and 45.2.1.131.2. Change renumbered 45.2.1.131.1 and 45.2.1.131.2 (as added by IEEE Std 802.3bw-2015) as follows:

~~**45.2.1.131.1 BASE-T1 MASTER-SLAVE manual config enable (1.2100.15)**~~

~~Bit 1.2100.15 returns a one to indicate that MASTER or SLAVE configuration is set manually.~~

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45.2.1.131.1 ~~BASE-T1~~ MASTER-SLAVE config value (1.2100.14)

Bit 1.2100.14 is used to select MASTER or SLAVE operation when ~~MASTER-SLAVE manual config enable bit 1.2100.15 is set to one~~Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. If bit 1.2100.14 is set to one the PHY shall operate as MASTER. If bit 1.2100.14 is set to zero the PHY shall operate as SLAVE. This bit shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

45.2.1.131.2 ~~BASE-T1 t~~Type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented. When these bits are set to 0000, the mode of operation is 100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. These bits shall be ignored when the Auto-Negotiation enable bit 7.512.12 is set to one.

Insert 45.2.1.133 through 45.2.1.137 after 45.2.1.132 (as inserted by IEEE Std 802.3bw-2015) as follows:

45.2.1.133 1000BASE-T1 PMA control register (Register 1.2304)

The assignment of bits in the 1000BASE-T1 PMA control register is shown in Table 45–98c.

Table 45–98c—1000BASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2304.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2304.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2304.13:12	Reserved	Value always 0	RO
1.2304.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2304.10:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.1.133.1 PMA/PMD reset (1.2304.15)

Resetting the 1000BASE-T1 PMA/PMD is accomplished by setting bit 1.2304.15 to a one. This action shall set all 1000BASE-T1 PMA/PMD registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PMA/PMD shall return a value of one in bit 1.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 1.2304.15.

During a reset, the 1000BASE-T1 PMD/PMA shall respond to reads from register bits 1.2304.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

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Bit 1.2304.15 is a copy of 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PMA/PMD.

45.2.1.133.2 Transmit disable (1.2304.14)

When bit 1.2304.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2304.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2304.14 is a copy of 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.133.3 Low power (1.2304.11)

When the low-power ability is supported, the 1000BASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2304.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the 1000BASE-T1 PMA/PMD. The behavior of the 1000BASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power mode, the device shall, as a minimum, respond to management transactions necessary to exit the low-power mode. The default value of bit 1.2304.11 is zero.

This operation interrupts data communication. The data path of the 1000BASE-T1 PMD, depending on type and temperature, may take many seconds to run at optimum error ratio after exiting from reset or low-power mode.

Bit 1.2304.11 is a copy of 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the 1000BASE-T1 PMA/PMD in low-power mode.

45.2.1.134 1000BASE-T1 PMA status register (Register 1.2305)

The assignment of bits in the 1000BASE-T1 PMA status register is shown in Table 45–98d.

45.2.1.134.1 1000BASE-T1 OAM ability (1.2305.11)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports 1000BASE-T1 OAM (see 97.3.8). When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.134.2 EEE ability (1.2305.10)

When read as a one, this bit indicates that the 1000BASE-T1 PHY supports EEE. When read as a zero, this bit indicates that the 1000BASE-T1 PHY does not support EEE.

45.2.1.134.3 Receive fault ability (1.2305.9)

When read as a one, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2305.9 indicates that the 1000BASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

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Table 45–98d—1000BASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2305.15:12	Reserved	Value always 0	RO
1.2305.11	1000BASE-T1 OAM Ability	1 = PHY has 1000BASE-T1 OAM ability 0 = PHY does not have 1000BASE-T1 OAM ability	RO
1.2305.10	EEE Ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2305.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2305.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2305.7:3	Reserved	Value always 0	RO
1.2305.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2305.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO
1.2305.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LL = Latching Low

45.2.1.134.4 Low-power ability (1.2305.8)

When read as a one, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD supports the low-power ability. When read as a zero, bit 1.2305.8 indicates that the 1000BASE-T1 PMA/PMD does not support the low-power feature. If the 1000BASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2304.11 or bit 1.0.11.

45.2.1.134.5 Receive polarity (1.2305.2)

When read as zero, bit 1.2305.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2305.2 indicates that the polarity of receiver is reversed.

45.2.1.134.6 Receive fault (1.2305.1)

When read as a one, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2305.1 indicates that the 1000BASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2305.9. The 1000BASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for this bit.

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45.2.1.134.7 Receive link status (1.2305.0)

When read as a one, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2305.0 indicates that the 1000BASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.135 1000BASE-T1 training register (Register 1.2306)

The assignment of bits in the 1000BASE-T1 training register is shown in Table 45–98e.

Table 45–98e—1000BASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2306.15:11	Reserved	Value always 0	RO
1.2306.10:4	User field	7-bit user defined field to send to the link partner	R/W
1.2306.3:2	Reserved	Value always 0	RO
1.2306.1	1000BASE-T1 OAM advertisement	1 = 1000BASE-T1 OAM ability advertised to link partner 0 = 1000BASE-T1 OAM ability not advertised to link partner	R/W
1.2306.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.135.1 User field (1.2306.10:4)

This register is a user defined 7-bit field that is transmitted to the link partner during training.

45.2.1.135.2 1000BASE-T1 OAM advertisement (1.2306.1)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising 1000BASE-T1 OAM capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising 1000BASE-T1 OAM capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support 1000BASE-T1 OAM.

45.2.1.135.3 EEE advertisement (1.2306.0)

When set as a one, this bit indicates to the link partner that the 1000BASE-T1 PHY is advertising EEE capability. When set as a zero, this bit indicates to the link partner that the 1000BASE-T1 PHY is not advertising EEE capability. This bit shall be set to 0 if the 1000BASE-T1 PHY does not support EEE.

45.2.1.136 1000BASE-T1 link partner training register (Register 1.2307)

The assignment of bits in the 1000BASE-T1 link partner training register is shown in Table 45–98f. The values in this register are not valid until link is up.

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Table 45–98f—1000BASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2307.15:11	Reserved	Value always 0	RO
1.2307.10:4	Link partner user field	7-bit user defined field received from the link partner	RO
1.2307.3:2	Reserved	Value always 0	RO
1.2307.1	Link partner 1000BASE-T1 OAM advertisement	1 = Link partner has 1000BASE-T1 OAM ability 0 = Link partner does not have 1000BASE-T1 OAM ability	RO
1.2307.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.136.1 Link partner user field (1.2307.10:4)

This register is a user defined 7-bit field that is received from the link partner during training.

45.2.1.136.2 Link partner 1000BASE-T1 OAM advertisement (1.2307.1)

When read as a one, this bit indicates the link partner is advertising 1000BASE-T1 OAM capability. When read as a zero, this bit indicates the link partner is not advertising 1000BASE-T1 OAM capability. 1000BASE-T1 OAM capability shall be enabled only when both the local device and its link partner are advertising 1000BASE-T1 OAM capability.

45.2.1.136.3 Link partner EEE advertisement (1.2307.0)

When read as a one, this bit indicates the link partner is advertising EEE capability. When read as a zero, this bit indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local device and its link partner are advertising EEE capability.

45.2.1.137 1000BASE-T1 test mode control register (Register 1.2308)

The assignment of bits in the 1000BASE-T1 test mode control register is shown in Table 45–98g. The default values for each bit should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

45.2.1.137.1 Test mode control (1.2308.15:13)

Transmitter test mode operations defined by bits 1.2307.15:13, are described in 97.5.2 and Table 97–12. The default value for bits 1.2308.15:13 is zero.

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Table 45–98g—1000BASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2308.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Reserved 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	RO
1.2308.12:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.3 PCS Registers

Change reserved register space (3.1809 through 3.32767) in Table 45–119 as follows:

Table 45–119—PCS registers

Register address	Register name	Subclause
3.1809 through 3.~~32767~~2303	Reserved	
3.2304	1000BASE-T1 PCS control	45.2.3.51
3.2305	1000BASE-T1 PCS status 1	45.2.3.52
3.2306	1000BASE-T1 PCS status 2	45.2.3.53
3.2307	Reserved	
3.3208	1000BASE-T1 OAM transmit	45.2.3.54
3.2309 through 3.2312	1000BASE-T1 OAM message	45.2.3.55
3.2313	1000BASE-T1 OAM receive	45.2.3.56
3.2314 through 3.2317	Link partner 1000BASE-T1 OAM message	45.2.3.57
3.2318 through 3.32767	Reserved	

Insert new subclauses 45.2.3.51 through 45.2.3.57 after 45.2.3.50 as follows:

45.2.3.51 1000BASE-T1 PCS control register (Register 3.2304)

The assignment of bits in the 1000BASE-T1 PCS control register is shown in Table 45–163a. The default value for each bit of the 1000BASE-T1 PCS control register should be chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–163a—1000BASE-T1 PCS control register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2304.15	PCS reset	1 = PCS reset 0 = Normal operation	R/W, SC
3.2304.14	Loopback	1 = Enable loopback mode 0 = Disable loopback mode	R/W
3.2304.13:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.3.51.1 PCS reset (3.2304.15)

Resetting the 1000BASE-T1 PCS is accomplished by setting bit 3.2304.15 to a one. This action shall set all 1000BASE-T1 PCS registers to their default states. As a consequence, this action may change the internal state of the 1000BASE-T1 PCS and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 1000BASE-T1 PCS shall return a value of one in bit 3.2304.15 when a reset is in progress; otherwise, it shall return a value of zero. The 1000BASE-T1 PCS is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation within 0.5 s from the setting of bit 3.2304.15. During a reset, a PCS shall respond to reads from register bits 3.0.15, 3.8.15:14, and 3.2304.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 3.2304.15 is a copy of 3.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the 1000BASE-T1 PCS.

45.2.3.51.2 Loopback (3.2304.14)

The 1000BASE-T1 PCS shall be placed in a loopback mode of operation when bit 3.2304.14 is set to a one. When bit 3. 2304.14 is set to a one, the 1000BASE-T1 PCS shall accept data on the transmit path and return it on the receive path.

The default value of bit 3.2304.14 is zero.

Bit 3.2304.14 is a copy of 3.0.14 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback.

45.2.3.52 1000BASE-T1 PCS status 1 register (Register 3.2305)

The assignment of bits in the 1000BASE-T1 PCS status 1 register is shown in Table 45–163b. All the bits in the 1000BASE-T1 PCS status 1 register are read only; a write to the 1000BASE-T1 PCS status 1 register shall have no effect.

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Table 45–163b—1000BASE-T1 PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2305.15:12	Reserved	Value always 0	RO
3.2305.11	Tx LPI received	1 = Tx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.10	Rx LPI received	1 = Rx PCS has received LPI 0 = LPI not received	RO/LH
3.2305.9	Tx LPI indication	1 = Tx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.8	Rx LPI indication	1 = Rx PCS is currently receiving LPI 0 = PCS is not currently receiving LPI	RO
3.2305.7	Fault	1 = Fault condition detected 0 = No fault condition detected	RO
3.2305.6:3	Reserved	Value always 0	RO
3.2305.2	PCS receive link status	1 = PCS receive link up 0 = PCS receive link down	RO/LL
3.2305.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching high, LL = Latching low

45.2.3.52.1 Tx LPI received (3.2305.11)

When read as a one, bit 3.2305.11 indicates that the transmit 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.11 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.52.2 Rx LPI received (3.2305.10)

When read as a one, bit 3.2305.10 indicates that the receive 1000BASE-T1 PCS has received LPI signaling one or more times since the register was last read. When read as a zero, bit 3.2305.10 indicates that the 1000BASE-T1 PCS has not received LPI signaling. This bit shall be implemented with latching high behavior.

45.2.3.52.3 Tx LPI indication (3.2305.9)

When read as a one, bit 3.2305.9 indicates that the transmit 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.9 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

45.2.3.52.4 Rx LPI indication (3.2305.8)

When read as a one, bit 3.2305.8 indicates that the receive 1000BASE-T1 PCS is currently receiving LPI signals. When read as a zero, bit 3.2305.8 indicates that the 1000BASE-T1 PCS is not currently receiving LPI signals. The behavior if read during a state transition is undefined.

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45.2.3.52.5 Fault (3.2305.7)

When read as a one, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has detected a fault condition on either the transmit or receive paths. When read as a zero, bit 3.2305.7 indicates that the 1000BASE-T1 PCS has not detected a fault condition.

45.2.3.52.6 PCS receive link status (3.2305.2)

When read as a one, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link is up. When read as a zero, bit 3.2305.2 indicates that the 1000BASE-T1 PCS receive link was down since the last read from this register. This bit is a latching low version of bit 3.2306.10. The PCS receive link status bit shall be implemented with latching low behavior.

45.2.3.53 1000BASE-T1 PCS status 2 register (Register 3.2306)

The assignment of bits in the 1000BASE-T1 PCS status 2 register is shown in Table 45–163c. All the bits in the 1000BASE-T1 PCS status 2 register are read only; a write to the 1000BASE-T1 PCS status 2 register shall have no effect.

Table 45–163c—1000BASE-T1 PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2306.15:11	Reserved	Value always 0	RO
3.2306.10	Receive link status	1 = PCS receive link up 0 = PCS receive link down	RO
3.2306.9	PCS high BER	1 = PCS reporting a high BER 0 = PCS not reporting a high BER	RO
3.2306.8	PCS block lock	1 = PCS locked to received blocks 0 = PCS not locked to received blocks	RO
3.2306.7	Latched high BER	1 = PCS has reported a high BER 0 = PCS has not reported a high BER	RO/LH
3.2306.6	Latched block lock	1 = PCS has block lock 0 = PCS does not have block lock	RO/LL
3.2306.5:0	BER count	BER counter	RO/NR

[a]RO = Read only, LH = Latching High, LL = Latching Low, NR = Non Roll-over

45.2.3.53.1 Receive link status (3.2306.10)

When read as a one, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2306.10 indicates that the 1000BASE-T1 PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in 97.3.7.1.

45.2.3.53.2 PCS high BER (3.2306.9)

When read as a one, bit 3.2306.9 indicates that the 1000BASE-T1 PCS receiver is detecting a BER of $> 4 \times 10^{-4}$. When read as a zero, bit 3.2306.9 indicates that the 1000BASE-T1 PCS is not detecting a BER of $> 4 \times 10^{-4}$. This bit is a reflection of the state of the hi_rfer variable defined in 97.3.7.1.

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45.2.3.53.3 PCS block lock (3.2306.8)

When read as a one, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2306.8 indicates that the 1000BASE-T1 PCS receiver has not achieved block lock. This bit is a reflection of the state of the block_lock variable defined in 97.3.7.1.

45.2.3.53.4 Latched high BER (3.2306.7)

When read as a one, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has detected a high BER one or more times since the register was last read. When read as a zero, bit 3.2306.7 indicates that the 1000BASE-T1 PCS has not detected a high BER. The latched high BER bit shall be implemented with latching high behavior. This bit is a latching high version of the 1000BASE-T1 PCS high BER status bit (3.2306.9).

45.2.3.53.5 Latched block lock (3.2306.6)

When read as a one, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has achieved block lock. When read as a zero, bit 3.2306.6 indicates that the 1000BASE-T1 PCS has lost block lock one or more times since the register was last read. The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 1000BASE-T1 PCS block lock status bit (3.2306.8).

45.2.3.53.6 BER count (3.2306.5:0)

The BER counter formed by bits 3.2306.5:0 is a six bit count as defined by RFER_count in 97.3.7.2. These bits shall be reset to all zeros when the 1000BASE-T1 PCS status 2 register is read by the management function or upon execution of the 1000BASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

45.2.3.54 1000BASE-T1 OAM transmit register (Register 3.2308)

The assignment of bits in the 1000BASE-T1 OAM transmit register is shown in Table 45–163d.

Table 45–163d—1000BASE-T1 OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	1000BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit shall self-clear when registers are loaded by the state machine. 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	1000BASE-T1 OAM message received	This bit shall self clear on read. 1 = 1000BASE-T1 OAM message received by link partner 0 = 1000BASE-T1 OAM message not received by link partner	RO, LH
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO

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Table 45–163d—1000BASE-T1 OAM transmit register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.2308.11:8	Message number	User-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good 1000BASE-T1 OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.54.1 1000BASE-T1 OAM message valid (3.2308.15)

Bit 3.2308.15 shall be set to 1 when the 1000BASE-T1 OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. This register shall be cleared by the state machine to indicate whether the next 1000BASE-T1 OAM message can be written into the registers.

45.2.3.54.2 Toggle value (3.2308.14)

The state machine shall assign a value alternating between 0 and 1 to associate with the 8 octet 1000BASE-T1 OAM message transmit by the 1000BASE-T1 PHY. Bit 3.2308.14 should be read and recorded prior to setting 3.2308.15 to 1. The recorded value can be correlated with 3.2308.12 as a confirmation that the 1000BASE-T1 OAM message is received by the link partner.

45.2.3.54.3 1000BASE-T1 OAM message received (3.2308.13)

Bit 3.2308.13 shall indicate whether the most recently transmitted 1000BASE-T1 OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.54.4 Received message toggle value (3.2308.12)

Bit 3.2308.12 indicates the toggle bit value of the 1000BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is 1.

45.2.3.54.5 Message number (3.2308.11:8)

The 1000BASE-T1 OAM message number to be transmitted. This field is user defined but is recommended that it be used to indicate the meaning of the 8 octet 1000BASE-T1 OAM message. If used this way, up to 16 different 8-octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

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45.2.3.54.6 Ping received (3.2308.3)

Bit 3.2308.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.54.7 Ping transmit (3.2308.2)

Bit 3.2308.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.54.8 Local SNR (3.2308.1:0)

Bits 3.2308.1:0 are set by the 1000BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.55 1000BASE-T1 OAM message register (Registers 3.2309 to 3.2312)

The 8-octet 1000BASE-T1 OAM message data to be transmitted. The 8-octet message data is user defined and its definition is outside the scope of this standard. See Table 45–163e.

Table 45–163e—1000BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	1000BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	1000BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	1000BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	1000BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	1000BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	1000BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	1000BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	1000BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

45.2.3.56 1000BASE-T1 OAM receive register (Register 3.2313)

The assignment of bits in the 1000BASE-T1 OAM receive register is shown in Table 45–163f.

45.2.3.56.1 Link partner 1000BASE-T1 OAM message valid (3.2313.15)

Bit 3.2313.15 shall be set to 1 when the 1000BASE-T1 OAM message from the link partner is stored into registers 3.2314, 3.2315, 3.2316, and 3.2317 and the message number in 3.2313.11:8. This register shall be cleared when register 3.2317 is read.

45.2.3.56.2 Link partner toggle value (3.2313.14)

Bit 3.2313.14 indicates the toggle value associate with the 8 octet 1000BASE-T1 OAM message from the link partner.

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Table 45–163f—1000BASE-T1 OAM receive register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2313.15	Link partner 1000BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2313.11:8, 3.2314, 3.2315, 3.2316, and 3.2317 are stored and ready to be read. This bit shall self clear when register 3.2317 is read. 1 = Message data in registers are valid 0 = Message data in registers are not valid	RO, SC
3.2313.14	Link partner toggle value	Toggle value received with message.	RO
3.2313.13:12	Reserved	Value always 0	RO
3.2313.11:8	Link partner message number	Message number from link partner	RO
3.2313.7:2	Reserved	Value always 0	RO
3.2313.1:0	Link partner SNR	00 = Link partner link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current 1000BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain link partner SNR. Link partner requests local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.	RO

[a]RO = Read only, SC = Self-clearing

45.2.3.56.3 Link partner message number (3.2313.11:8)

The 1000BASE-T1 OAM message number from the link partner.

45.2.3.56.4 Link partner SNR (3.2313.1:0)

Bits 3.2313.1:0 indicate the status of the link partner receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.57 Link partner 1000BASE-T1 OAM message register (Registers 3.2314 to 3.2317)

The 8 octet 1000BASE-T1 OAM message data from the link partner. Register 3.2313.15 shall be cleared when register 3.2317 is read. See Table 45–163g.

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Table 45–163g—Link partner 1000BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2314.15:8	Link partner 1000BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	RO
3.2314.7:0	Link partner 1000BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	RO
3.2315.15:8	Link partner 1000BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	RO
3.2315.7:0	Link partner 1000BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	RO
3.2316.15:8	Link partner 1000BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	RO
3.2316.7:0	Link partner 1000BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	RO
3.2317.15:8	Link partner 1000BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	RO
3.2317.7:0	Link partner 1000BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	RO

[a]RO = Read only

45.2.7 Auto-Negotiation registers

Change reserved register space (7.62 through 7.32767) in Table 45-200 as follows:

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.62 through 7.~~32 767~~511	Reserved	
7.512	BASE-T1 AN control	45.2.7.14c
7.513	BASE-T1 AN status	45.2.7.14d
7.514 through 7.516	BASE-T1 AN advertisement	45.2.7.14e
7.517 through 7.519	BASE-T1 AN LP Base Page ability	45.2.7.14f
7.520 through 7.522	BASE-T1 AN Next Page transmit	45.2.7.14g
7.523 through 7.525	BASE-T1 AN LP Next Page ability	45.2.7.14h
7.526 through 7.32767	Reserved	

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Insert subclauses 45.2.7.14c through 45.2.7.14h (after 45.2.7.14b inserted by IEEE Std 802.3bq-2016) as follows:

45.2.7.14c BASE-T1 AN control register (Register 7.512)

The assignment of bits in the BASE-T1 AN control register is shown in Table 45–211c. The default value for each bit of the BASE-T1 AN control register has been chosen so that the initial state of the device upon power up or completion of reset is a normal operational state without management intervention.

Table 45–211c—BASE-T1 AN control register bit definitions

Bit(s)	Name	Description	R/W[a]
7.512.15	AN reset	1 = AN reset 0 = AN normal operation	R/W, SC
7.512.14:13	Reserved	Value always 0	RO
7.512.12	Auto-Negotiation enable	1 = enable Auto-Negotiation process 0 = disable Auto-Negotiation process	R/W
7.512.11:10	Reserved	Value always 0	RO
7.512.9	Restart Auto-Negotiation	1 = Restart Auto-Negotiation process 0 = Auto-Negotiation in process, disabled, or not supported	R/W, SC
7.512.8:0	Reserved	Value always 0	RO

[a]RO = Read only, R/W = Read/Write, SC = Self-clearing

45.2.7.14c.1 AN reset (7.512.15)

Resetting AN is accomplished by setting bit 7.512.15 to a one. This action shall set all BASE-T1 AN registers to their default states. As a consequence, this action may change the internal state of AN and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and AN shall return a value of one in bit 7.512.15 when a reset is in progress and a value of zero otherwise. AN is not required to accept a write transaction to any of its registers until the reset process is complete. The reset process shall be completed within 0.5 s from the setting of bit 7.512.15. During an AN reset, AN shall respond to reads from register bit 7.512.15. All other register bits shall be ignored.

The default value for bit 7.512.15 is zero.

NOTE—This operation may interrupt data communication.

45.2.7.14c.2 Auto-Negotiation enable (7.512.12)

The Auto-Negotiation function shall be enabled by setting bit 7.512.12 to a one. If bit 7.512.12 is set to one, then type selection bits 1.2100.3:0 and MASTER-SLAVE bits 1.2100.14 shall have no effect on the link configuration, and the Auto-Negotiation process determines the link configuration. If bit 7.512.12 is cleared to zero, then bits 1.2100.3:0 and bit 1.2100.14 determine the link configuration regardless of the prior state of the link configuration and the Auto-Negotiation process.

If the BASE-T1 PHY reports via bit 7.513.3 that it lacks the ability to perform Auto-Negotiation, then the value of bit 7.512.12 shall be zero.

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45.2.7.14c.3 Restart Auto-Negotiation (7.512.9)

If the BASE-T1 PMA/PMD reports (via bit 7.513.3) that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the BASE-T1 PMA/PMD shall return a value of zero in bit 7.512.9 and any attempt to write a one to bit 7.512.9 shall be ignored.

Otherwise, the Auto-Negotiation process shall be restarted by setting bit 7.512.9 to one. This bit is self-clearing, and the BASE-T1 PMA/PMD shall return a value of one in bit 7.512.9 until the Auto-Negotiation process has been initiated. If Auto-Negotiation was completed prior to this bit being set, the process shall be reinitialized. The Auto-Negotiation process shall not be affected by clearing this bit to zero.

The default value for 7.512.9 is zero.

45.2.7.14d BASE-T1 AN status (Register 7.513)

The assignment of bits in the BASE-T1 AN status register is shown in Table 45–211d. All the bits in the BASE-T1 AN status register are read only; therefore, a write to the BASE-T1 AN status register shall have no effect.

Table 45–211d—BASE-T1 AN status register bit definitions

Bit(s)	Name	Description	R/W[a]
7.513.15:7	Reserved	Value always 0	RO
7.513.6	Page received	1 = A page has been received 0 = A page has not been received	RO, LH
7.513.5	Auto-Negotiation complete	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	RO
7.513.4	Remote fault	1 = remote fault condition detected 0 = no remote fault condition detected	RO, LH
7.513.3	Auto-Negotiation ability	1 = PHY is able to perform Auto-Negotiation 0 = PHY is not able to perform Auto-Negotiation	RO
7.513.2	Link status	1 = Link is up 0 = Link is down	RO, LL
7.513.1:0	Reserved	Value always 0	RO

[a]RO = Read only, LH = Latching High, LL = Latching Low

45.2.7.14d.1 Page received (7.513.6)

The Page received bit (7.513.6) shall be set to one to indicate that a new link codeword has been received and stored in the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 or the BASE-T1 AN LP Next Page ability registers 7.523 to 7.525. The contents of the BASE-T1 AN LP Base Page ability registers 7.517 to 7.519 are valid when bit 7.513.6 is set the first time during the Auto-Negotiation. The Page received bit shall be reset to zero on a read of the BASE-T1 AN status register (Register 7.513).

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