
**Information technology —
Telecommunications and information
exchange between systems — Local
and metropolitan area networks —
Specific requirements —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 6: Physical layer
specifications and management
parameters for ethernet passive optical
networks protocol over coax**

*Technologies de l'information — Télécommunications et échange
d'information entre systèmes — Réseaux locaux et métropolitains —
Prescriptions spécifiques —*

Partie 3: Norme pour Ethernet

AMENDEMENT 6



Reference number
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as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016, and
IEEE Std 802.3br™-2016)

IEEE Standard for Ethernet

Amendment 6: Physical Layer Specifications and Management Parameters for Ethernet Passive Optical Networks Protocol over Coax

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 22 September 2016
IEEE-SA Standards Board

Abstract: Physical Layer specifications and management parameters for the operation of Ethernet Passive Optical Networks (EPON) Protocol over coaxial media is defined by this amendment to IEEE Std 802.3-2015.

Keywords: amendment, EPoC, EPON, EPON Protocol over Coax, Ethernet; Ethernet Passive Optical Networks, IEEE 802.3™, IEEE 802.3bn™, Multi-Point MAC Control (MPMC), orthogonal frequency division multiplexing (OFDM), Physical Coding Sublayer (PCS), Physical Media Attachment (PMA), Physical Medium Dependent (PMD), PON, point to multipoint (P2MP)

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Introduction

This introduction is not part of IEEE Std 802.3bn-2016, IEEE Standard for Ethernet—Amendment 6: Physical Layer Specifications and Management Parameters for Ethernet Passive Optical Networks Protocol over Coax.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bn-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Acknowledgments

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.¹

The editing instructions are shown in **bold italic**. Four editing instructions are used: change, delete, insert, and replace. **Change** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). **Delete** removes existing material. **Insert** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. **Replace** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.2 Notation

Insert a new 1.2.7 after 1.2.6 “Accuracy and resolution of numerical quantities” as follows:

1.2.7 Qm.n number format

The Qm.n number format is a fixed-point number format where the number of fractional bits is specified by n and optionally the number of integer bits is specified by m. For example, a Q14 number has 14 fractional bits; a Q2.14 number has 2 integer bits and 14 fractional bits. Preceding the “Q” with a “U” indicates an unsigned number.

1.3 Normative references

Insert the following references in alphanumeric order:

CFR 76, Code of Federal Regulations, Title 47, Part 76, October 2005.

IEC 61169-24:2009, Radio-frequency connectors—Part 24: Sectional specification—Radio frequency coaxial connectors with screw coupling, typically for use in 75 Ω cable networks (type F).

IEEE Std 802.1AS™-2011, IEEE Standard for Local and metropolitan area networks—Timing and Synchronization for Time-Sensitive Applications in Bridged Local Area Networks.

SCTE 02 2006, Specification for “F” Port, Female, Indoor.

1.4 Definitions

Insert the following definition after 1.4.49 “10GBASE-X” as follows:

1.4.49a 10GPASS-XR: A collection of IEEE 802.3 EPON Protocol over Coax (EPoC) Physical Layer specifications for up to 10 Gb/s downstream and up to 1.6 Gb/s upstream point-to-multipoint link over a coax cable distribution network. (See IEEE Std 802.3, Table 56–1, Clause 100, Clause 101, Clause 102, and Clause 103.)

Change the definition of 1.4.134 as modified by IEEE Std 802.3by-2016 as follows:

1.4.134 channel: In 10BROAD36 and 10GPASS-XR, a band of frequencies dedicated to a certain service transmitted on the broadband medium. Otherwise, a defined path along which data in the form of an electrical or optical signal passes. (For 10BROAD36, see IEEE Std 802.3, [Clause 11](#), for 10GPASS-XR see [Clause 100](#), [Clause 101](#), and [Clause 102](#).)

Insert the following definitions after 1.4.144 “Clocked Violation LO (CVL)” as follows:

1.4.144a coax cable distribution network (CCDN): A radio frequency (RF) distribution plant composed of either amplified or passive coaxial media.

1.4.144b coax line terminal (CLT): The network-end DTE for a coaxial access network. The CLT is the master entity in a P2MP EPoC network with regard to the MPCP protocol.

1.4.144c coax network unit (CNU): The subscriber-end DTE to a coaxial access network. A CNU is a slave entity in a P2MP EPoC network with regard to the MPCP protocol.

Insert the following definition after 1.4.170 “cross connect” as follows:

1.4.170a cyclic prefix (CP): A redundant set of samples prepended to an OFDM symbol.

Insert the following definition after 1.4.277 “mixing segment” and before 1.4.277a (as inserted by IEEE Std 802.3bq-2016) as follows:

1.4.277aa modulation error ratio (MER): The ratio of average signal constellation power to average constellation error power—that is, digital complex baseband signal-to-noise ratio—expressed in decibels.

Insert the following definition after 1.4.294 “OAM Discovery” as follows:

1.4.294a OFDM channel: See orthogonal frequency division multiplexing (OFDM) channel.

Insert the following definition after 1.4.296 “Operations, Administration, and Maintenance (OAM)” as follows:

1.4.296a optical distribution network (ODN): An optical distribution plant composed of fiber optic cabling and a passive optical splitter or cascade of splitters.

Insert the following definition after 1.4.306 “Organizationally Unique Identifier (OUI)” as follows:

1.4.306a orthogonal frequency division multiplexing (OFDM) channel: A data transmission channel in which the transmitted data is carried over a number of orthogonal subcarriers.

Change the definition of 1.4.331 “Point-to-Multipoint network (P2MP)” as follows:

1.4.331 Point-to-Multipoint network (P2MP): ~~A passive optical network providing transport of Ethernet frames. A network topology based on a centralized station connected to a number of end stations. Frames transit the network between the central station and the end stations and do not transit directly from end station to end station.~~ (See IEEE Std 802.3, [Clause 64](#), ~~and~~ [Clause 65](#), [Clause 76](#), [Clause 77](#), [Clause 101](#), and [Clause 103](#)).

Insert the following definition after 1.4.348 “quad” as follows:

1.4.348a quadrature amplitude modulation (QAM) symbol: The amplitude-phase representation of the bits of data that modulate a carrier signal or that modulate each of the subcarriers in OFDM.

Change the note in 1.4.400 as follows:

NOTE—See [Clause 64](#), ~~and~~ [Clause 77](#), ~~and~~ [Clause 103](#). The value of time_{quantum} is defined in 64.2.2.1.

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphabetical order:

CCDN	coax cable distribution network
CLT	coax line terminal
CNU	coax network unit
CP	cyclic prefix

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EPoC	EPON protocol over coax
HFC	hybrid fiber coax
MER	modulation error ratio
OFDM	orthogonal frequency division multiplexing
OFDMA	orthogonal frequency division multiple access
QAM	quadrature amplitude modulation
RF	radio frequency
RTT	round trip time

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert after 10/1GBASE-PRX a single line for “10GPASS-XR” type into the APPROPRIATE SYNTAX list of 30.3.2.1.2 aPhyType (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, and IEEE Std 802.3bp-2016) as follows:

...	10GPASS-XR	Clause 101 PCS up to 10 Gb/s 64B/66B OFDM downstream and up to 1.6 Gb/s 64B/66B OFDMA upstream
...		

30.3.2.1.3 aPhyTypeList

Insert after 10/1GBASE-PRX a single line for “10GPASS-XR” type into the APPROPRIATE SYNTAX list of 30.3.2.1.3 aPhyTypeList (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, and IEEE Std 802.3bp-2016) as follows:

...	10GPASS-XR	Clause 101 PCS up to 10 Gb/s 64B/66B OFDM downstream and up to 1.6 Gb/s 64B/66B OFDMA upstream
...		

30.3.5 MPCP managed object class

Change the capitalization of the title for 30.3.5.1 as follows:

30.3.5.1 MPCP Attributes

30.3.5.1.2 aMPCPAdminState

Change the description for “BEHAVIOUR DEFINED AS” section of 30.3.5.1.2 aMPCPAdminState to add Clause 103 to the list of cross references as follows:

....
 BEHAVIOUR DEFINED AS:
 A read-only value that identifies the operational state of the Multipoint MAC Control sublayer. An interface that can provide the Multipoint MAC Control sublayer functions specified in [Clause 64](#), ~~or Clause 77~~, or [Clause 103](#) is enabled to do so when this attribute has the enumeration “enabled”. When this attribute has the enumeration “disabled”, the interface acts as it would if it had no Multipoint MAC Control sublayer. The operational state of the Multipoint MAC Control sublayer can be changed using the acMPCPAdminControl action.;

30.3.5.1.3 aMPCPMode

Change the description for “APPROPRIATE SYNTAX” and “BEHAVIOUR DEFINED AS” section of 30.3.5.1.3 aMPCPMode as follows:

...

APPROPRIATE SYNTAX:

An ENUMERATED VALUE that has the following entries:

OLT

ONU

CLT

CNU

BEHAVIOUR DEFINED AS:

A read-only value that identifies the operational mode of the Multipoint MAC Control sublayer.

An interface that can provide the Multipoint MAC Control sublayer functions specified in Clause 64, ~~or Clause 77, or Clause 103. When operates as an OLT when~~ this attribute has the enumeration “OLT”, the interface acts as an OLT. When this attribute has the enumeration “ONU”, the interface acts as an ONU. When this attribute has the enumeration “CLT”, the interface acts as a CLT. When this attribute has the enumeration “CNU”, the interface acts as a CNU.

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert after 10GBASE-T a single line for “10GPASS-XR” type into the APPROPRIATE SYNTAX list of 30.5.1.1.2 aMAUType (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3by-2016, IEEE Std 802.3bq-2016, and IEEE Std 802.3bp-2016) as follows:

...

10GBASE-XR

Coax cable distribution network PHY continuous downstream/burst mode upstream PHY as specified in Clause 100 and Clause 101

...

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

Change reserved row 12 through 28 of Table 45–1 and insert a new row 12 as follows (unchanged rows are not shown):

Table 45–1—MDIO Manageable Device addresses

Device address	MMD name
<u>12</u>	<u>OFDM PMA/PMD</u>
12 13 through 28	Reserved

Change the identified reserved row in Table 45–2 and insert a new row for OFDM devices immediately below the changed row as follows (unchanged rows and footnotes not shown):

Table 45–2—Devices in package registers bit definitions

Bit(s)	Name	Description	R/W
m.5.15: 12 <u>13</u>	Reserved	Value always 0	RO
m.5.12	OFDM	1 = OFDM present in package 0 = OFDM not present in package	RO

45.2.1 PMA/PMD registers

Change the reserved row for 1.17 in Table 45–3 (as inserted by IEEE Std 802.3bw-2015) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.17	Reserved <u>EPoC PMA/PMD ability</u>	<u>45.2.1.14aa</u>

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Change Table 45–3 (as inserted by IEEE Std 802.3bw-2015) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.1809 through 1.1899 ²⁰⁹⁹	Reserved	
<u>1.1900</u>	<u>10GPASS-XR control and status</u>	<u>45.2.1.130a</u>
<u>1.1901</u>	<u>DS OFDM control</u>	<u>45.2.1.130b</u>
<u>1.1902 through 1.1906</u>	<u>DS OFDM channel frequency control</u>	<u>45.2.1.130c</u>
<u>1.1907</u>	<u>US OFDM control</u>	<u>45.2.1.130d</u>
<u>1.1908</u>	<u>US OFDM channel frequency control</u>	<u>45.2.1.130e</u>
<u>1.1909</u>	<u>US OFDMA pilot pattern</u>	<u>45.2.1.130f</u>
<u>1.1910</u>	<u>Profile control</u>	<u>45.2.1.130g</u>
<u>1.1911</u>	<u>DS PHY Link control</u>	<u>45.2.1.130h</u>
<u>1.1912</u>	<u>US PHY Link control</u>	<u>45.2.1.130i</u>
<u>1.1913 and 1.1914</u>	<u>PHY Discovery control</u>	<u>45.2.1.130j</u>
<u>1.1915</u>	<u>New CNU control</u>	<u>45.2.1.130k</u>
<u>1.1916 through 1.1920</u>	<u>New CNU info</u>	<u>45.2.1.130l</u>
<u>1.1921</u>	<u>DS PHY Link frame counter</u>	<u>45.2.1.130m</u>
<u>1.1922 and 1.1923</u>	<u>PMA/PMD timing offset</u>	<u>45.2.1.130n</u>
<u>1.1924</u>	<u>PMA/PMD power offset</u>	<u>45.2.1.130o</u>
<u>1.1925 and 1.1926</u>	<u>PMA/PMD ranging offset</u>	<u>45.2.1.130p</u>
<u>1.1927 through 1.1929</u>	<u>DS PMA/PMD data rate</u>	<u>45.2.1.130q</u>
<u>1.1930 through 1.1932</u>	<u>US PMA/PMD data rate</u>	<u>45.2.1.130r</u>
<u>1.1933 and 1.1934</u>	<u>10GPASS-XR FEC codeword counter</u>	<u>45.2.1.130s</u>
<u>1.1935 and 1.1936</u>	<u>10GPASS-XR FEC codeword success counter</u>	<u>45.2.1.130t</u>
<u>1.1937 and 1.1938</u>	<u>10GPASS-XR FEC codeword fail counter</u>	<u>45.2.1.130u</u>
<u>1.1939</u>	<u>PHY Link EPFH counter</u>	<u>45.2.1.130v</u>
<u>1.1940</u>	<u>PHY Link EPFH error counter</u>	<u>45.2.1.130w</u>
<u>1.1941</u>	<u>PHY Link EPCH counter</u>	<u>45.2.1.130x</u>

Table 45–3—PMA/PMD registers (continued)

Register address	Register name	Subclause
<u>1.1942</u>	<u>PHY Link EPCH error counter</u>	<u>45.2.1.130y</u>
<u>1.1943</u>	<u>PHY Link EMB counter</u>	<u>45.2.1.130z</u>
<u>1.1944</u>	<u>PHY Link EMB error counter</u>	<u>45.2.1.130z1</u>
<u>1.1945</u>	<u>PHY Link FPMB counter</u>	<u>45.2.1.130z2</u>
<u>1.1946</u>	<u>PHY Link FPMB error counter</u>	<u>45.2.1.130z3</u>
<u>1.1947</u>	<u>US PHY Link response time</u>	<u>45.2.1.130z4</u>
<u>1.1948</u>	<u>10GPASS-XR modulation ability</u>	<u>45.2.1.130z5</u>
<u>1.1949</u>	<u>PHY Discovery Response power control</u>	<u>45.2.1.130z6</u>
<u>1.1950</u>	<u>US target receive power</u>	<u>45.2.1.130z7</u>
<u>1.1951 through 1.1955</u>	<u>DS transmit power</u>	<u>45.2.1.130z8</u>
<u>1.1956 and 1.1957</u>	<u>US receive power measurement</u>	<u>45.2.1.130z9</u>
<u>1.1958</u>	<u>Reported power</u>	<u>45.2.1.130z10</u>
<u>1.1959 through 1.2099</u>	<u>Reserved</u>	

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the reserved row for 1.4.10 in Table 45–6 as inserted by IEEE Std 802.3by-2016 as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.4.10	<u>Reserved</u> <u>10GPASS-XR capable</u>	<u>Value always 0</u> <u>1 = PMA/PMD is capable of operating as 10GPASS-XR</u> <u>0 = PMA/PMD is not capable of operating as</u> <u>10GPASS-XR</u>	RO

^aRO = Read only

Insert 45.2.1.4.b after 45.2.1.4.a (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.4.b 10GPASS-XR capable (1.4.10)

When read as one, bit 1.4.10 indicates that the PMA/PMD is able to operate as 10GPASS-XR. When read as zero, bit 1.4.10 indicates that the PMA/PMD is not able to operate as 10GPASS-XR.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the PMA/PMD type selection row in Table 45–7 to add 10GPASS-XR PMDs as follows (only Bits, Name, added Description text, and R/W is shown). Change “reserved” line(s) as appropriate for values defined by this and other approved amendments.

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.5:0	PMA/PMD type selection	<u>1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD</u> <u>1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD</u>	R/W

^aR/W = Read/Write, RO = Read only

Insert 45.2.1.14aa and Table 45–17aa before 45.2.1.14a as inserted by IEEE Std 802.3bw-2015 as follows:

45.2.1.14aa EPoC PMA/PMD ability register (Register 1.17)

The assignment of bits in the EPoC PMA/PMD ability register is shown in Table 45–17aa. All of the bits in the EPoC PMA/PMD ability register are read only; a write to the EPoC PMA/PMD ability register shall have no effect.

Table 45–17aa—EPoC PMA/PMD ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.17.15:2	Reserved	Value always 0	RO
1.17.1	10GPASS-XR-D ability	1 = PMA/PMD is able to perform 10GPASS-XR-D 0 = PMA/PMD is not able to perform 10GPASS-XR-D	RO
1.17.0	10GPASS-XR-U ability	1 = PMA/PMD is able to perform 10GPASS-XR-U 0 = PMA/PMD is not able to perform 10GPASS-XR-U	RO

^aRO = Read only

45.2.1.14aa.1 10GPASS-XR-D ability (1.17.1)

When read as one, bit 1.17.1 indicates that the PMA/PMD is able to operate as a 10GPASS-XR-D PMA/PMD type. When read as zero, bit 1.17.1 indicates that the PMA/PMD is not able to operate as a 10GPASS-XR-D PMA/PMD type.

45.2.1.14aa.2 10GPASS-XR-U ability (1.17.0)

When read as one, bit 1.17.0 indicates that the PMA/PMD is able to operate as a 10GPASS-XR-U PMA/PMD type. When read as zero, bit 1.17.0 indicates that the PMA/PMD is not able to operate as a 10GPASS-XR-U PMA/PMD type.

Insert 45.2.1.130a through 45.2.1.130z10 after 45.2.1.130 as follows:

45.2.1.130a 10GPASS-XR control and status register (Register 1.1900)

The assignment of bits in the 10GPASS-XR control and status register is shown in Table 45–98aa.

Table 45–98aa—10GPASS-XR control and status register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1900.15:14	Reserved	Value always 0	RO
1.1900.13	Time synch capable	1 = The CNU supports time synchronization variables 0 = The CNU does not support time synchronization variables	RO
1.1900.12	US rate mismatch	1 = the upstream rate calculated at the CNU and the CLT matches within 10 b/s 0 = the upstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s	RO
1.1900.11	DS rate mismatch	1 = the downstream rate calculated at the CNU and the CLT matches within 10 b/s 0 = the downstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s	RO
1.1900.10	Link up ready	1 = the CNU is ready to enter the Link-Up state 0 = the CNU is not ready to enter the Link-Up state	R/W
1.1900.9:3	Continuous pilot scaling factor	Number of continuous pilots in the downstream OFDM channels	R/W
1.1900.2	CRC40 errored blocks	1 = 65-bit blocks with detected CRC40 errors are labeled as errored 0 = 65-bit blocks with detected CRC40 errors are not labeled as errored	R/W
1.1900.1	PHY Discovery complete	1 = The PMA/PMD has completed PHY Discovery on the coaxial cable distribution network 0 = The PMA/PMD has not completed PHY Discovery on the coaxial cable distribution network	R/W
1.1900.0	PHY Discovery enable	1 = PMA/PMD is permitted to transmit on the media 0 = PMA/PMD is not permitted to transmit on the media	R/W

^aRO = Read only, R/W = Read/Write

45.2.1.130a.1 Time synch capable (1.1900:13)

When read as one, bit 1.1900:13 indicates that the 10G-PASS-XR PMA/PMD is capable of supporting the time synchronization variables PHY differential delay and PHY differential delay tolerance reflected in registers 1.1949 and 1.1950. This bit is a reflection of the *TimeSyncCapable* variable defined in 101.6.

45.2.1.130a.2 US rate mismatch (1.1900:12)

When read as one, bit 1.1900.12 indicates that the upstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as zero. This bit is a reflection of the *US_RateMatchFail* variable defined in 100.3.2.3.

45.2.1.130a.3 DS rate mismatch (1.1900:11)

When read as one, bit 1.1900.11 indicates that the downstream rate calculated at the CNU and the CLT is mismatched by greater than 10 b/s. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as zero. This bit is a reflection of the *DS_RateMatchFail* variable defined in 100.3.2.3.

45.2.1.130a.4 Link up ready (1.1900:10)

Bit 1.1900.10 indicates that the CNU is ready for the link-up state. This bit is a reflection of the *LinkUpRdy* variable defined in 102.4.1.9.2.

45.2.1.130a.5 Continuous pilot scaling factor (1.1900.9:3)

Bits 1.1900.9:3 form an unsigned integer that is used to determine the number of continuous pilots in the downstream OFDM channels. These bits are a reflection of the variable *CntPltSF* defined in 101.4.3.6.5.

45.2.1.130a.6 CRC40 errored blocks (1.1900.2)

Bit 1.1900.2 is used to control whether 65-bit blocks with detected CRC40 errors are labeled as errored before being passed higher layers as described in 101.3.3.1.4. This bit is a reflection of the variable *CRC40ErrCtrl* defined in 101.3.3.1.6.

45.2.1.130a.7 PHY Discovery complete (1.1900.1)

When read as one, bit 1.1900.1 indicates that the 10GPASS-XR PMA/PMD has completed PHY Discovery (see 102.4.1) on the coaxial cable distribution network. When read as zero, bit 1.1900.1 indicates that the PMA/PMD has not completed PHY Discovery on the coaxial cable distribution network. This bit is defined in 10GPASS-XR-U PMA/PMD only, in 10GPASS-XR-D always read as one. This bit is a reflection of the variable *PhyDiscCmplt* defined in 102.4.1.9.2.

The default value for bit 1.1900.1 is zero.

45.2.1.130a.8 PHY Discovery enable (1.1900.0)

When read as one, bit 1.1900.0 indicates that the 10GPASS-XR PMA/PMD is permitted to transmit on the media. When read as zero, bit 1.1900.0 indicates that the PMA/PMD is not permitted to transmit on the media. This bit is a reflection of the variable *PD_Enable* defined in 102.2.7.3.

The default value for bit 1.1900.0 is zero.

45.2.1.130b DS OFDM control register (Register 1.1901)

The assignment of bits in the DS OFDM control register is shown in Table 45–98ab.

Table 45–98ab—DS OFDM control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1901.15	CLT tx mute	1 = CLT PHY muted state for test purposes 0 = CLT PHY not muted (normal operation)	R/W

Table 45–98ab—DS OFDM control register bit definitions (continued)

Bit(s)	Name	Description	R/W ^a
1.1901.14:12	DS OFDM channels	Indicates the number of OFDM channels the PMA/PMD is operating in the downstream direction	R/W
1.1901.11:7	DS time interleaving	Indicates the number of OFDM symbols the PMA/PMD is time interleaving in the downstream direction	R/W
1.1901.6:4	DS windowing	Indicates the size of the windowing control for the PMA/PMD in the downstream direction	R/W
1.1901.3:0	DS cyclic prefix	Indicates the size of the cyclic prefix for the PMA/PMD in the downstream direction	R/W

^aR/W = Read/Write**45.2.1.130b.1 CLT tx mute (1.1901.15)**

When bit 1.1901.15 is set to one, the CLT PMD transmitter enters the test mode and it is muted. When bit 1.1901.15 is set to a zero, the CLT PMD enters the normal operating state. This bit has no effect in the CNU. This bit is a reflection of the variable *CLT_TxMute* defined in 100.4.1.

45.2.1.130b.2 DS OFDM channels (1.1901.14:12)

Bits 1.1901.14:12 indicate the integer number of downstream OFDM channels in use. The number is between 1 and 5; where bit 1.1901.12 is the LSB and bit 1.1901.14 is the MSB. These bits are a reflection of the counter *DS_ChCnt* defined in 100.3.2.3.

45.2.1.130b.3 DS time interleaving (1.1901.11:7)

Bits 1.1901.11:7 indicate the integer number of time interleaved OFDM symbols in the downstream direction. The number is between 1 and 32; where bit 1.1901.7 is the LSB and bit 1.1901.11 is the MSB. These bits are a reflection of the variable *DS_TmIntrlv* defined in 101.4.3.9.5.

45.2.1.130b.4 DS windowing (1.1901.6:4)

Bits 1.1901.6:4 indicate the size, in OFDM Clock periods (1/204.8 MHz), of the windowing control for the 10GPASS-XR PMA/PMD in the downstream direction. These bits are a reflection of the variable *DSNrp* defined in 101.4.3.12.1 with bits 1.1901.6:4 mapping to bits 2:0 of *DSNrp*, respectively.

45.2.1.130b.5 DS cyclic prefix (1.1901.3:0)

Bits 1.1901.3:0 indicate the size, in OFDM Clock periods (1/204.8 MHz), of the cyclic prefix control for the 10GPASS-XR PMA/PMD in the downstream direction. These bits are a reflection of the variable *DSNcp* defined in 101.4.3.12.1 with bits 1.1901.3:0 mapping to bits 3:0 of *DSNcp*, respectively.

45.2.1.130c DS OFDM channel frequency control register 1 through 5 (Register 1.1902 through 1.1906)

The assignment of bits in the DS OFDM channel frequency control register 1 through 5 is shown in Table 45–98ac.

Table 45–98ac—DS OFDM channel frequency control register 1 through 5 bit definitions

Bit(s)	Name	Description	R/W ^a
1.1902.15:0	DS OFDM freq ch 1	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 1.	R/W
1.1903.15:0	DS OFDM freq ch 2	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 2.	R/W
1.1904.15:0	DS OFDM freq ch 3	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 3.	R/W
1.1905.15:0	DS OFDM freq ch 4	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 4.	R/W
1.1906.15:0	DS OFDM freq ch 5	This register specifies the center frequency of subcarrier 0 of downstream OFDM channel number 5.	R/W

^aR/W = Read/Write

45.2.1.130c.1 DS OFDM freq ch 1 (1.1902.15:0)

Register 1.1902 specifies the center frequency for OFDM channel number 1 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(1)* defined in 100.3.2.3.

45.2.1.130c.2 DS OFDM freq ch 2 (1.1903.15:0)

Register 1.1903 specifies the center frequency of OFDM channel number 2 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(2)* defined in 100.3.2.3.

45.2.1.130c.3 DS OFDM freq ch 3 (1.1904.15:0)

Register 1.1904 specifies the center frequency of OFDM channel number 3 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(3)* defined in 100.3.2.3.

45.2.1.130c.4 DS OFDM freq ch 4 (1.1905.15:0)

Register 1.1905 specifies the center frequency of OFDM channel number 4 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(4)* defined in 100.3.2.3.

45.2.1.130c.5 DS OFDM freq ch 5 (1.1906.15:0)

Register 1.1906 specifies the center frequency of OFDM channel number 5 in units of 50 kHz. This register is a reflection of the variable *DS_FreqCh(5)* defined in 100.3.2.3.

45.2.1.130d US OFDM control register (Register 1.1907)

The assignment of bits in the US OFDM control register is shown in Table 45–98ad.

Table 45–98ad—US OFDM control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1907.15:8	Random seed	Random back-off seed for PHY Discovery	R/W
1.1907.7	Resource Block size	1 = 16 OFDMA symbols in the upstream OFDMA Resource Block 0 = 8 OFDMA symbols in the upstream OFDMA Resource Block	R/W
1.1907.6:4	US windowing	Indicates the size of the windowing control for the PMA/PMD in the upstream direction	R/W
1.1907.3:0	US cyclic prefix	Indicates the size of the cyclic prefix for the PMA/PMD in the upstream direction	R/W

^aR/W = Read/Write

45.2.1.130d.1 Random seed (1.1907.15:8)

Bits 1.1907.15:8 form an 8-bit integer that is used by the CNU for the seed of the PHY Discovery back-off algorithm. These bits are a reflection of the *Rnd* variable defined in 102.4.1.9.2.

45.2.1.130d.2 Resource Block size (1.1907.7)

Bit 1.1907.7 indicates the number of OFDM symbols in a Resource Block in the upstream direction. This bit is a reflection of the variable *RBsize* defined in 101.4.4.3.5.

45.2.1.130d.3 US windowing (1.1907.6:4)

Bits 1.1907.6:4 indicate the size, in units of OFDM Clock periods (1/204.8 MHz), of the windowing control for the 10GPASS-XR PMA/PMD in the upstream direction. These bits are a reflection of the variable *USNrp* defined in 101.4.4.10.1 with bits 1.1907.6:4 mapping to bits 2:0 of *USNrp*, respectively.

45.2.1.130d.4 US cyclic prefix (1.1907.3:0)

Bits 1.1907.3:0 indicate the size, in units of OFDM Clock periods (1/204.8 MHz), of the cyclic prefix control for the 10GPASS-XR PMA/PMD in the upstream direction. These bits are a reflection of the variable *USNcp* defined in 101.4.4.10.1 with bits 1.1907.3:0 mapping to bits 3:0 of *USNcp*, respectively.

45.2.1.130e US OFDM channel frequency control register (Register 1.1908)

The assignment of bits in the US OFDM channel frequency control register is shown in Table 45–98ae.

Register 1.1908 indicates the center frequency, in units of 50 kHz, of subcarrier 0 for the upstream OFDM channel. This register is a reflection of the variable *US_FreqCh1* defined in 100.3.2.3.

Table 45–98ae—US OFDM channel frequency control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1908.15:0	US OFDM freq	This specifies the center frequency of subcarrier 0 of the upstream OFDM channel.	R/W

^aR/W = Read/Write**45.2.1.130f US OFDMA pilot pattern register (Register 1.1909)**

The assignment of bits in the US OFDMA pilot pattern register is shown in Table 45–98af. For additional information on the use of the parameters in this register see 101.4.4.6.

Table 45–98af—US OFDMA pilot pattern register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1909.15	Reserved	Value always 0	RO
1.1909.14:12	Type 2 repeat	Indicates the number of subcarriers between Type 2 Pilots	R/W
1.1909.11:8	Type 2 start	Indicates the number of the subcarrier on which the Type 2 Pilot pattern starts	R/W
1.1909.7	Reserved	Value always 0	RO
1.1909.6:4	Type 1 repeat	Indicates the number of subcarriers between Type 1 Pilots	R/W
1.1909.3:0	Type 1 start	Indicates the number of the subcarrier on which the Type 1 Pilot pattern starts	R/W

^aRO = Read only, R/W = Read/Write**45.2.1.130f.1 Type 2 repeat (1.1909.14:12)**

Bits 1.1909.14:12 indicate the number of subcarriers between repeating Type 2 Pilots. Additional information on pilot patterns and encoding for these bits is located in 101.4.4.6 and Table 101–14. These bits are a reflection of the variable *Type2_Repeat* defined in 101.4.4.6.1.

45.2.1.130f.2 Type 2 start (1.1909.11:8)

Bits 1.1909.11:8 indicate the number of the first subcarrier designated as a Type 2 Pilot. These bits are a reflection of the variable *Type2_Start* defined in 101.4.4.6.1.

45.2.1.130f.3 Type 1 repeat (1.1909.6:4)

Bits 1.1909.6:4 indicate the number of subcarriers between repeating Type 1 Pilots. Additional information on pilot patterns and encoding for these bits is located in 101.4.4.6 and Table 101–14. These bits are a reflection of the variable *Type1_Repeat* defined in 101.4.4.6.1.

45.2.1.130f.4 Type 1 start (1.1909.3:0)

Bits 1.1909.3:0 indicate the number of the first subcarrier designated as a Type 1 Pilot. These bits are a reflection of the variable *Type1_Start* defined in 101.4.4.6.1.

45.2.1.130g Profile control register (Register 1.1910)

The assignment of bits in the Profile control register is shown in Table 45–98ag. See 102.4.5 for additional information on the profile copy functionality.

Table 45–98ag—Profile control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1910.15:12	Reserved	Value always 0	RO
1.1910.11	US copy in process	1 = the active upstream profile is being copied to the off-line profile 0 = the upstream off-line profile is not being modified by a profile copy	RO
1.1910.10	US profile copy	1 = initiates a copy of the active upstream profile to the off-line profile 0 = no copy initiated	R/W, SC
1.1910.9:8	US configuration ID	Controls switching the active upstream profile	RO
1.1910.7	Reserved	Value always 0	RO
1.1910.6:4	DS copy channel ID	Indicates which of the 5 downstream OFDM channel profiles is to be copied	
1.1910.3	DS copy in process	1 = the active downstream profile is being copied to the off-line profile 0 = the downstream off-line profile is not being modified by a profile copy	RO
1.1910.2	DS profile copy	1 = initiates a copy of the active downstream profile to the off-line profile 0 = normal	R/W, SC
1.1910.1:0	DS configuration ID	Controls switching the active downstream profile	RO

^aR/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.1.130g.1 US copy in process (1.1910.11)

When read as one, bit 1.1910.11 indicates that a copy of the currently active upstream profile to the inactive profile is in process, writes to all upstream profile descriptors and their reflective registers (see 45.2.7a.3 and 102.4.5) are ignored, and switching between profiles (see 102.2.3.1.1) is prohibited. This bit is a reflection of the variable *US_CpyInP* defined in 102.4.5.1.

45.2.1.130g.2 US profile copy (1.1910.10)

When bit 1.1910.10 is set to one, a copy of the currently active upstream profile to the inactive profile is initiated and will continue to completion. This bit is set to zero by the PMA/PMD on or before completion of the profile copy. This bit is a reflection of the variable *US_ProfICpy* defined in 102.4.5.1.

45.2.1.130g.3 US configuration ID (1.1910.9:8)

Bits 1.1910.9:8 indicate the value of the most recently received upstream Configuration ID bits (see 102.2.3.1). These bits are a reflection of the variable *US_CID* defined in 102.2.3.1.1.

45.2.1.130g.4 DS copy channel ID (1.1910.6:4)

Bits 1.1910.6:4 indicate which one of the five downstream ODFM channel profiles is to be copied. These bits are a reflection of the *DS_CpyCh* variable defined in 102.4.5.1.

45.2.1.130g.5 DS copy in process (1.1910.3)

When read as one, bit 1.1910.3 indicates that a copy of the currently active downstream profile to the inactive profile is in process, writes to all downstream profile descriptors and their reflective registers (see 45.2.7a.2 and 102.4.5) are ignored, and switching between profiles (see 102.2.3.1) is prohibited. This bit is a reflection of the variable *DS_CpyInP* defined in 102.4.5.1.

45.2.1.130g.6 DS profile copy (1.1910.2)

When bit 1.1910.2 is set to one, a copy of the currently active downstream profile to the inactive profile is initiated and will continue to completion. This bit is set to zero by the PMA/PMD on or before completion of the profile copy. This bit is a reflection of the variable *UDS_PrfICpy* defined in 102.4.5.1.

45.2.1.130g.7 DS configuration ID (1.1910.1:0)

Bits 1.1910.1:0 indicate the value of the most recently received downstream Configuration ID bits (see 102.2.3.1). These bits are a reflection of the variable *DS_CID* defined in 102.2.7.3.

45.2.1.130h DS PHY Link control register (Register 1.1911)

The assignment of bits in the DS PHY Link control register is shown in Table 45–98ah.

Table 45–98ah—DS PHY Link control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1911.15:12	Reserved	Value always 0	RO
1.1911.11:0	DS PHY Link start	DS PHY Link starting subcarrier	R/W

^aRO = Read only, R/W = Read/Write

45.2.1.130h.1 DS PHY Link start (1.1911.11:0)

Bits 1.1911.11:0 set the starting subcarrier number of the downstream 10GPASS-XR PHY Link. They indicate the lowest frequency subcarrier of the downstream PHY Link used to carry PHY Link information bits. See 102.2 for additional details on the downstream PHY Link. These bits are a reflection of the variable *DS_PhyLinkStrt* defined in 102.2.7.3.

45.2.1.130i US PHY Link control register (Register 1.1912)

The assignment of bits in the US PHY Link control register is shown in Table 45–98ai.

45.2.1.130i.1 US PHY Link modulation (1.1912.15:12)

Bits 1.1912.15:12 are used to set the modulation type of the upstream PHY Link. These bits are a reflection of the *US_PhyLinkMod* variable defined in 102.3.5.3 with bits 1.1912.15:12 mapping to bits 3:0 of *US_PhyLinkMod*, respectively.

Table 45–98ai—US PHY Link control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1912.15:12	US PHY Link modulation	US PHY Link modulation type	R/W
1.1912.11:0	US PHY Link start	US PHY Link starting subcarrier	R/W

^aR/W = Read/Write

45.2.1.130i.2 US PHY Link start (1.1912.11:0)

Bits 1.1912.11:0 set the starting subcarrier number of the upstream 10GPASS-XR PHY Link. They indicate the lowest frequency subcarrier of the upstream PHY Link used to carry PHY Link information bits. See 102.3 for additional details on the upstream PHY Link. These bits are a reflection of the variable *US_PhyLinkStrt* defined in 102.3.5.3.

45.2.1.130j PHY Discovery control registers (Registers 1.1913 and 1.1914)

The PHY Discovery process is used to bring up new CNUs on the EPoC coax cable distribution network. Registers 1.1913 and 1.1914 indicate when the next PHY Discovery window is opened relative to the downstream Timestamp with bit 1.1913.0 being the LSB and bit 1.1914.15 being the MSB. Setting the PHY Discovery start parameter to zero disables the PHY Discovery window. The PHY Discovery control registers direct this process, which is described in 102.4.1. The assignment of bits in the PHY Discovery control registers is shown in Table 45–98aj. These registers are a reflection of the *DiscStrt* variable defined in 102.2.3.2.4

Table 45–98aj—PHY Discovery control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1913.15:0	PHY Discovery start lower	Time of next open PHY Discovery window bits [15:0]	R/W, MW
1.1914.15:0	PHY Discovery start upper	Time of next open PHY Discovery window bits [31:16]	R/W, MW

^a R/W = Read/Write, MW = Multi-word

45.2.1.130k New CNU control register (Register 1.1915)

The assignment of bits in the New CNU control register is shown in Table 45–98ak. Additional information on the use of the New CNU control register can be found in 102.4.1.6 and 102.4.3.

Table 45–98ak—New CNU control register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1915.15	CNU_ID assigned flag	1 = the allowed CNU_ID value has been assigned to a CNU 0 = the allowed CNU_ID value has not been assigned to a CNU	R/W
1.1915.14:0	Allowed CNU_ID	A new CNU may be assigned this value for CNU_ID if the CNU_ID assigned flag is FALSE	R/W

^aR/W = Read/Write

45.2.1.130k.1 CNU_ID assigned flag 1 (1.1915.15)

Bit 1.1915.15 indicates if the associated CNU_ID value has been assigned to a CNU by the PHY. When this bit is set to one, the associated CNU_ID has been assigned to a CNU. When this bit is set to zero the associated CNU_ID has not been assigned. See 102.4.1.6 and 102.4.3 for additional details on the use of this flag. This bit is a reflection of the variable *AssgndCNU_ID* defined in 102.4.1.9.2.

45.2.1.130k.2 Allowed CNU_ID (1.1915.14:0)

Bits 1.1915.14:0 indicate to the 10GPASS-XR PHY a valid CNU_ID value. The value may be assigned to a new CNU when the CNU_ID assigned flag (bit 1.1915.15) is set to zero, when the flag is set to one it is an indication that this value has already been assigned to a CNU and it should not be use for another CNU. These bits are a reflection of the *AllwdCNU_ID* variable defined in 102.4.1.9.2.

45.2.1.130l New CNU info registers 1 through 5 (Registers 1.1916 through 1.1920)

The assignment of bits in the New CNU info registers 1 through 5 is shown in Table 45–98al. Additional information on the use of the New CNU info registers see 102.4.3.

Table 45–98al—New CNU info registers 1 through 5 bit definitions

Bit(s)	Name	Description	R/W ^a
1.1916.15:0	New CNU range	The range of the CNU corresponding to Allowed CNU_ID	RO
1.1917.15:0	New CNU MAC 0	MAC address bits [15:0] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1918.15:0	New CNU MAC 1	MAC address bits [31:16] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1919.15:0	New CNU MAC 2	MAC address bits [47:32] of the CNU corresponding to Allowed CNU_ID	RO, MW
1.1920.15:0	Reserved	Value always 0	RO

^aRO = Read only, MW = Multi-word

45.2.1.130l.1 New CNU range (1.1916.15:0)

Register 1.1916 forms an integer that indicates the range of the CNU corresponding to Allowed CNU_ID (see 102.4.1.6) in units of OFDM Clock periods (1/204.8 MHz). This register is a reflection of the variable *NewCNU_Rng* defined in 102.4.1.9.2.

45.2.1.130l.2 New CNU MAC 0 through 2 (1.1917.15:0 through 1.1919.15:0)

Registers 1.1917 through 1.1919 hold the MAC address of the CNU, as determined by the PHY Discovery process, corresponding to Allowed CNU_ID (see 45.2.1.130k) with bit 1.1917.0 being the LSB and 1.1919.15 being the MSB. These registers are a reflection of the variable *New_MAC* defined in 102.4.1.9.2.

45.2.1.130m DS PHY Link frame counter (Register 1.1921)

Register 1.1921 represents the DS PHY Link frame count. This counter is incremented at the beginning of the PHY Link frame and, on terminal count, rolls over to zero. The assignment of bits in the DS PHY Link frame counter is shown in Table 45–98am.

Table 45–98am—DS PHY Link frame counter bit definitions

Bit(s)	Name	Description	R/W ^a
1.1921.15:0	PHY Link frame counter	Counter that indicates the PHY Link frame currently being processed by the PHY. This counter rolls over to zero and is incremented at the beginning of each PHY Link frame	RO

^aRO = Read only

45.2.1.130n PMA/PMD timing offset register (Registers 1.1922 and 1.1923)

The assignment of bits in the PMA/PMD timing offset registers is shown in Table 45–98an. Registers 1.1923 and 1.1922 form an offset, in units of OFDM Clock periods (1/204.8 MHz), used to align the CNU to the upstream OFDM timing. For more information on the use of this register see 102.4.1.6. These registers are a reflection of the variable *PhyTimingOffset* defined in 102.4.1.9.2.

Table 45–98an—PMA/PMD timing offset register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1922.15:0	PMA/PMD timing offset lower	Transmit timing offset [15:0]	R/W, MW
1.1923.15:0	PMA/PMD timing offset upper	Transmit timing offset [31:16]	R/W, MW

^aR/W = Read/Write, MW = Multi-word

45.2.1.130o PMA/PMD power offset register (Register 1.1924)

The assignment of bits in the PMA/PMD power offset register is shown in Table 45–98ao.

Table 45–98ao—PMA/PMD power offset register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1924.15:8	Reserved	Value always 0	RO
1.1924.7:0	PMA/PMD power offset	TX Power offset	R/W

^a RO = Read Only, R/W = Read/Write

45.2.1.130o.1 PMA/PMD power offset (1.1924.7:0)

Bits 1.1924.7:0 represent a power offset, in units of 0.25 dB, the CNU is to make in order that transmissions arrive at the CLT at the desired power level. For more information on the use of these bits see 102.4.1.6. These bits are a reflection of the variable *PhyPowerOffset* defined in 102.4.1.9.2.

45.2.1.130p PMA/PMD ranging offset registers (Registers 1.1925 and 1.1926)

Registers 1.1925 and 1.1926 represent the PMA/PMD ranging offset parameter, in units of OFDM Clock periods (1/204.8 MHz). The assignment of bits in the PMA/PMD ranging offset register is shown in Table 45–98ap. These registers are a reflection of the variable *PhyRngOffset* defined in 102.4.1.9.2.

Table 45–98ap—PMA/PMD ranging offset registers bit definitions

Bit(s)	Name	Description	R/W ^a
1.1925.15:0	PMA/PMD ranging offset lower	PMA/PMD ranging offset register bits [15:0]	R/W, MW
1.1926.15:0	PMA/PMD ranging offset upper	PMA/PMD ranging offset register bits [31:16]	R/W, MW

^aR/W = Read/Write, MW = Multi-word

45.2.1.130q DS PMA/PMD data rate registers (Registers 1.1927, 1.1928 and 1.1929)

Registers 1.1927, 1.1928, and 1.1929 represent the downstream data rate, in units of b/s. Bit 1.1929.4 is the MSB and bit 1.1927.0 is the LSB of the value. The bit assignments for the DS Data Rate registers is illustrated in Table 45–98aq. These registers are a reflection of the variable *DS_DataRate* defined in 100.3.2.3.

45.2.1.130r US PMA/PMD data rate registers (Registers 1.1930, 1.1931 and 1.1932)

Registers 1.1930, 1.1931, and 1.1932 represent the upstream data rate in units of b/s. Bit 1.1932.4 is the MSB and bit 1.1930.0 is the LSB of the value. The bit assignments for the US Data Rate registers is illustrated in Table 45–98ar. These registers are a reflection of the variable *US_DataRate* defined in 100.3.2.3.

Table 45–98aq—DS PMA/PMD data rate register bit definitions

Bit(s)	Name	Description	R/W ^a
1.1927.15:3	DS PMA/PMD data rate lower	The downstream PMA/PMD data rate bits [15:3] of a UQ34.3 formatted number	RO, MW
1.1927.2:0	DS PMA/PMD data rate fractional	The downstream PMA/PMD data rate bits [2:0] of a UQ34.3 formatted number	RO, MW
1.1928.15:0	DS PMA/PMD data rate mid	The downstream PMA/PMD data rate bits [31:16] of a UQ34.3 formatted number	RO, MW
1.1929.15:5	Reserved	Value always 0	RO
1.1929.4:0	DS PMA/PMD data rate upper	The downstream PMA/PMD data rate bits [36:32] of a UQ34.3 formatted number	RO, MW

^aRO = read only, MW = Multi-word**Table 45–98ar—US PMA/PMD data rate register bit definitions**

Bit(s)	Name	Description	R/W ^a
1.1930.15:3	US PMA/PMD data rate lower	The upstream PMA/PMD data rate bits [15:3] of a UQ34.3 formatted number	RO, MW
1.1930.2:0	US PMA/PMD data rate fractional	The upstream PMA/PMD data rate bits [2:0] of a UQ34.3 formatted number	RO, MW
1.1931.15:0	US PMA/PMD data rate mid	The upstream PMA/PMD data rate bits [31:16] of a UQ34.3 formatted number	RO, MW
1.1932.15:5	Reserved	Value always 0	RO
1.1932.4:0	US PMA/PMD data rate upper	The upstream PMA/PMD data rate bits [36:32] of a UQ34.3 formatted number	RO, MW

^aRO = read only, MW = Multi-word**45.2.1.130s 10GPASS-XR FEC codeword counter (Registers 1.1933, 1.1934)**

The assignment of bits in the 10GPASS-XR FEC codeword counter is shown in Table 45–98as. Registers 1.1933 and 1.1934 are used to read the value of a 32-bit counter. When registers 1.1933 and 1.1934 are used to read the 32-bit counter value, the register 1.1933 is read first, the value of the register 1.1934 is latched when (and only when) register 1.1933 is read and reads of register 1.1934 return the latched value rather than the current value of the counter. These registers are a reflection of the variable *FecCodeWordCount* defined in 101.3.3.1.6.

Table 45–98as—10GPASS-XR FEC codeword counter bit definitions

Bit(s)	Name	Description	R/W ^a
1.1933.15:0	FEC codeword counter lower	Total FEC codewords counter [15:0]	RO, MW
1.1934.15:0	FEC codeword counter upper	Total FEC codewords counter [31:0]	RO, MW

^aRO = Read only, MW = Multi-word