
**Information technology —
Telecommunications and information
exchange between systems — Local
and metropolitan area networks —
Specific requirements —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 7: Media access control
parameters, physical layers, and
management parameters for 2.5 Gb/s
and 5 Gb/s operation, types 2.5GBASE-T
and 5GBASE-T**

*Technologies de l'information — Télécommunications et échange
d'information entre systèmes — Réseaux locaux et métropolitains —
Prescriptions spécifiques —*

Partie 3: Norme pour Ethernet

*AMENDEMENT 7: Paramètres de commandes d'accès aux
supports, couches physiques et paramètres de gestion en vue d'un
fonctionnement à 2,5 Gb/s et à 5 Gb/s, de types 2.5GBASE-T et
5GBASE-T*





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IEEE Std 802.3bz™-2016

(Amendment to
IEEE Std 802.3™-2015
as amended by
IEEE Std 802.3bw™-2015,
IEEE Std 802.3by™-2016,
IEEE Std 802.3bq™-2016,
IEEE Std 802.3bp™-2016,
IEEE Std 802.3br™-2016, and
IEEE Std 802.3bn™-2016)

IEEE Standard for Ethernet

Amendment 7: Media Access Control Parameters, Physical Layers, and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation, Types 2.5GBASE-T and 5GBASE-T

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 22 September 2016
IEEE-SA Standards Board

Abstract: Ethernet Media Access Control (MAC) parameters, Physical Layer specifications, and management objects for the transfer of Ethernet format frames at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair transmission media used in structured cabling are defined in this amendment to IEEE Std 802.3-2015.

Keywords: 2.5G/5GBASE-T, amendment, Auto-Negotiation, Ethernet, IEEE 802.3™, IEEE 802.3bz™, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, structured cabling, XGMII

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Introduction

This introduction is not part of IEEE Std 802.3bz-2016, IEEE Standard for Ethernet—Amendment 7: Media Access Control Parameters, Physical Layers, and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation, Types 2.5GBASE-T and 5GBASE-T.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2015 and are not maintained as separate documents.

At the date of IEEE Std 802.3bz-2016 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2015

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

IEEE Std 802.3bw-2015

Amendment 1—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

IEEE Std 802.3by-2016

Amendment 2—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 105 through Clause 112, Annex 109A, Annex 109B, Annex 110A, Annex 110B, and Annex 110C. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 25 Gb/s.

IEEE Std 802.3bq-2016

Amendment 3—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 113 and Annex 113A. This amendment adds new Physical Layers for 25 Gb/s and 40 Gb/s operation over balanced twisted-pair structured cabling systems.

IEEE Std 802.3bp-2016

Amendment 4—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 97 and Clause 98. This amendment adds point-to-point 1 Gb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable in automotive and other applications not utilizing the structured wiring plant.

IEEE Std 802.3br-2016

Amendment 5—This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 99. This amendment adds a MAC Merge sublayer and a MAC Merge Service Interface to support for Interspersing Express Traffic over a single link.

IEEE Std 802.3bn-2016

Amendment 6—This amendment adds the Physical Layer specifications and management parameters for symmetric and/or asymmetric operation of up to 10 Gb/s on point-to-multipoint Radio Frequency (RF) distribution plants comprising either amplified or passive coaxial media. It also extends the operation of Ethernet Passive Optical Networks (EPON) protocols, such as Multipoint Control Protocol (MPCP) and Operation Administration and Management (OAM).

IEEE Std 802.3bz™-2016

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 125 and Clause 126. This amendment adds new rates of 2.5 Gb/s and 5 Gb/s and new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over balanced twisted-pair structured cabling systems.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.¹

The editing instructions are shown in **bold italic**. Four editing instructions are used: change, delete, insert, and replace. **Change** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). **Delete** removes existing material. **Insert** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. **Replace** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Change item f) XGMII as follows:

- f) *10 Gigabit Media Independent Interface (XGMII).* The XGMII is designed to connect a 2.5 Gb/s, 5 Gb/s, or 10 Gb/s capable MAC to a 10 Gb/s PHY of the same rate. While conformance with implementation of this interface is not necessary to ensure communication, it allows maximum flexibility in intermixing PHYs and DTEs at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s speeds. The XGMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XGMII. The XGMII is optional.

1.3 Normative references

Insert the following reference in alphanumeric order:

TIA TSB-5021, Guidelines for the Assessment and Mitigation of Installed Cabling to Support 2.5GBASE-T and 5GBASE-T.

1.4 Definitions

Insert the definitions for 2.5GBASE-T after the definition for 1.4.64 10/10G-EPON and before the definition for 25GBASE, inserted by IEEE Std 802.3by-2016:

1.4.64aa 2.5GBASE-T: IEEE 802.3 Physical Layer specification for a 2.5 Gb/s LAN using four pairs of Category 5e/Class D balanced copper cabling. (See IEEE Std 802.3, Clause 126.)

Insert the definitions for 5GBASE-T after the definition for 1.4.72a 40GBASE-T, inserted by IEEE Std 802.3bq-2016:

1.4.72b 5GBASE-T: IEEE 802.3 Physical Layer specification for a 5 Gb/s LAN using four pairs of Category 5e/Class D balanced copper cabling. (See IEEE Std 802.3, Clause 126.)

Change the definition for 10 Gigabit Media Independent Interface (XGMII) as follows:

1.4.76 10 Gigabit Media Independent Interface (XGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation. (See IEEE Std 802.3, Clause 46.)

Insert a new definition for Category 5e balanced cabling, after Category 5 balanced cabling as follows:

1.4.127a Category 5e balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz per ISO/IEC 11801:2002 and ANSI/TIA-568-B.2-2001. (See IEEE Std 802.3, [Clause 14](#), [Clause 25](#), [Clause 40](#), [Clause 33](#), and Clause 126.)

Change the definition for Category 6 balanced cabling, as follows:

1.4.128 Category 6 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 250 MHz per ISO/IEC 11801:2002 and ANSI/TIA-568-C.2-2009. (See IEEE Std 802.3, Clause 14, Clause 25, Clause 40, Clause 55, Clause 33, and Clause 126.) (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002 and ANSI/TIA-568-C.2). In addition to the requirements outlined in ISO/IEC 11801:1995 and ANSI/TIA-568-C.2, IEEE 802.3 Clause 14, Clause 23, Clause 25, Clause 40, and Clause 55 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T, and 10GBASE-T. ~~Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 100 MHz per ISO/IEC 11801:2002 and ANSI/TIA-568-B.2-2001.~~

Change the definition for Category 6A balanced cabling, as follows:

1.4.129 Category 6A balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 500 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002 Amendment 2 and ANSI/TIA-568-C.2). In addition to the requirements outlined in ISO/IEC 11801:2002 Amendment 2 and ANSI/TIA-568-C.2, IEEE 802.3 Clause 14, Clause 23, Clause 25, Clause 40, and Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

Change the definition for Category 7 balanced cabling, as follows:

1.4.130 Category 7 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 600 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002). In addition to the requirements outlined in ISO/IEC 11801:2002, IEEE 802.3 Clause 14, Clause 23, Clause 25, Clause 40, and Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

Change the definition for Category 7A balanced cabling, as follows:

1.4.131 Category 7A balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 1000 MHz (i.e., cabling components meet the performance specified in ISO/IEC 11801:2002 Amendment 2). In addition to the requirements outlined in ISO/IEC 11801:2002 Amendment 2, IEEE 802.3 Clause 14, Clause 23, Clause 25, Clause 40, and Clause 55, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, 100BASE-T, 2.5GBASE-T, 5GBASE-T, and 10GBASE-T.

Change the definition for Category 8 balanced cabling (as inserted by IEEE Std 802.3bq-2016) as follows:

1.4.131a Category 8 balanced cabling: Balanced 100 Ω cables and associated connecting hardware whose transmission characteristics are specified up to 2000 MHz (i.e., cabling components that meet the Category 8.1 or Category 8.2 requirements specified in ISO/IEC 11801-1 or Category 8 specified in ANSI/TIA-568-C.2-1). In addition to the requirements outlined in ISO/IEC 11801-1 and ANSI/TIA-568-C.2-1, IEEE Std 802.3 Clause 14, Clause 23, Clause 25, Clause 40, Clause 55, and Clause 113, and Clause 126 specify additional requirements for this cabling when used with 10BASE-T, ~~100BASE-T~~ 100BASE-T4, 100BASE-TX, 1000BASE-T, 2.5GBASE-T, 5GBASE-T, 10GBASE-T, 25GBASE-T, and 40GBASE-T.

Change the definition for Infocfield (as inserted by IEEE Std 802.3bq-2016) as follows:

1.4.237a Infocfield: A sixteen octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 55, and Clause 113, and Clause 126.)

Change the definition for MultiGBASE-T (as inserted by IEEE Std 802.3bq-2016) as follows:

1.4.277a MultiGBASE-T: PHYs that belong to the set of specific BASE-T Ethernet PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T, 5GBASE-T, 10GBASE-T, 25GBASE-T, and 40GBASE-T. [See IEEE Std 802.3, Clause 126 (for both 2.5GBASE-T and 5GBASE-T), Clause 55 (10GBASE-T), and Clause 113 (for both 25GBASE-T and 40GBASE-T).]

1.5 Abbreviations

Insert the following new abbreviation into the abbreviations list, in alphanumeric order:

ALSNR	alien limited signal-to-noise ratio
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4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows, inserting a new column between 1 Gb/s and 10 Gb/s, and deleting rightmost column (25 Gb/s, 40Gb/s, and 100 Gb/s) (as modified by IEEE Std 802.3by-2016):

Table 4–2—MAC parameters

Parameters	MAC data rate				
	Up to and including 100 Mb/s	1 Gb/s	<u>2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, and 100 Gb/s</u>	10 Gb/s	25 Gb/s, 40 Gb/s, and 100 Gb/s
slotTime	512 bit times	4096 bit times	<u>not applicable</u>	not applicable	not applicable
interPacketGap ^a	96 bits	96 bits	<u>96 bits</u>	96 bits	96 bits
attemptLimit	16	16	<u>not applicable</u>	not applicable	not applicable
backoffLimit	10	10	<u>not applicable</u>	not applicable	not applicable
jamSize	32 bits	32 bits	<u>not applicable</u>	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	<u>1518 octets</u>	1518 octets	1518 octets
maxEnvelopeFrame-Size	2000 octets	2000 octets	<u>2000 octets</u>	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	<u>512 bits (64 octets)</u>	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	<u>not applicable</u>	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	<u>not applicable</u>	104 bits	not applicable

^aReferences to interFrameGap or interFrameSpacing in other clauses (e.g., [Clause 13](#), [Clause 35](#), and [Clause 42](#)) shall be interpreted as interPacketGap.

Change NOTE 4 (as modified by IEEE Std 802.3by-2016) as follows:

NOTE 4—For 2.5 Gb/s, 5 Gb/s, 10 Gb/s, and 25 Gb/s operation, the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet, can have a minimum value of 40 BT (bit times), as measured at the XGMII or 25GMII receive signals at the DTE. This interpacket gap shrinkage may be caused by variable network delays and clock tolerances.

28. Physical Layer link signaling for Auto-Negotiation on twisted pair

28.3 State diagrams and variable definitions

28.3.1 State diagram variables

Insert new rows for 2p5GigT and 5GigT in the first list in 28.3.1 (as modified by IEEE Std 802.3bq-2016) above the row for 10GigT as follows:

2p5GigT; represents that the 2.5GBASE-T PMA is the signal source.

5GigT; represents that the 5GBASE-T PMA is the signal source.

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entries in "APPROPRIATE SYNTAX" after 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016):

2.5GBASE-T	Clause 126 2.5 Gb/s PAM16
5GBASE-T	Clause 126 5 Gb/s PAM16

30.3.2.1.3 aPhyTypeList

Insert the following new entries in "APPROPRIATE SYNTAX" after 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016):

2.5GBASE-T	Clause 126 2.5 Gb/s PAM16
5GBASE-T	Clause 126 5 Gb/s PAM16

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in "APPROPRIATE SYNTAX" after 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016):

2.5GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 126
5GBASE-T	Four-pair twisted-pair balanced copper cabling PHY as specified in Clause 126

30.5.1.1.4 aMediaAvailable

Change the eighth paragraph of 30.5.1.1.4 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bq-2016) as follows:

For 2.5 Gb/s, 5 Gb/s, 10 Gb/s, and 25 Gb/s the enumerations map to value of the link_fault variable within the Link Fault Signaling state diagram (Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration “available”, the value Local Fault maps to the enumeration “not available” and the value Remote Fault maps to the enumeration “remote fault”.

30.5.1.1.24 aLDFastRetrainCount

Change 30.5.1.1.24 aLDFastRetrainCount (as modified by IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T [as part of the Energy-Efficient Ethernet package (optional)] as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of fast retrains initiated by the local device. The counter can be derived from fr_tx_counter (see 55.4.5.4, and 113.4.5.4, and 126.4.5.4). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from the LD fast retrain count register (see 45.2.1.79.2).;

30.5.1.1.25 aLPFastRetrainCount

Change 30.5.1.1.25 aLPFastRetrainCount (as modified by IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T [as part of the Energy-Efficient Ethernet package (optional)] as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

Generalized nonresettable counter. This counter has a maximum increment rate of 1000 counts per second

BEHAVIOUR DEFINED AS:

A count of the number of fast retrains initiated by the link partner. The counter can be derived from fr_rx_counter (see 55.4.5.4, and 113.4.5.4, and 126.4.5.4). If a Clause 45 MDIO Interface to the PMA/PMD is present, then this attribute can be derived from the LP fast retrain count register (see 45.2.1.79.1).;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entries in "APPROPRIATE SYNTAX" after 1000BASE-T1 (inserted by IEEE Std 802.3bp-2016):

2.5GBASE-T	2.5GBASE-T PHY as specified in Clause 126
5GBASE-T	5GBASE-T PHY as specified in Clause 126

45. Management Data Input/Output (MDIO) Interface

45.1 Overview

Change third paragraph of 45.1 as follows:

This extension to the MDIO interface is applicable to the following:

- Implementations that operate at speeds of 2.5~~10~~ Gb/s and above.

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Insert rows for 1.20 and 1.21 and change the reserved row for 1.20 through 1.29 in Table 45–3, (as modified by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
<u>1.20</u>	<u>Reserved</u>	
<u>1.21</u>	<u>2.5G/5G PMA/PMD extended ability</u>	<u>45.2.1.14c</u>
1.20 <u>22</u> through 1.29	Reserved	

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change Table 45–4 (as modified by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit	Name	Description	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved 0 1 1 x = Reserved 0 1 1 1 = 5 Gb/s <u>0 1 1 0 = 2.5 Gb/s</u> 0 1 0 1 = Reserved 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the first sentence of the last paragraph of 45.2.1.1.3 (as modified by IEEE Std 802.3by-2016) as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected.

45.2.1.4 PMA/PMD speed ability (Register 1.4)

Change the Reserved row for 1.4.15:12 in Table 45–6 (as modified by IEEE Std 802.3by-2016) and insert rows for 1.4.14, 1.4.13, and 1.4.12 as follows (unchanged rows not shown):

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.4.15:12	Reserved for future speeds	Value always 0	RO
<u>1.4.14</u>	<u>5G capable</u>	<u>1 = PMA/PMD is capable of operating at 5 Gb/s</u> <u>0 = PMA/PMD is not capable of operating as 5 Gb/s</u>	<u>RO</u>
<u>1.4.13</u>	<u>2.5G capable</u>	<u>1 = PMA/PMD is capable of operating at 2.5 Gb/s</u> <u>0 = PMA/PMD is not capable of operating as 2.5 Gb/s</u>	<u>RO</u>
<u>1.4.12</u>	<u>Reserved for future speeds</u>	<u>Value always 0</u>	<u>RO</u>

^aRO = Read only

Insert 45.2.1.4.aa and 45.2.1.4.ab before 45.2.1.4.a (inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.4.aa 5G capable (1.4.14)

When read as a one, bit 1.4.14 indicates that the PMA/PMD is able to operate at a data rate of 5 Gb/s. When read as a zero, bit 1.4.14 indicates that the PMA/PMD is not able to operate at a data rate of 5 Gb/s.

45.2.1.4.ab 2.5G capable (1.4.13)

When read as a one, bit 1.4.13 indicates that the PMA/PMD is able to operate at a data rate of 2.5 Gb/s. When read as a zero, bit 1.4.13 indicates that the PMA/PMD is not able to operate at a data rate of 2.5 Gb/s.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the description for bit 1.7.5:0 in Table 45–7 (as modified by IEEE Std 802.3bw-2015, IEEE Std 802.3bp-2016, IEEE Std 802.3by-2016, and IEEE Std 802.3bq-2016) as follows and adjust reserved rows as appropriate (unchanged rows not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 <u>1 1 0 0 0 1 = 5GBASE-T PMA</u> <u>1 1 0 0 0 0 = 2.5GBASE-T PMA</u>	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert description location for 2.5GBASE-T and 5GBASE-T before the row for 10GBASE-KR in Table 45–9 as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
2.5GBASE-T, 5GBASE-T	126.4.2.2

45.2.1.7.5 Receive fault (1.8.10)

Insert description location for 2.5GBASE-T and 5GBASE-T above the row for 10GBASE-KR in Table 45–10 as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
2.5GBASE-T, 5GBASE-T	126.4.2.4

45.2.1.8 PMD transmit disable register (Register 1.9)

Insert description location for 2.5GBASE-T and 5GBASE-T after the row for 10GBASE-KR in Table 45–12 as follows (unchanged rows not shown):

Table 45–12—Transmit disable description location

PMA/PMD	Description location
2.5GBASE-T and 5GBASE-T	126.4.2.3

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change the Reserved row for 1.11.15:13 in Table 45–14 (as modified by IEEE Std 802.3by-2016) and insert rows for 1.11.14 and 1.11.13 as follows (unchanged rows not shown):

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.11.15:13	Reserved	Value always zero	RO
1.11.14	2.5G/5G extended abilities	1 = PMA/PMD has 2.5G/5G extended abilities listed in register 1.21 0 = PMA/PMD does not have 2.5G/5G extended abilities	RO
1.11.13	Reserved	Value always zero	RO

^aRO = Read only

Insert 45.2.1.10.aaa before 45.2.1.10.aa (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.10.aaa 2.5G/5G extended abilities (1.11.14)

When read as a one, bit 1.11.14 indicates that the PMA/PMD has 2.5G/5G extended abilities listed in register 1.21. When read as a zero, bit 1.11.14 indicates that the PMA/PMD does not have 2.5G/5G extended abilities.

Insert 45.2.1.14c after 45.2.1.14b (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.1.14c 2.5G/5G PMA/PMD extended ability register (Register 1.21)

The assignment of bits in the 2.5G/5G PMA/PMD extended ability register is shown in Table 45–17c. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

45.2.1.14c.1 5GBASE-T ability (1.21.1)

When read as a one, bit 1.21.1 indicates that the PMA/PMD is able to operate as a 5GBASE-T PMA type. When read as a zero, bit 1.21.1 indicates that the PMA is not able to operate as a 5GBASE-T PMA type.

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Table 45–17c—2.5G/5G PMA/PMD extended ability register bit definitions

Bit	Name	Description	R/W ^a
1.21.15:2	Reserved	Value always 0	RO
1.21.1	5GBASE-T ability	1 = PMA/PMD is able to perform 5GBASE-T 0 = PMA/PMD is not able to perform 5GBASE-T	RO
1.21.0	2.5GBASE-T ability	1 = PMA/PMD is able to perform 2.5GBASE-T 0 = PMA/PMD is not able to perform 2.5GBASE-T	RO

^aRO = Read only

45.2.1.14c.2 2.5GBASE-T ability (1.21.0)

When read as a one, bit 1.21.0 indicates that the PMA/PMD is able to operate as a 2.5GBASE-T PMA type. When read as a zero, bit 1.21.0 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-T PMA type.

45.2.1.62 MultiGBASE-T status (Register 1.129)

45.2.1.62.1 LP information valid (1.129.0)

Change the text of 45.2.1.62.1 (as modified by IEEE Std 802.3bq-2016) to add references 2.5G/5GBASE-T as follows:

When read as a one, bit 1.129.0 indicates that the startup protocol defined in 55.4.2.5 (for 10GBASE-T), ~~or 113.4.2.5 (for 25G/40GBASE-T), or 126.4.2.5 (for 2.5G/5GBASE-T)~~ has been completed, and that the contents of bits 1.130.11:0, 1.131.15:10, 1.145.14:8, 1.146.14:8, and 1.146.6:0, which are established during the startup protocol, are valid. When read as a zero, bit 1.129.0 indicates that the startup process has not been completed, and that the contents of these bits that are established during the startup protocol are invalid. A PMA in the MultiGBASE-T set shall return a value of zero in bit 1.129.1 if PMA link_status=FAIL.

45.2.1.64 MultiGBASE-T TX power backoff and PHY short reach setting (Register 1.131)

45.2.1.64.1 MultiGBASE-T TX power backoff settings (1.131.15:10)

Change the text of 45.2.1.64.1 (as modified by IEEE Std 802.3bq-2016) to reference 2.5GBASE-T and 5GBASE-T as follows:

The MultiGBASE-T TX power backoff settings reflects the TX power backoff selected during the startup negotiation process. The 10GBASE-T startup negotiation process and all TX power backoff settings are defined in 55.4.2.5 and 55.4.5.1. The 25GBASE-T and 40GBASE-T startup negotiation process and all TX power backoff settings are defined in 113.4.2.5 and 113.4.5.1. For 2.5GBASE-T and 5GBASE-T, startup negotiation process and all TX power backoff settings are defined in 126.4.2.5 and 126.4.5.1. If LP information valid bit, 1.129.0, is set to one then bits 1.131.15:13 indicates the TX power backoff setting of the link partner and bits 1.131.12:10 indicates the TX power backoff setting of the local device.

45.2.1.65 MultiGBASE-T test mode register (Register 1.132)

45.2.1.65.1 Test mode control (1.132.15:13)

Change text of 45.2.1.65.1 (as modified by IEEE Std 802.3bq-2016) to include references to 2.5G/5GBASE-T and Clause 126 as follows:

Transmitter test mode operations defined by bits 1.132.15:13, are described for 10GBASE-T in 55.5.2 and Table 55–12, for 2.5G/5GBASE-T in 126.5.2 and Table 126–13, and for 25G/40GBASE-T in 113.5.2 and Table 113–17. The default value for bits 1.132.15:13 is zero.

45.2.1.65.2 Transmitter test frequencies (1.132.12:10)

Change text of 45.2.1.65.2 (as modified by IEEE Std 802.3bq-2016) to include references to 2.5G/5GBASE-T and Clause 126 as follows:

When test mode 4 is selected by setting bits 1.132.15:13 to one, zero, zero respectively, bits 1.132.12:10 select the transmit test frequency as follows in Table 45–57. Detailed use and operation of these transmitter test frequencies is described in 55.5.2, and 113.5.2, and 126.5.2.

45.2.1.74 RX signal power channel A register (Register 1.141)

Change the text of 45.2.1.74 (as modified by IEEE Std 802.3bq-2016) to add reference to 2.5G/5GBASE-T specifications as follows:

The RX signal power channel A register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, and 113.4.3.1, and 126.4.6.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see 55.4.6.1, and 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.75 RX signal power channel B register (Register 1.142)

Change the text of 45.2.1.75 (as modified by IEEE Std 802.3bq-2016) to add reference to 2.5G/5GBASE-T specifications as follows:

The RX signal power channel B register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, and 113.4.3.1, and 126.4.6.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see 55.4.6.1, and 113.4.6.1, and 126.4.6.1), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of –20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.76 RX signal power channel C register (Register 1.143)

Change the text of 45.2.1.76 (as modified by IEEE Std 802.3bq-2016) to add reference to 2.5G/5GBASE-T specifications as follows:

The RX signal power channel C register is read only and contains the receive signal power measured at the MDI during training as described in 55.4.3.1, and 113.4.3.1, and 126.4.6.1. The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or

MA_Training_Init_S (as appropriate, see [55.4.6.1](#), ~~and 113.4.6.1~~, and [126.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.77 RX signal power channel D register (Register 1.144)

Change the text of 45.2.1.77 (as modified by IEEE Std 802.3bq-2016) to add reference to 2.5G/5GBASE-T specifications as follows:

The RX signal power channel D register is read only and contains the receive signal power measured at the MDI during training as described in [55.4.3.1](#), ~~and 113.4.3.1~~, and [126.4.6.1](#). The RX signal power should reflect the power measured when the device transitions out of the state PMA_Training_Init_M or MA_Training_Init_S (as appropriate, see [55.4.3.1](#), ~~and 113.4.6.1~~, and [126.4.6.1](#)), when the link partner is transmitting with PBO_tx = 4 (8 dB power backoff). It is reported in units of 0.1 dB to an accuracy of 0.5 dB within the range of -20 dBm to 5.5 dBm. The number is in offset two's complement notation, with 0.0 dB represented by 0x8000. Implementation of this register is optional.

45.2.1.78 MultiGBASE-T skew delay register (Registers 1.145 and 1.146)

Change the text of 45.2.1.78 (as modified by IEEE Std 802.3bq-2016) to reference 2.5G/5GBASE-T as follows:

The skew delay register reports the current skew delay on each of the pair with respect to physical pair A (see [Table 45-58](#)). It is reported with resolution equal to one symbol period (see [55.1.3](#), ~~and 113.1.2~~, and [126.1.3](#)) of the PHY (e.g., 1.25 ns for 10GBASE-T) to an accuracy of two symbol periods (e.g., 2.5 ns for 10GBASE-T). The number reported is in two's complement notation with positive values representing delay and negative values representing advance with respect to physical pair A. If the delay exceeds the maximum amount that can be represented by the range (-64 symbols to +63 symbols), the field displays the maximum respective value. The value shall be updated at least once per second.

45.2.1.79 MultiGBASE-T fast retrain status and control register (Register 1.147)

45.2.1.79.1 LP fast retrain count (1.147.15:11)

Change the text of 45.2.1.79.1 (as modified by IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T as follows:

These bits map to fr_rx_counter as defined in [55.4.5.4](#) for 10GBASE-T, ~~and 113.4.5.4~~ for 25GBASE-T and 40GBASE-T, and [126.4.5.4](#) for 2.5GBASE-T and 5GBASE-T. The counter is a 5-bit count of the number of fast retrains requested by the link partner. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.79.2 LD fast retrain count (1.147.10:6)

Change the text of 45.2.1.79.2 (as modified by IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T as follows:

These bits map to fr_tx_counter as defined in [55.4.5.4](#) for 10GBASE-T, ~~and 113.4.5.4~~ for 25GBASE-T and 40GBASE-T, and [126.4.5.4](#) for 2.5GBASE-T and 5GBASE-T. The counter is a 5-bit count of the number of fast retrains requested by the local device. These bits shall be reset to all zeros when read or upon execution of the PMA reset. These bits shall be held at all ones in the case of overflow.

45.2.1.79.5 Fast retrain signal type (1.147.2:1)

Change the text of 45.2.1.79.5 (as modified by IEEE Std 802.3bq-2016) to add reference to 126.3.6.2.2 as follows:

For PHYs that support fast retrain, these bits map to fr_sigtype as defined in [55.3.6.2.2](#), ~~and 113.3.6.2.2~~, and [126.3.6.2.2](#). When Fast retrain signal type is set to 00, the PMA sends IDLE characters on the receive path during fast retrain. When Fast retrain signal type is set to 01, the PMA sends Local Fault on the receive path during fast retrain. When Fast retrain signal type is set to 10, the PMA sends Link Interruption on the receive path during fast retrain.

45.2.1.79.6 Fast retrain enable (1.147.0)

Change the text of 45.2.1.79.6 (as modified by IEEE Std 802.3bq-2016) to add reference to 126.4.5.1 as follows:

For PHYs that support fast retrain, ~~this bit 1.147.0~~ controls fr_enable as defined in [55.4.5.1](#), ~~and 113.4.5.1~~, and [126.4.5.1](#). When PMA reset is executed, this bit is set to one.

NOTE—Setting this bit to zero while a link is up will cause the PHY to stop supporting fast retrain, and the link will drop if the link partner initiates a fast retrain.

45.2.3 PCS registers

45.2.3.1 PCS control 1 register (Register 3.0)

Change the description for bit 3.0.5:2 in Table 45–120 (as modified by IEEE Std 802.3by-2016) as follows, and adjust reserved rows as appropriate (unchanged rows not shown):

Table 45–120—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = Reserved 1 0 0 0 = 5 Gb/s 0 1 1 1 = 2.5 Gb/s 0 1 1 0 = Reserved	R/W

^aR/W = Read/Write

Change the text of 45.2.3.1.2 (as modified by IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T as follows:

45.2.3.1.2 Loopback (3.0.14)

When any MultiGBASE-T or the 10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 10GBASE-R, 10GBASE-T₁ or any PCS in the MultiGBASE-T set shall accept data on the transmit path and return it on the receive path. The speed of the loopback is selected by the PCS control 1 (Register 3.0) defined in 45.2.3.1. The specific behavior of the 10GBASE-R PCS during loopback is specified in [49.2](#). The specific behavior for the 10GBASE-T PCS during loopback is

specified in 55.3.6.3. The specific behavior for the 25GBASE-T and 40GBASE-T PCS during loopback is specified in 113.3.7.3. The specific behavior for the 2.5GBASE-T or 5GBASE-T PCS during loopback is specified in 126.3.7.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

45.2.3.4 PCS speed ability register (Register 3.4)

Change Table 45–122 (as modified by IEEE Std 802.3by-2016) as follows (unchanged rows not shown):

Table 45–122—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W ^a
3.4.15:58	Reserved for future speeds	Value always 0	RO
<u>3.4.7</u>	<u>5G capable</u>	<u>1 = PCS is capable of operating at 5 Gb/s</u> <u>0 = PCS is not capable of operating at 5 Gb/s</u>	<u>RO</u>
<u>3.4.6</u>	<u>2.5G capable</u>	<u>1 = PCS is capable of operating at 2.5 Gb/s</u> <u>0 = PCS is not capable of operating at 2.5 Gb/s</u>	<u>RO</u>
<u>3.4.5</u>	<u>Reserved</u>	<u>Value always 0</u>	<u>RO</u>

^aRO = Read only

Insert 45.2.3.4.6 and 45.2.3.4.7 after 45.2.3.4.5 (as inserted by IEEE Std 802.3by-2016) as follows:

45.2.3.4.6 2.5G capable (3.4.6)

When read as a one, bit 3.4.6 indicates that the PCS is able to operate at a data rate of 2.5 Gb/s. When read as a zero, bit 3.4.6 indicates that the PCS is not able to operate at a data rate of 2.5 Gb/s.

45.2.3.4.7 5G Capable (3.4.7)

When read as a one, bit 3.4.7 indicates that the PCS is able to operate at a data rate of 5 Gb/s. When read as a zero, bit 3.4.7 indicates that the PCS is not able to operate at a data rate of 5 Gb/s.

45.2.3.6 PCS control 2 register (Register 3.7)

Change the description for bit 3.7.3:0 in Table 45–123 (as modified by IEEE Std 802.3bq-2016) as follows (unchanged rows not shown):

Table 45–123—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.7.3:0	PCS type selection	3 2 1 0 1 0 1 x reserved 1 0 1 1 = Select 5GBASE-T PCS type 1 0 1 0 = Select 2.5GBASE-T PCS type	R/W

^aR/W = Read/Write

45.2.3.7 PCS status 2 register (Register 3.8)

Change Table 45–124 as follows (unchanged rows not shown):

Table 45–124—PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.8.13:12	Reserved 5GBASE-T capable	Value always 0 1 = PCS is able to support 2.5GBASE-T PCS type 0 = PCS is not able to support 2.5GBASE-T PCS type	RO
3.8.12	2.5GBASE-T capable	1 = PCS is able to support 5GBASE-T PCS type 0 = PCS is not able to support 5GBASE-T PCS type	RO

^aRO = Read only, LH = Latching high

Insert 45.2.3.7.1a and 45.2.3.7.1b after 45.2.3.7.1 as follows:

45.2.3.7.1a 5GBASE-T capable (3.8.13)

When read as a one, bit 3.8.13 indicates that the PCS is able to support the 5GBASE-T PCS type. When read as a zero, bit 3.8.13 indicates that the PCS is not able to support the 5GBASE-T PCS type.

45.2.3.7.1b 2.5GBASE-T capable (3.8.12)

When read as a one, bit 3.8.12 indicates that the PCS is able to support the 2.5GBASE-T PCS type. When read as a zero, bit 3.8.12 indicates that the PCS is not able to support the 2.5GBASE-T PCS type.

45.2.3.9a EEE control and capability 2 register (Register 3.21)

Change Table 45–125a (as inserted by IEEE Std 802.3bq-2016) as follows:

Table 45–125a—EEE control and capability 2 register

Bit(s)	Name	Description	R/W ^a
3.21.1	5GBASE-T EEE	1 = EEE is supported for 5GBASE-T 0 = EEE is not supported for 5GBASE-T	RO
3.21.4:0	Reserved 2.5GBASE-T EEE	Value always 0 1 = EEE is supported for 2.5GBASE-T 0 = EEE is not supported for 2.5GBASE-T	RO

^a RO = Read only

Insert 45.2.3.9a.2 and 45.2.3.9a.3 after 45.2.3.9a.1 (as inserted by IEEE Std 802.3bq-2016) as follows:

45.2.3.9a.2 5GBASE-T EEE supported (3.21.1)

If the device supports EEE operation for 5GBASE-T as defined in 126.1.3.3, bit 3.21.1 shall be set to one.

45.2.3.9a.3 2.5GBASE-T EEE supported (3.21.0)

If the device supports EEE operation for 2.5GBASE-T as defined in 126.1.3.3, bit 3.21.0 shall be set to one.

45.2.3.13 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)**45.2.3.13.1 BASE-R and MultiGBASE-T receive link status (3.32.12)**

Change the text of 45.2.3.13.1 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bq-2016) to reference 2.5GBASE-T and 5GBASE-T as follows:

When read as a one, bit 3.32.12 indicates that the PCS is in a fully operational state. When read as a zero, bit 3.32.12 indicates that the PCS is not fully operational. This bit is a reflection of the PCS_status variable defined in [49.2.14.1](#) for 10/25GBASE-R, in [126.3.7.1](#) for 2.5GBASE-T and 5GBASE-T, in [55.3.6.1](#) ~~55.3.7.1~~ for 10GBASE-T, in [113.3.7.1](#) for 25GBASE-T and 40GBASE-T, and in [82.3.1](#) for 40/100GBASE-R.

45.2.3.13.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

Change the text of the second paragraph of 45.2.3.13.4 (as modified by IEEE Std 802.3bq-2016) to reference 2.5GBASE-T and 5GBASE-T as follows:

For any member of the MultiGBASE-T set, when read as a one, bit 3.32.1 indicates that the 64B/65B receiver is detecting a BER of $\geq 10^{-4}$. When read as a zero, bit 3.32.1 indicates that the 64B/65B receiver is detecting a BER of $< 10^{-4}$. This bit is a direct reflection of the state of the hi_lfer variable in the MultiGBASE-T 64B/65B state diagrams, defined in [126.3.6.2.2](#) for 2.5GBASE-T and 5GBASE-T, in [55.3.6.1](#) for 10GBASE-T, and in [113.3.6.2.2](#) for 25GBASE-T and 40GBASE-T.

45.2.3.13.5 BASE-R and MultiGBASE-T block lock (3.32.0)

Change the text of 45.2.3.13.5 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bq-2016) to reference 2.5GBASE-T and 5GBASE-T as follows:

When read as a one, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for a member of the MultiGBASE-T set has block lock. When read as a zero, bit 3.32.0 indicates that the 64B/66B receiver for BASE-R or the 64B/65B receiver for a member of the MultiGBASE-T set has not achieved block lock. This bit is a direct reflection of the state of the block_lock variable in the 64B/66B state diagram and is defined in 49.2.13.2.2 for 10/25GBASE-R and in 82.2.19.2.2 for 40/100GBASE-R. For both the 2.5GBASE-T and 5GBASE-T PCS, the block_lock variable in the 64B/65B state diagram is defined in 126.3.6.2.2. For the 10GBASE-T PCS the block_lock variable in the 64B/65B state diagram is defined in 55.3.2.3. For both the 25GBASE-T and 40GBASE-T PCS the block_lock variable in the 64B/65B state diagram is defined in 113.3.6.2.2. For a multi-lane PCS, this bit indicates that the receiver has both block lock and alignment for all lanes and is identical to 3.50.12 (see 45.2.3.25.1).

45.2.3.14 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

45.2.3.14.3 BER (3.33.13:8)

Change the text of 45.2.3.14.3 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T as follows:

The BER counter is a six bit count as defined by the ber_count variable in 49.2.14.2 and 82.2.19.2.4 for 10/25/40/100GBASE-R and defined by the lfer_count counter in 126.3.6.2 in 2.5GBASE-T and 5GBASE-T, 55.3.6.2 for 10GBASE-T, and in 113.3.6.2.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the BASE-R and MultiGBASE-T PCS status 2 register is read by the management function or upon execution of the PCS reset. If the BER high order counter, 3.44 (see 45.2.3.23) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.3.14.4 Errored blocks (3.33.7:0)

Change the text of 45.2.3.14.4 (as modified by IEEE Std 802.3by-2016 and IEEE Std 802.3bq-2016) to include 2.5GBASE-T and 5GBASE-T as follows:

The errored blocks counter is an eight bit count defined by the errored_block_count counter specified in 49.2.14.2 for 10/25GBASE-R, in 82.3.1 for 40/100GBASE-R and defined by counter errored_block_count in 126.3.6.2 in 2.5GBASE-T and 5GBASE-T, 55.3.6.2 for 10GBASE-T and in 113.3.6.2 for 25GBASE-T and 40GBASE-T. These bits shall be reset to all zeros when the errored blocks count is read by the management function or upon execution of the PCS reset. If the Errored blocks high order counter, 3.45 (see 45.2.3.24) is not implemented then these bits shall be held at all ones in the case of overflow.

45.2.7 Auto-Negotiation registers

Change the names of registers 7.60 and 7.61 (EEE advertisement 1 and EEE LP ability 1), and the reserved row (7.62:63) in Table 45–200 (as modified by IEEE Std 802.3bq-2016, IEEE Std 802.3bw-2015, and IEEE Std 802.3bp-2016) to add EEE advertisement 2 register 7.62, and insert row for register 7.63, EEE LP ability 2, after 7.62 as follows (unchanged rows not shown):

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.60	EEE advertisement <u>1</u>	45.2.7.13
7.61	EEE LP link partner ability <u>1</u>	45.2.7.14
7.62:63	Reserved EEE advertisement <u>2</u>	<u>45.2.7.14aa</u>
7.63	EEE LP link partner ability <u>2</u>	45.2.7.14ab

45.2.7.10 MultiGBASE-T AN control 1 register (Register 7.32)

Change the reserved row in Table 45–207 (as modified by IEEE Std 802.3bq-2016) and insert rows for bits 7.32.8, 7.32.7, 7.32.6, and 7.32.5 above the reserved row as follows (unchanged rows not shown):

Table 45–207—MultiGBASE-T AN control 1 register

Bit(s)	Name	Description	R/W ^a
<u>7.32.8</u>	<u>5GBASE-T ability</u>	<u>1 = Advertise PHY as 5GBASE-T capable</u> <u>0 = Do not advertise PHY as 5GBASE-T capable</u>	<u>R/W</u>
<u>7.32.7</u>	<u>2.5GBASE-T ability</u>	<u>1 = Advertise PHY as 2.5GBASE-T capable</u> <u>0 = Do not advertise PHY as 2.5GBASE-T capable</u>	<u>R/W</u>
<u>7.32.6</u>	<u>5GBASE-T Fast retrain ability</u>	<u>1 = Advertise PHY as 5GBASE-T fast retrain capable</u> <u>0 = Do not advertise PHY as 5GBASE-T fast retrain capable</u>	<u>R/W</u>
<u>7.32.5</u>	<u>2.5GBASE-T Fast retrain ability</u>	<u>1 = Advertise PHY as 2.5GBASE-T fast retrain capable</u> <u>0 = Do not advertise PHY as 2.5GBASE-T fast retrain capable</u>	<u>R/W</u>
7.32.8:4	Reserved	Value always 0	RO

^aR/W = Read/Write, RO = Read only

Insert 45.2.7.10.4ca through 45.2.7.10.4cd after 45.2.7.10.4c (as inserted by IEEE Std 802.3bq-2016) as follows:

45.2.7.10.4ca 5GBASE-T capability (7.32.8)

Bit 7.32.8 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 5GBASE-T PHY. If bit 7.32.8 is set to one the PHY shall advertise 5GBASE-T PHY capability. If bit 7.32.8 is set to zero the PHY shall not advertise 5GBASE-T PHY capability.

45.2.7.10.4cb 2.5GBASE-T capability (7.32.7)

Bit 7.32.7 is used to select whether or not Auto-Negotiation advertises the ability to operate as a 2.5GBASE-T PHY. If bit 7.32.7 is set to one the PHY shall advertise 2.5GBASE-T PHY capability. If bit 7.32.7 is set to zero the PHY shall not advertise 2.5GBASE-T PHY capability.

45.2.7.10.4cc 5GBASE-T Fast retrain ability (7.32.6)

Bit 7.32.6 is used to select whether or not the 5GBASE-T PHY advertises the ability to support 5GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 126.4.2.5.10. If bit 7.32.6 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.6 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.10.4cd 2.5GBASE-T Fast retrain ability (7.32.5)

Bit 7.32.5 is used to select whether or not the 2.5GBASE-T PHY advertises the ability to support 2.5GBASE-T fast retrain. Fast retrain ability is exchanged during link training, see 126.4.2.5.10. If bit 7.32.5 is set to one, the PHY shall advertise fast retrain ability. If bit 7.32.5 is set to zero, the PHY shall not advertise fast retrain ability.

45.2.7.11 MultiGBASE-T AN status 1 register (Register 7.33)

Change the reserved row in Table 45–208 (as modified by IEEE Std 802.3bq-2016) and insert three new rows below it as follows (unchanged rows not shown):

Table 45–208—MultiGBASE-T AN status 1 register

Bit(s)	Name	Description	R/W ^a
7.33.6:3	Reserved <u>Link partner 5GBASE-T capability</u>	Value always 0 <u>1 = Link partner is able to operate as 5GBASE-T</u> <u>0 = Link partner is not able to operate as 5GBASE-T</u>	RO
<u>7.33.5</u>	<u>Link partner 2.5GBASE-T capability</u>	<u>1 = Link partner is able to operate as 2.5GBASE-T</u> <u>0 = Link partner is not able to operate as 2.5GBASE-T</u>	<u>RO</u>
<u>7.33.4</u>	<u>5GBASE-T Fast retrain ability</u>	<u>1 = Link partner is capable of 5GBASE-T fast retrain</u> <u>0 = Link partner is not capable of 5GBASE-T fast retrain</u>	<u>RO</u>
<u>7.33.3</u>	<u>2.5GBASE-T Fast retrain ability</u>	<u>1 = Link partner is capable of 2.5GBASE-T fast retrain</u> <u>0 = Link partner is not capable of 2.5GBASE-T fast retrain</u>	<u>RO</u>

^aRO = Read only, SC = Self-clearing, LH = Latching high

45.2.7.11.1 MASTER-SLAVE configuration fault (7.33.15)

Change the text of 45.2.7.11.1 to include 2.5GBASE-T and 5GBASE-T as follows:

MASTER-SLAVE configuration fault bit 7.33.15 shall be set in the event that determination of the MASTER-SLAVE cannot be successfully concluded. MASTER-SLAVE configuration fault, as well as the criteria and method of fault detection, is PHY specific. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 10GBASE-T is contained in 55.6.2. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 25GBASE-T and 40GBASE-T is contained in 113.6.2. Additional information regarding the resolution and selection of MASTER-SLAVE and bit 7.33.15 for 2.5GBASE-T and 5GBASE-T is contained in 126.6.2. The MASTER-SLAVE configuration fault bit 7.33.15 shall be cleared each time the MultiGBASE-T status register 7.33 is read via the management interface and shall be cleared by a PMA reset of a PHY in the MultiGBASE-T set. Bit 7.33.15 shall self clear upon Auto-Negotiation enable.

45.2.7.11.2 MASTER-SLAVE configuration resolution (7.33.14)

Change the text of 45.2.7.11.2 to include 2.5GBASE-T and 5GBASE-T as follows:

Bit 7.33.14 is determined by the ~~10GBASE-T~~ MASTER-SLAVE configuration resolution function, ~~described in 55.6.2 or the 25GBASE-T/40GBASE-T MASTER-SLAVE configuration resolution function described in 113.6.2.~~ These are described in 126.6.2, 55.6.2, and 113.6.2, for 2.5G/5GBASE-T, 10GBASE-T, and 25G/40GBASE-T, respectively. If the MASTER-SLAVE configuration resolution bit 7.33.14 is set to one and the Auto-Negotiation complete bit 7.1.5 is set and MASTER-SLAVE configuration fault bit 7.33.15 in the MultiGBASE-T status register is zero, then MASTER mode of operation has been selected. If the MASTER-SLAVE configuration resolution bit 7.33.14 is set to zero and the Auto-Negotiation complete bit 7.1.5 is set and MASTER-SLAVE configuration fault bit 7.33.15 in the MultiGBASE-T status register is zero, then SLAVE mode of operation has been selected. In all other cases, neither SLAVE mode nor MASTER mode has been selected.

Insert the following new subclauses (45.2.7.11.7ba, 45.2.7.11.7bb, 45.2.7.11.7bc, and 45.2.7.11.7bd) after 45.2.7.11.7b, inserted by IEEE Std 802.3bq-2016:

45.2.7.11.7ba Link partner 5GBASE-T capability (7.33.6)

Bit 7.33.6 is only valid when page received bit 7.1.6 is set to one. When read as a one, bit 7.33.6 indicates that the link partner is able to operate as 5GBASE-T. When read as a zero, bit 7.33.6 indicates that the link partner is not able to operate as 5GBASE-T.

45.2.7.11.7bb Link partner 2.5GBASE-T capability (7.33.5)

Bit 7.33.5 is only valid when page received bit 7.1.5 is set to one. When read as a one, bit 7.33.5 indicates that the link partner is able to operate as 2.5GBASE-T. When read as a zero, bit 7.33.5 indicates that the link partner is not able to operate as 2.5GBASE-T.

45.2.7.11.7bc 5GBASE-T Fast retrain ability (7.33.4)

When read as a one, bit 7.33.4 indicates that the link partner has the ability to support the 5GBASE-T fast retrain capability as specified in 126.4.2.5.16. When read as a zero, bit 7.33.4 indicates that the PHY lacks the ability to support the 5GBASE-T fast retrain capability. This bit is only valid after link is established.

45.2.7.11.7bd 2.5GBASE-T Fast retrain ability (7.33.3)

When read as a one, bit 7.33.3 indicates that the link partner has the ability to support the 2.5GBASE-T fast retrain capability as specified in 126.4.2.5.16. When read as a zero, bit 7.33.3 indicates that the PHY lacks the ability to support the 2.5GBASE-T fast retrain capability. This bit is only valid after link is established.

Change the title of 45.2.7.13 and the text of the first paragraph of 45.2.7.13 (as modified by IEEE Std 802.3bq-2016) to rename the register EEE advertisement 1 as follows (unchanged paragraphs not shown):

45.2.7.13 EEE advertisement 1 (Register 7.60)

This register defines the EEE advertisement for several device types. Devices that use Clause 28 Auto-Negotiation send EEE advertisement in the Unformatted Next Page following a EEE technology message code as defined in 28C.12 as part of the 10GBASE-T and 1000BASE-T technology message code as defined in 28C.11. Devices that use Clause 73 Auto-Negotiation send EEE advertisement in the unformatted code field of Message Next Page with EEE technology message code as defined in 73A.4. For 25GBASE-T and 40GBASE-T, the EEE advertisement is exchanged in the Infobfield during training as defined in 113.4.2.5.10.

For 2.5GBASE-T and 5GBASE-T, the EEE advertisement is exchanged in the Infocfield during training as defined in 126.4.2.5.10. The assignment of bits in the EEE advertisement 1 register and the correspondence with the bits in the Next Page messages or in the training Infocfield are shown in Table 45–210.

Change the title of Table 45–210 as follows:

Table 45–210—EEE advertisement 1 register (Register 7.60) bit definitions

Change the title and text of 45.2.7.14 (as modified by IEEE Std 802.3bq-2016) to change the name of register 7.61 as follows:

45.2.7.14 EEE link partner ability 1 (Register 7.61)

All of the bits in the EEE LP ability 1 register are read-only. A write to the EEE LP ability 1 register shall have no effect. Except for 10GBASE-T, members of the MultiGBASE-T PHY set exchange the EEE ability in the Infocfield during link training. For these PHYs, the EEE LP ability register is updated after link is established. For all other PHYs, when the AN process has been completed, this register shall reflect the contents of the link partner's EEE advertisement 1 register. The assignment of bits in the EEE link partner ability 1 register and the correspondence with the bits in the Next Page messages are shown in Table 45–211.

Change the title of Table 45–211 as follows (unchanged rows not shown):

Table 45–211—EEE link partner ability 1 (Register 7.61) bit definitions

Change the second paragraph of 45.2.7.14 as follows:

The definitions for the contents of the EEE LP ability register are given by the definitions for the contents on the link partner's EEE advertisement 1 register, 7.60 (see 45.2.7.13).

Insert a new subclause (45.2.7.14aa including Table 45–211aa) after 45.2.7.14 and before 45.2.7.14a (inserted by IEEE Std 802.3bz-2016) as follows:

45.2.7.14aa EEE advertisement 2 (Register 7.62)

EEE advertisement 2 register is a continuation of EEE advertisement 1 register. The assignment of bits in the EEE advertisement 2 register are shown in Table 45–211aa.

Table 45–211aa—EEE advertisement 2 register (Register 7.62) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W ^a
7.62.15:2	Reserved	Value always 0		RO
7.62.1	5GBASE-T EEE	1 = Advertise that the 5GBASE-T has EEE capability 0 = Do not advertise that the 5GBASE-T has EEE capability	126.4.2.5.10	R/W
7.62.0	2.5GBASE-T EEE	1 = Advertise that the 2.5GBASE-T has EEE capability 0 = Do not advertise that the 2.5GBASE-T has EEE capability	126.4.2.5.10	R/W

^aR/W = Read/Write, RO = Read only

45.2.7.14aa.1 5GBASE-T EEE (7.62.1)

If the device supports EEE operation for 5GBASE-T as defined in 126.6.1, and EEE operation is desired, bit 7.62.1 shall be set to one.

45.2.7.14aa.2 2.5GBASE-T EEE (7.62.0)

If the device supports EEE operation for 2.5GBASE-T as defined in 126.6.1, and EEE operation is desired, bit 7.62.0 shall be set to one.

Insert new subclause (45.2.7.14ab including Table 45–211ab) as follows:

45.2.7.14ab EEE link partner ability 2 (Register 7.63)

All of the bits in the EEE LP ability 2 register are read-only. A write to the EEE LP ability 2 register shall have no effect. When the AN and training processes have been completed, this register shall reflect the contents of the link partner's EEE advertisement 2 register. The assignment of bits in the EEE link partner ability 2 register and the correspondence with the bits in the Next Page messages (for PHYs that exchange EEE abilities during AutoNegotiation) are shown in Table 45–211ab.

The definitions for the contents of the EEE LP ability 2 register are given by the definitions for the contents on the link partner's EEE advertisement 2 register, 7.62 (see 45.2.7.14aa).

Table 45–211ab—EEE link partner ability 2 (Register 7.63) bit definitions

Bit(s)	Name	Description	Clause reference; Next Page bit number	R/W ^a
7.63.15:2	Reserved	Value always 0		RO
7.63.1	5GBASE-T EEE	1 = Link partner is advertising that the 5GBASE-T has EEE capability 0 = Link partner is not advertising that the 5GBASE-T has EEE capability	126.4.2.5.10	RO
7.63.0	2.5GBASE-T EEE	1 = Link partner is advertising that the 2.5GBASE-T has EEE capability 0 = Link partner is not advertising that the 2.5GBASE-T has EEE capability	126.4.2.5.10	RO

^aRO = Read only

45.2.7.14a MultiGBASE-T AN control 2 (Register 7.64)

Change the reserved row and insert two new rows in Table 45-211a, inserted by IEEE Std 802.3bq-2016, as follows (unchanged rows not shown):

Table 45–211a—MultiGBASE-T AN control 2 (Register 7.64) bit definitions

Bit(s)	Name	Description	R/W ^a
7.64.15:24	Reserved	Value always 0	RO
<u>7.64.3</u>	<u>2.5GBASE-T THP Bypass Request</u>	<u>1 = Local device requests link partner to initially reset THP during fast retrain</u> <u>0 = Local device requests link partner not to initially reset THP during fast retrain</u>	<u>R/W</u>
<u>7.64.2</u>	<u>5GBASE-T THP Bypass Request</u>	<u>1 = Local device requests link partner to initially reset THP during fast retrain</u> <u>0 = Local device requests link partner not to initially reset THP during fast retrain</u>	<u>R/W</u>

^aR/W = Read/Write, RO = Read only

Insert 45.2.7.14a.a and 45.2.7.14a.b after 45.2.7.14a and before 45.2.7.14a.1 (both inserted by IEEE Std 802.3bq-2016) as follows:

45.2.7.14a.a 2.5GBASE-T THP Bypass Request

Bit 7.64.3 is valid only if 7.32.5 is set to one advertising fast retrain ability, and is used to request the link partner whether to initially reset the THP during fast retrain. THP Bypass Request is exchanged during link training, see 126.4.2.5.10. If bit 7.64.3 is set to zero the local device requests link partner not to reset THP during fast retrain. If bit 7.64.3 is set to one the local device requests link partner to initially reset THP during fast retrain.