INTERNATIONAL STANDARD

ISO/ IEC/IEEE 8802-3

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AMENDMENT 3
2021-12

Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

Part 3: Standard for Ethernet

AMENDMENT 3: Media access control parameters for 50 Gb/s and physical layers and management parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s operation

Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —

Partie 3: Norme pour Ethernet

AMENDEMENT 3: Paramètres de commande d'accès media pour 50 Gb/s et couches physiques et paramètres de gestion pour fonctionnement à 50 Gb/s, 100 Gb/s et 200 Gb/s

Reference number
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IEEE Std 802.3cd™-2018
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018
and IEEE Std 802.3bt™-2018)

IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

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Approved 5 December 2018

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Abstract: Clause 131 through Clause 140 and Annex 135A through Annex 136D are added to IEEE Std 802.3-2018 by this amendment to specify IEEE 802.3 Media Access Control (MAC) parameters, Physical Layer specifications, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

Keywords: 50GAUI-1, 50GAUI-2, 50GBASE-CR, 50GBASE-FR, 50GBASE-KR, 50GBASE-LR, 50GBASE-SR, 50 Gigabit Ethernet, 50GMII, 100GAUI-2, 100GAUI-4, 100GBASE-CR2, 100GBASE-DR, 100GBASE-KR2, 100GBASE-SR2, 100 Gigabit Ethernet, 200GBASE-CR4, 200GBASE-KR4, 200GBASE-SR4, 200 Gigabit Ethernet, amendment, EEE, Energy-Efficient Ethernet, Ethernet, FEC, forward error correction, IEEE 802.3™, IEEE 802.3cd™, LAUI-2, MMF, SMF

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Introduction

This introduction is not part of IEEE Std 802.3cd-2018, IEEE Standard for Ethernet. Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3cd-2018, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber

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access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, Annex 128C, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

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A companion document, IEEE Std 802.3.1, describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018 and IEEE Std 802.3bt™-2018.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

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1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Insert the following new compatibility interfaces into 1.1.3.2 after m) "40 Gb/s Parallel Physical Interface (XLPPI)":

m1) *50 Gb/s Media Independent Interface (50GMII)*. The 50GMII is designed to connect a 50 Gb/s capable MAC to a 50 Gb/s PHY. While conformance with implementation of this interface is not necessary to ensure communication, it allows flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The 50GMII is a logical interconnection intended for use as an intra-chip interface. No mechanical connector is specified for use with the 50GMII. The 50GMII is optional.

m2) *50 Gb/s Attachment Unit Interface (LAUI-2/50GAUI-n)*. The LAUI-2/50GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 50 Gb/s speeds. The LAUI-2/50GAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Two widths of 50GAUI-n are defined: a two-lane version (50GAUI-2) in Annex 135D and Annex 135E, and a one-lane version (50GAUI-1) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the LAUI-2/50GAUI-n. The LAUI-2/50GAUI-n is optional.

Change the compatibility interface o) "100 Gb/s Attachment Unit Interface (CAUI-n)" in 1.1.3.2 as follows:

o) *100 Gb/s Attachment Unit Interface (CAUI-n/100GAUI-n)*. The CAUI-n/100GAUI-n is a physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs. While conformance with implementation of this interface is not necessary to ensure communication, it is recommended, since it allows maximum flexibility in intermixing PHYs and DTEs at 100 Gb/s speeds. The CAUI-n is intended for use as a chip-to-chip or a chip-to-module interface. Three~~Two~~ widths of CAUI-n are defined: a ten-lane version (CAUI-10) in Annex 83A and Annex 83B, ~~and~~ a four-lane version (CAUI-4/100GAUI-4) in Annex 83D, ~~and~~ Annex 83E, Annex 135D, and Annex 135E, and a two-lane version (100GAUI-2) in Annex 135F and Annex 135G. No mechanical connector is specified for use with the CAUI-n/100GAUI-n. The CAUI-n/100GAUI-n is optional.

1.3 Normative references

Change the following reference in 1.3 as shown:

IEC 61753-022-2:2012, Fibre optic interconnecting devices and passive components—Performance standard—Part 022-2: Fibre optic connectors terminated on multimode fibre for category C—Controlled environment~~, performance Class M~~.

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1.4 Definitions

Insert the following new definition after 1.4.25 "100GBASE-CR10":

1.4.25a 100GBASE-CR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

Insert the following new definition after 1.4.26 "100GBASE-CR4":

1.4.26a 100GBASE-DR: IEEE 802.3 Physical Layer specification for 100 Gb/s serial transmission using 100GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 500 m. (See IEEE Std 802.3, Clause 140.)

Insert the following new definition after 1.4.28 "100GBASE-KP4":

1.4.28a 100GBASE-KR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.34 "100GBASE-SR10":

1.4.34a 100GBASE-SR2: IEEE 802.3 Physical Layer specification for 100 Gb/s using 100GBASE-R encoding over two lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Change 1.4.36 as follows:

1.4.36 100 Gb/s Attachment Unit Interface (CAUI-n, 100GAUI-n): A physical instantiation of the PMA service interface to extend the connection between 100 Gb/s capable PMAs over n lanes, used for chip-to-chip or chip-to-module interconnections. Three~~Two~~ widths~~ of CAUI-n~~ are defined: a ten-lane version (CAUI-10), ~~and a~~two four-lane versions (CAUI-4, 100GAUI-4), and a two-lane version (100GAUI-2). (See IEEE Std 802.3, Annex 83A and Annex 83B for CAUI-10, ~~or~~ Annex 83D and Annex 83E for CAUI-4, Clause 135, Annex 135D, and Annex 135E for 100GAUI-4, or Clause 135, Annex 135F, and Annex 135G for 100GAUI-2.)

Insert the following new definition after 1.4.82c "2.5GSEI" as inserted by IEEE Std 802.3cb-2018:

1.4.82d 200GBASE-CR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136)

Insert the following new definition after 1.4.84 "200GBASE-FR4":

1.4.84a 200GBASE-KR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

Insert the following new definition after 1.4.86 "200GBASE-R":

1.4.86a 200GBASE-SR4: IEEE 802.3 Physical Layer specification for 200 Gb/s using 200GBASE-R encoding over four lanes of multimode fiber. (See IEEE Std 802.3, Clause 138.)

Insert the following new definitions before 1.4.128a "5GBASE-KR" as inserted by IEEE Std 802.3cb-2018:

1.4.128aa 50GBASE-CR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of shielded balanced copper cabling. (See IEEE Std 802.3, Clause 136.)

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1.4.128ab 50GBASE-FR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 2 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ac 50GBASE-KR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over one lane of an electrical backplane. (See IEEE Std 802.3, Clause 137.)

1.4.128ad 50GBASE-LR: IEEE 802.3 Physical Layer specification for 50 Gb/s serial transmission using 50GBASE-R encoding and 4-level pulse amplitude modulation over one wavelength on single-mode fiber, with reach up to at least 10 km. (See IEEE Std 802.3, Clause 139.)

1.4.128ae 50GBASE-R: An IEEE 802.3 physical coding sublayer for one-lane 50 Gb/s operation. (See IEEE Std 802.3, Clause 131.)

1.4.128af 50GBASE-SR: IEEE 802.3 Physical Layer specification for 50 Gb/s using 50GBASE-R encoding over multimode fiber. (See IEEE Std 802.3, Clause 138.)

1.4.128ag 50 Gb/s Attachment Unit Interface (50GAUI-n, LAUI-2): A physical instantiation of the PMA service interface to extend the connection between 50 Gb/s capable PMAs over one lane (50GAUI-1) or two lanes (50GAUI-2, LAUI-2), used for chip-to-chip or chip-to-module interconnections. (See IEEE Std 802.3, Clause 135 and Annex 135B through Annex 135G.)

1.4.128ah 50 Gb/s Media Independent Interface (50GMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 50 Gb/s operation. (See IEEE Std 802.3, Clause 132.)

Insert the following new definition after 1.4.255 "fast wake":

1.4.255a FEC lane (FECL): In 50GBASE-R and 100GBASE-R, the FEC distributes encoded data to multiple logical lanes; these logical lanes are called FEC lanes. One or more FEC lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 135.)

Change 1.4.386 as follows:

1.4.386 PCS lane (PCSL): In 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R, the PCS distributes encoded data to multiple logical lanes; these logical lanes are called PCS lanes. One or more PCS lanes can be multiplexed and carried on a physical lane together at the PMA service interface. (See IEEE Std 802.3, Clause 83, and Clause 120, and Clause 135.)

1.5 Abbreviations

Insert the following new abbreviations into 1.5 in alphanumeric order:

100GAUI	100 Gb/s Attachment Unit Interface
50GAUI	50 Gb/s Attachment Unit Interface
50GMII	50 Gb/s Media Independent Interface
ERL	effective return loss
FECL	FEC Lane
LAUI	50 Gb/s Attachment Unit Interface

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4. Media Access Control

4.4 Specific implementations

4.4.2 MAC parameters

Change Table 4–2 as follows:

Table 4–2—MAC parameters

Parameters	MAC data rate			
	Up to and including 100 Mb/s	**1 Gb/s**	**2.5 Gb/s, 5 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s**	**10 Gb/s**
slotTime	512 bit times	4096 bit times	not applicable	not applicable
interPacketGap[a]	96 bits	96 bits	96 bits	96 bits
attemptLimit	16	16	not applicable	not applicable
backoffLimit	10	10	not applicable	not applicable
jamSize	32 bits	32 bits	not applicable	not applicable
maxBasicFrameSize	1518 octets	1518 octets	1518 octets	1518 octets
maxEnvelopeFrameSize	2000 octets	2000 octets	2000 octets	2000 octets
minFrameSize	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)	512 bits (64 octets)
burstLimit	not applicable	65 536 bits	not applicable	not applicable
ipgStretchRatio	not applicable	not applicable	not applicable	104 bits

[a]References to interFrameGap or interFrameSpacing in other clauses (e.g., 13, 35, and 42) shall be interpreted as interPacketGap.

Change Note 7 in 4.4.2 as follows:

NOTE 7—For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s operation, the received interpacket gap (the spacing between two packets, from the last bit of the FCS field of the first packet to the first bit of the Preamble of the second packet) can have a minimum value of 8 BT (bit times), as measured at the XLGMII, 50GMII, CGMII, 200GMII, or 400GMII receive signals at the DTE due to clock tolerance and lane alignment requirements.

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30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.3.2.1.2 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.3.2.1.3 after the entry for 40GBASE-T:

APPROPRIATE SYNTAX:

50GBASE-R	Clause 133 50 Gb/s multi-PCS lane 64B/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph of "BEHAVIOUR DEFINED AS" in 30.3.2.1.5 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:

For operation at 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate "Receive Error" on the media independent interface (see Table 46–4 and Table 81–4).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

APPROPRIATE SYNTAX:

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 40GBASE-T:

50GBASE-R	Multi-lane PCS as specified in Clause 133 with PMA as specified in Clause 135 over undefined PMD

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50GBASE-CR	50GBASE-R PCS/PMA over shielded copper balanced cable PMD as specified in Clause 136
50GBASE-KR	50GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
50GBASE-SR	50GBASE-R PCS/PMA over multimode fiber PMD as specified in Clause 138
50GBASE-FR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139
50GBASE-LR	50GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 139

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 100GBASE-ER4:

100GBASE-CR2	100GBASE-R PCS/PMA over 2 lane shielded copper balanced cable PMD as specified in Clause 136
100GBASE-KR2	100GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
100GBASE-SR2	100GBASE-R PCS/PMA over 2 lane multimode fiber PMD as specified in Clause 138
100GBASE-DR	100GBASE-R PCS/PMA over single mode fiber PMD as specified in Clause 140

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 200GBASE-LR4:

200GBASE-CR4	200GBASE-R PCS/PMA over 4 lane shielded copper balanced cable PMD as specified in Clause 136
200GBASE-KR4	200GBASE-R PCS/PMA over an electrical backplane PMD as specified in Clause 137
200GBASE-SR4	200GBASE-R PCS/PMA over 4 lane multimode fiber PMD as specified in Clause 138

Change the last paragraph of "BEHAVIOUR DEFINED AS" in 30.5.1.1.2 (as modified by IEEE Std 802.3cb-2018) as follows:

BEHAVIOUR DEFINED AS:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 2.5GBASE-X, 5GBASE-R, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 50GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.5.1.1.4 aMediaAvailable

Change the sixth paragraph of "BEHAVIOUR DEFINED AS" in 30.5.1.1.4 as follows:

BEHAVIOUR DEFINED AS:

For 40 Gb/s, 50 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, the enumerations map to value of the link_fault variable (see 81.3.4) within the Link Fault Signaling state diagram (see 81.3.4.1 and Figure 46–11) as follows: the values OK and Link Interruption map to the enumeration "available", the value Local Fault maps to the enumeration "not available" and the value Remote Fault maps to the enumeration "remote fault".

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30.5.1.1.11 aBIPErrorCount

Change the text of "APPROPRIATE SYNTAX" and the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.11 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 10 000 counts per second for 40 Gb/s and 50 Gb/s implementations and 5 000 counts per second for 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 40/50/100GBASE-R PHYs and 100GBASE-P PHYS, an array of BIP error counters.

30.5.1.1.12 aLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.12 as follows:

BEHAVIOUR DEFINED AS:

For 40/50/100/200/400GBASE-R PHYs and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.17 aFECCorrectedBlocks

Change the text of "APPROPRIATE SYNTAX" in 30.5.1.1.17 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.17 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of corrected FEC block counters.

30.5.1.1.18 aFECUncorrectableBlocks

Change the text of "APPROPRIATE SYNTAX" in 30.5.1.1.18 as follows:

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresettable counters. Each counter has a maximum increment rate of 1 200 000 counts per second for 1000 Mb/s implementations, 5 000 000 counts per second for 10 Gb/s, 25 Gb/s, and 40 Gb/s implementations, 10 000 000 counts per second for 50 Gb/s implementations, 2 500 000 counts per second for 100 Gb/s implementations, 40 000 000 counts per second for 200 Gb/s implementations, and 80 000 000 counts per second for 400 Gb/s implementations.

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Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.18 as follows:

BEHAVIOUR DEFINED AS:

For 1000BASE-PX, 10/25/40/50/100/200/400GBASE-R, 100GBASE-P, 10GBASE-PR, or 10/1GBASE-PRX PHYs, an array of uncorrectable FEC block counters.

30.5.1.1.26 aRSFECBIPErrorCount

Change the text of "APPROPRIATE SYNTAX" and the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.26 as follows:

ATTRIBUTE

APPROPRIATE SYNTAX:

A SEQUENCE of generalized nonresetable counters. Each counter has a maximum increment rate of 5 000 counts per second for 50 Gb/s and 100 Gb/s implementations.

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of BIP error counters.

30.5.1.1.27 aRSFECLaneMapping

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.27 as follows:

BEHAVIOUR DEFINED AS:

For 50GBASE-R, 100GBASE-R, and 100GBASE-P PHYs, an array of PCS lane identifiers.

30.5.1.1.29 aRSFECBypassIndicationAbility

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.29 as follows:

BEHAVIOUR DEFINED AS:

A read-only value that indicates if the PHY supports an optional RS-FEC error indication bypass ability ~~(see 91.5.3.3)~~.

30.5.1.1.31 aRSFECBypassIndicationEnable

Change the first sentence of "BEHAVIOUR DEFINED AS" in 30.5.1.1.31 as follows:

BEHAVIOUR DEFINED AS:

A read-write value that indicates the mode of operation of the RS-FEC error indication bypass function ~~(see 91.5.3.3)~~.

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30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

APPROPRIATE SYNTAX:

Insert the following new entry into "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 40GBASE-T:

50GR	50GBASE-CR as specified in Clause 136 or 50GBASE-KR as specified in Clause 137

Insert the following new entries into "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 100GBASE-KP4:

100GR2	100GBASE-CR2 as specified in Clause 136 or 100GBASE-KR2 as specified in Clause 137
200GR4	200GBASE-CR4 as specified in Clause 136 or 200GBASE-KR4 as specified in Clause 137

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change Table 45–3 as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.20	~~Reserved~~ 50G PMA/PMD extended ability	45.2.1.17a
…		
1.25~~, 1.26~~	~~Reserved~~ PMA/PMD extended ability 2	45.2.1.21a
1.26	Reserved	
…		
1.500 through 1.515	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, receive direction, lane 0 through lane 15	45.2.1.129, 45.2.1.130
1.516 through 1.531	50GAUI-n, 100GAUI-2, 200GAUI-n, and 400GAUI-n chip-to-chip transmitter equalization, transmit direction, lane 0 through lane 15	45.2.1.131, 45.2.1.132
~~1.532 through 1.699~~ 1.532 through 1.599	Reserved	
1.600	PMA precoder control Tx output	45.2.1.132a
1.601	PMA precoder control Rx input	45.2.1.132b
1.602	PMA precoder control Rx output	45.2.1.132c
1.603	PMA precoder control Tx input	45.2.1.132d
1.604	PMA precoder request flag	45.2.1.132e
1.605	PMA precoder request Rx input status	45.2.1.132f
1.606	PMA precoder request Tx input status	45.2.1.132g
1.607 through 1.649	Reserved	
1.650, 1.651	RS-FEC degraded SER activate threshold	45.2.1.132h
1.652, 1.653	RS-FEC degraded SER deactivate threshold	45.2.1.132i
1.654, 1.655	RS-FEC degraded SER interval	45.2.1.132j
1.656 through 1.699	Reserved	
…		

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Table 45–3—PMA/PMD registers *(continued)*

Register address	Register name	Subclause
~~1.1110 through 1.1199~~ 1.1110 through 1.1119	Reserved	
1.1120 through 1.1123	BASE-R PAM4 PMD training LP control, lane 0 through lane 3	45.2.1.135a
1.1124 through 1.1199	Reserved	
…		
~~1.1210 through 1.1299~~ 1.1210 through 1.1219	Reserved	
1.1220 through 1.1223	BASE-R PAM4 PMD training LP status, lane 0 through lane 3	45.2.1.136a
1.1224 through 1.1299	Reserved	
…		
~~1.1310 through 1.1399~~ 1.1310 through 1.1319	Reserved	
1.1320 through 1.1323	BASE-R PAM4 PMD training LD control, lane 0 through lane 3	45.2.1.137a
1.1324 through 1.1399	Reserved	
…		
~~1.1410 through 1.1449~~ 1.1410 through 1.1419	Reserved	
1.1420 through 1.1423	BASE-R PAM4 PMD training LD status, lane 0 through lane 3	45.2.1.138a
1.1424 through 1.1449	Reserved	
…		

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45.2.1.1 PMA/PMD control 1 register (Register 1.0)

Change the bits 1.0.5:2 row in Table 45–4 as follows (unchanged rows not shown):

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.0.5:2	Speed selection	5 4 3 2 1 1 x x = Reserved 1 0 1 x = Reserved 1 0 0 1 = 400 Gb/s 1 0 0 0 = 200 Gb/s 0 1 1 1 = 5 Gb/s 0 1 1 0 = 2.5 Gb/s 0 1 0 1 = ~~Reserved~~ 50 Gb/s 0 1 0 0 = 25 Gb/s 0 0 1 1 = 100 Gb/s 0 0 1 0 = 40 Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10 Gb/s	R/W
…			

[a]R/W = Read/Write, SC = Self-clearing, RO = Read only

45.2.1.1.3 Speed selection (1.0.13, 1.0.6, 1.0.5:2)

Change the last paragraph of 45.2.1.1.3 as follows:

When bits 5 through 2 are set to 0010 the use of a 40G PMA/PMD is selected; when set to 0011 the use of a 100G PMA/PMD is selected; when set to 0100 the use of a 25G PMA/PMD is selected; when set to 0101 the use of a 50G PMA/PMD is selected; when set to 0110 the use of a 2.5G PMA/PMD is selected; when set to 0111 the use of a 5G PMA/PMD is selected; when set to 1000 the use of a 200G PMA/PMD is selected; when set to 1001 the use of a 400G PMA/PMD is selected. More specific selection is performed using the PMA/PMD control 2 register (Register 1.7) (see 45.2.1.6.3).

45.2.1.2 PMA/PMD status 1 register (Register 1.1)

45.2.1.2.3 Fault (1.1.7)

Change the fourth sentence of 45.2.1.2.3 as follows:

For 10/25/40/50/100/200/400 Gb/s operation, bit 1.1.7 is set to a one when either of the fault bits (1.8.11, 1.8.10) located in register 1.8 are set to a one.

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