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**Telecommunications and exchange
between information technology
systems — Requirements for local and
metropolitan area networks —**

**Part 3:
Standard for Ethernet**

**AMENDMENT 1: Physical layer
specifications and management
parameters for 2.5 Gb/s and 5 Gb/s
operation over backplane**

*Télécommunications et échange entre systèmes informatiques —
Exigences pour les réseaux locaux et métropolitains —*

Partie 3: Norme pour Ethernet

*AMENDEMENT 1: Spécifications de la couche physique et
paramètres de gestion pour fonctionnement à 2,5 Gb/s et 5 Gb/s sur
fond de panier*



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IEEE Standard for Ethernet

Amendment 1: Physical Layer Specifications and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation over Backplane

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of the
IEEE Computer Society

Approved 27 September 2018

IEEE-SA Standards Board

Abstract: Ethernet Media Access Control (MAC) parameters, Physical Layer specifications, and management objects for the serial transfer of Ethernet format frames at 2.5 Gb/s and 5 Gb/s over electrical backplanes are defined in this amendment to IEEE Std 802.3-2018.

Keywords: 2.5 Gigabit Ethernet, 5 Gigabit Ethernet, 2.5GBASE-KX, 2.5GBASE-X, 5GBASE-KR, 5GBASE-R, amendment, AN, Auto-Negotiation, Backplane Ethernet, BASE-R, BASE-X, EEE, Energy Efficient Ethernet, Ethernet, IEEE 802.3™, IEEE 802.3cb™

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Introduction

This introduction is not part of IEEE Std 802.3cb-2018, IEEE Standard for Ethernet—Amendment 1: Physical Layer Specifications and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation over Backplane.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of publication for IEEE Std 802.3cb-2018, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 1: Physical Layer Specifications and Management Parameters for 2.5 Gb/s and 5 Gb/s Operation over Backplane

[This amendment is based on IEEE Std 802.3™-2018.]

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in bold italic. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strike through~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.¹

¹ Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

1. Introduction

1.3 Normative references

Insert the following new reference (for SFF-8482 connector) in alphanumerical order:

SFF-8482, Specification for Serial Attachment 2X Unshielded Connector.²

1.4 Definitions

Insert the following new definition (for 2.5GBASE-KX) after 1.4.81 1G-EPON:

1.4.81a 2.5GBASE-KX: IEEE 802.3 Physical Layer specification for 2.5 Gb/s using 2.5GBASE-X encoding over an electrical backplane. (See IEEE Std 802.3, Clause 128.)

Insert the following new definitions (for 2.5GBASE-X, 2.5GP11, and 2.5GSEI) after 1.4.82 2.5GBASE-T:

1.4.82a 2.5GBASE-X: IEEE 802.3 physical coding and physical medium attachment for serial 2.5 Gb/s operation. (See IEEE Std 802.3, Clause 127.)

1.4.82b 2.5GP11: The 2.5 Gb/s PCS Internal Interface is a logical interface that is internal to the 2.5GBASE-X PCS and exists solely for the purposes of defining the 2.5GBASE-X PCS functionality. (See IEEE Std 802.3, 127.2.5.1.)

1.4.82c 2.5GSEI: The 2.5 Gb/s Interface from storage sub-system or bridge subsystem onto backplane (See IEEE Std 802.3, Annex 128A.)

Insert the following new definitions (for 5GBASE-KR and 5GBASE-R) after 1.4.128 4D-PAM5:

1.4.128a 5GBASE-KR: IEEE 802.3 Physical Layer specification for 5 Gb/s using 5GBASE-R encoding over an electrical backplane. (See IEEE Std 802.3, Clause 130.)

1.4.128b 5GBASE-R: An IEEE 802.3 physical coding sublayer and physical medium attachment sublayer for serial 5 Gb/s operation. (See IEEE Std 802.3, Clause 129.)

Insert the following new definition (for 5GSEI) after 1.4.129 5GBASE-T:

1.4.129a 5GSEI: The 5 Gb/s Interface from storage sub-system or bridge subsystem onto backplane (See IEEE Std 802.3, Annex 130A.)

Change 1.4.150 as shown:

1.4.150 BASE-R: An IEEE 802.3 family of Physical Layer devices using 64B/66B encoding defined in Clause 49, Clause 82, Clause 107, or Clause 119, or Clause 129 of IEEE Std 802.3. (~~See IEEE Std 802.3, Clause 49, Clause 82, Clause 107, Clause 119.~~)

²SFF documents are available from the Storage Networking Industry Association (www.snia.org/sff/specifications).

1.5 Abbreviations

Insert the following new abbreviations into 1.5 in alphanumeric order:

2.5GPII	2.5 Gb/s PCS Internal Interface
2.5GSEI	2.5 Gb/s Storage Enclosure Interface
5GSEI	5 Gb/s Storage Enclosure Interface

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.3.2.1.2 after the entry for 2.5GBASE-T:

2.5GBASE-X Clause 127 2.5 Gb/s 8B/10B

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.3.2.1.2 after the entry for 5GBASE-T:

5GBASE-R Clause 129 5 Gb/s 64/66B

30.3.2.1.3 aPhyTypeList

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.3.2.1.3 after the entry for 2.5GBASE-T:

2.5GBASE-X Clause 127 2.5 Gb/s 8B/10B

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.3.2.1.3 after the entry for 5GBASE-T:

5GBASE-R Clause 129 5 Gb/s 64/66B

30.3.2.1.5 aSymbolErrorDuringCarrier

Change the fourth paragraph of "BEHAVIOUR DEFINED AS" in 30.3.2.1.5 as shown:

BEHAVIOUR DEFINED AS:

For operation at 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, 100 Gb/s, 200 Gb/s, and 400 Gb/s, it is a count of the number of times the receiving media is non-idle (the time between the Start of Packet Delimiter and the End of Packet Delimiter as defined by 46.2.5 and 81.2.5) for a period of time equal to or greater than minFrameSize, and during which there was at least one occurrence of an event that causes the PHY to indicate "Receive Error" on the media independent interface (see Table 46–4 and Table 81–4).

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.5.1.1.2 before the entry for 2.5GBASE-T:

2.5GBASE-KX 2.5GBASE-X PMD as specified in Clause 128 over an electrical backplane as specified in Clause 128

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.5.1.1.2 after the entry for 2.5GBASE-T:

2.5GBASE-X 2.5GBASE-X PCS/PMA as specified in Clause 127 over undefined PMD

Insert the following new entries in "APPROPRIATE SYNTAX" in 30.5.1.1.2 before the entry for 5GBASE-T:

5GBASE-KR 5GBASE-KR PMD as specified in Clause 130 over an electrical backplane as specified in Clause 130
5GBASE-R 5GBASE-R PCS/PMA as specified in Clause 129 over undefined PMD

Change the second paragraph of "BEHAVIOUR DEFINED AS" in 30.5.1.1.2 as shown:

The enumerations 1000BASE-X, 1000BASE-XHD, 1000BASE-XFD, 2.5GBASE-X, 5GBASE-R, 10GBASE-X, 10GBASE-R, 10GBASE-W, 25GBASE-R, 40GBASE-R, 100GBASE-R, 200GBASE-R, and 400GBASE-R shall only be returned if the underlying PMD type is unknown.;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 2.5GBASE-T:

2.5GKX 2.5GBASE-KX as specified in Clause 128

Insert the following new entry in "APPROPRIATE SYNTAX" in 30.6.1.1.5 after the entry for 5GBASE-T:

5GKR 5GBASE-KR as specified in Clause 130

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the name of registers 1.160 and 1.161 in Table 45–3 as shown (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
1.160	1000BASE-KX/ 2.5GBASE-KX control	45.2.1.97
1.161	1000BASE-KX/ 2.5GBASE-KX status	45.2.1.98

45.2.1.1 PMA/PMD control 1 register (Register 1.0)

45.2.1.1.5 PMA local loopback (1.0.0)

Change the first sentence of the second paragraph of 45.2.1.1.5 as shown:

The local loopback function is mandatory for the 1000BASE-KX, 2.5GBASE-X, 5GBASE-R, 10GBASE-KR, 10GBASE-X, 40GBASE-KR4, 40GBASE-CR4, and 100GBASE-CR10 port type and optional for all other port types, except 2BASE-TL, 10PASS-TS, and 10/1GBASE-PRX, which do not support loopback.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change the description for bits 1.7.6:0 in Table 45–7 as shown (unchanged table rows and bit description lines not shown):

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
1.7.6:0	PMA/PMD type selection	6 5 4 3 2 1 0 0 1 1 1 1 0 0 = 5GBASE-KR PMA/PMD reserved 0 1 1 1 0 1 1 = 2.5GBASE-KX PMA/PMD reserved	R/W

^aR/W = Read/Write, RO = Read only

45.2.1.7 PMA/PMD status 2 register (Register 1.8)**45.2.1.7.4 Transmit fault (1.8.11)**

Change Table 45-9 by adding the following new rows for 2.5GBASE-KX and 5GBASE-KR as shown (other unchanged rows not shown):

Table 45-9—Transmit fault description location

PMA/PMD	Description location
<u>2.5GBASE-KX</u>	<u>128.6.8</u>
2.5GBASE-T, 5GBASE-T	126.4.2.2
<u>5GBASE-KR</u>	<u>130.6.8</u>

45.2.1.7.5 Receive fault (1.8.10)

Change Table 45-10 by adding the following new rows for 2.5GBASE-KX and 5GBASE-KR as shown (other unchanged rows not shown):

Table 45-10—Receive fault description location

PMA/PMD	Description location
<u>2.5GBASE-KX</u>	<u>128.6.9</u>
2.5GBASE-T, 5GBASE-T	126.4.2.4
<u>5GBASE-KR</u>	<u>130.6.9</u>

45.2.1.8 PMD transmit disable register (Register 1.9)

Change Table 45-12 by adding the following new rows for 2.5GBASE-KX and 5GBASE-KR as shown (other unchanged rows not shown):

Table 45-12—Transmit disable description location

PMA/PMD	Description location
<u>2.5GBASE-KX</u>	<u>128.6.5</u>
2.5GBASE-T and 5GBASE-T	126.4.2.3
<u>5GBASE-KR</u>	<u>130.6.5</u>

45.2.1.18 2.5G/5G PMA/PMD extended ability register (Register 1.21)

Change Table 45–21 as shown:

Table 45–21— 2.5G/5G PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.21.15:24	Reserved	Value always 0	RO
1.21.3	5GBASE-KR ability	1 = PMA/PMD is able to perform 5GBASE-KR 0 = PMA/PMD is not able to perform 5GBASE-KR	RO
1.21.2	2.5GBASE-KX ability	1 = PMA/PMD is able to perform 2.5GBASE-KX 0 = PMA/PMD is not able to perform 2.5GBASE-KX	RO
1.21.1	5GBASE-T ability	1 = PMA/PMD is able to perform 5GBASE-T 0 = PMA/PMD is not able to perform 5GBASE-T	RO
1.21.0	2.5GBASE-T ability	1 = PMA/PMD is able to perform 2.5GBASE-T 0 = PMA/PMD is not able to perform 2.5GBASE-T	RO

^aRO = Read only

Insert the following new subclauses (45.2.1.18.a and 45.2.1.18.b) after the introductory text of 45.2.1.18 (i.e., before 45.2.1.18.1):

45.2.1.18.a 5GBASE-KR ability (1.21.3)

When read as a one, bit 1.21.3 indicates that the PMA/PMD is able to operate as a 5GBASE-KR PMA/PMD type. When read as a zero, bit 1.21.3 indicates that the PMA/PMD is not able to operate as a 5GBASE-KR PMA/PMD type.

45.2.1.18.b 2.5GBASE-KX ability (1.21.2)

When read as a one, bit 1.21.2 indicates that the PMA/PMD is able to operate as a 2.5GBASE-KX PMA/PMD type. When read as a zero, bit 1.21.2 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-KX PMA/PMD type.

45.2.1.89 BASE-R PMD control register (Register 1.150)

Insert the following new paragraph after the first paragraph of 45.2.1.89:

The BASE-R PMD control register is also used by 5GBASE-KR described in Clause 130 to disable the transmitter equalizer for test purposes. 5GBASE-KR does not use the start-up protocol.

Change Table 45-69 as shown:

Table 45-69— BASE-R PMD control register

Bit(s)	Name	Description	R/W ^a
1.150.15:2 1.150.15:3	Reserved	Value always 0	RO
1.150.2	Transmitter equalizer disable	1 = Disable the 5GBASE-KR transmitter equalizer 0 = Normal operation	R/W
1.150.1	Training enable	1 = Enable the BASE-R start-up protocol 0 = Disable the BASE-R start-up protocol	R/W
1.150.0	Restart training	1 = Restart BASE-R start-up protocol 0 = Normal operation	R/W SC

^aR/W = Read/Write, SC = Self-clearing, RO = Read only

Insert the following new subclause (45.2.1.89.3) after 45.2.1.89.2:

45.2.1.89.3 Transmitter equalizer disable (1.150.2)

When bit 1.150.2 is set to one, 5GBASE-KR transmitter equalization is disabled. The default value of bit 1.150.2 is zero.

Change the title and text of 45.2.1.97 as shown:

45.2.1.97 1000BASE-KX/2.5GBASE-KX control register (Register 1.160)

The assignment of bits in the 1000BASE-KX/2.5GBASE-KX control register is shown in Table 45-77.

Change the title of Table 45-77 as shown:

Table 45-77—1000BASE-KX/2.5GBASE-KX control register

45.2.1.97.1 PMD transmit disable (1.160.0)

Change 45.2.1.97.1 as shown:

This bit disables the 1000BASE-KX transmitter as defined in [70.6.5](#) or the 2.5GBASE-KX transmitter as defined in [128.6.5](#).

Change the title and text of 45.2.1.98 as shown:

45.2.1.98 1000BASE-KX/2.5GBASE-KX status register (Register 1.161)

The assignment of bits in the 1000BASE-KX/2.5GBASE-KX status register is shown in Table 45-78.

Change the title of Table 45-78 as shown:

Table 45-78—1000BASE-KX/2.5GBASE-KX status register

Change the title and text of 45.2.1.98.6 as shown:

45.2.1.98.6 1000BASE-KX/2.5GBASE-KX signal detect (1.161.0)

The PMD signal detect function is ~~optional~~ for both 1000BASE-KX PMD (see 70.6.4) and 2.5GBASE-KX PMD (see 128.6.4) is ~~mandatory~~ if EEE is implemented and ~~optional~~ otherwise. The 1000BASE-X PCS and 2.5GBASE-X PCS requires signal detect to be one before synchronization can occur. If the signal detect function is not implemented, this bit is set to one.

45.2.1.140 Test-pattern ability (Register 1.1500)

Change the first paragraph of 45.2.1.140 as shown:

The test-pattern ability register is used for PHY types that implement SSPRQ, square wave, and PRBS testing in the PMA. These functions are described in 127.3.4.1, 83.5.10, and 120.5.11. The assignment of bits in the test-pattern ability register is shown in Table 45–105.

45.2.3 PCS registers

Change the indicated rows of Table 45–176 as shown (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
3.34 through 3.37	5/10/25GBASE-R PCS test pattern seed A	45.2.3.17
3.38 through 3.41	5/10/25GBASE-R PCS test pattern seed B	45.2.3.18

45.2.3.1 PCS control 1 register (Register 3.0)

45.2.3.1.2 Loopback (3.0.14)

Change the first paragraph of 45.2.3.1.2 as shown:

When the 100BASE-T1, any MultiGBASE-T, or the 5/10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.3:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 100BASE-T1, 5/10GBASE-R, or any PCS in the MultiGBASE-T set shall accept data on the transmit path and return it on the receive path. The speed of the loopback is selected by the PCS control 1 (Register 3.0) defined in 45.2.3.1. The specific behavior of the 100BASE-T1 PCS during loopback is specified in 96.3.5. The specific behavior of the 5/10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in 55.3.7.3. The specific behavior for the 25GBASE-T and 40GBASE-T PCS during loopback is specified in 113.3.7.3. The specific behavior for the 2.5GBASE-T or 5GBASE-T PCS during loopback is specified in 126.3.7.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

45.2.3.6 PCS control 2 register (Register 3.7)

Change the description for bits 3.7.3:0 in Table 45–180 as shown (unchanged table rows and bit description lines not shown):

Table 45–180—PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.7.3:0	PCS type selection	<div> <div>3 2 1 0</div> <div>1 1 1 x reserved</div> <div>1 1 1 1 = Select 5GBASE-R PCS type</div> <div>1 1 1 0 = Select 2.5GBASE-X PCS type</div> </div>	R/W

^aRO = Read only, R/W = Read/Write

45.2.3.8 PCS status 3 register (Register 3.9)

Change Table 45–182 as shown:

Table 45–182—PCS status 3 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.9.15:24	Reserved	Value always 0	RO
3.9.3	5GBASE-R capable	<div>1 = PCS is able to support 5GBASE-R PCS type</div> <div>0 = PCS is not able to support 5GBASE-R PCS type</div>	RO
3.9.2	2.5GBASE-X capable	<div>1 = PCS is able to support 2.5GBASE-X PCS type</div> <div>0 = PCS is not able to support 2.5GBASE-X PCS type</div>	RO
3.9.1	400GBASE-R capable	<div>1 = PCS is able to support 400GBASE-R PCS type</div> <div>0 = PCS is not able to support 400GBASE-R PCS type</div>	RO
3.9.0	200GBASE-R capable	<div>1 = PCS is able to support 200GBASE-R PCS types</div> <div>0 = PCS is not able to support 200GBASE-R PCS types</div>	RO

^aRO = Read only

Insert the following new subclauses (45.2.3.8.a and 45.2.3.8.b) after the introductory text of 45.2.3.8 (i.e., before 45.2.3.8.1):

45.2.3.8.a 5GBASE-R capable (3.9.3)

When read as a one, bit 3.9.3 indicates that the PCS is able to support the 5GBASE-R PCS type. When read as a zero, bit 3.9.3 indicates that the PCS is not able to support the 5GBASE-R PCS type.

45.2.3.8.b 2.5GBASE-X capable (3.9.2)

When read as a one, bit 3.9.2 indicates that the PCS is able to support operation in a 2.5GBASE-X PCS type. When read as a zero, bit 3.9.2 indicates that the PCS is not able to support operation in a 2.5GBASE-X PCS type.

45.2.3.11 EEE control and capability 2 register (Register 3.21)

Change Table 45–184 as shown:

Table 45–184—EEE control and capability 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
3.21.15:69	Reserved	Value always 0	RO
<u>3.21.8</u>	<u>5GBASE-KR EEE</u>	<u>1 = EEE is supported for 5GBASE-R</u> <u>0 = EEE is not supported for 5GBASE-R</u>	<u>RO</u>
<u>3.21.7</u>	<u>2.5GBASE-KX EEE</u>	<u>1 = EEE is supported for 2.5GBASE-X</u> <u>0 = EEE is not supported for 2.5GBASE-X</u>	<u>RO</u>
<u>3.21.6</u>	<u>Reserved</u>	<u>Value always 0</u>	<u>RO</u>
3.21.5	400GBASE-R fast wake	1 = EEE fast wake is supported for 400GBASE-R 0 = EEE fast wake is not supported for 400GBASE-R	RO
3.21.4	Reserved	Value always 0	RO
3.21.3	200GBASE-R fast wake	1 = EEE fast wake is supported for 200GBASE-R 0 = EEE fast wake is not supported for 200GBASE-R	RO
3.21.2	25GBASE-T EEE	1 = EEE is supported for 25GBASE-T 0 = EEE is not supported for 25GBASE-T	RO
3.21.1	5GBASE-T EEE	1 = EEE is supported for 5GBASE-T 0 = EEE is not supported for 5GBASE-T	RO
3.21.0	2.5GBASE-T EEE	1 = EEE is supported for 2.5GBASE-T 0 = EEE is not supported for 2.5GBASE-T	RO

^aRO = Read only

Insert the following new subclauses (45.2.3.11.a and 45.2.3.11.b) after the introductory text of 45.2.3.11 (i.e., before 45.2.3.11.1):

45.2.3.11.a 5GBASE-KR EEE supported (3.21.8)

If the device supports EEE operation for 5GBASE-KR as defined in 130.1, this bit shall be set to one.

45.2.3.11.b 2.5GBASE-KX EEE supported (3.21.7)

If the device supports EEE operation for 2.5GBASE-KX as defined in 128.1, this bit shall be set to one.

45.2.3.15 BASE-R and MultiGBASE-T PCS status 1 register (Register 3.32)**45.2.3.15.1 BASE-R and MultiGBASE-T receive link status (3.32.12)**

Change last sentence of 45.2.3.15.1 as shown:

This bit is a reflection of the PCS_status variable defined in 49.2.14.1 for 5/10/25GBASE-R, in 126.3.7.1 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.1 for 10GBASE-T, in 113.3.7.1 for 25GBASE-T and 40GBASE-T, in 82.3.1 for 40/100GBASE-R, and in 119.3 for 200/400GBASE-R.

45.2.3.15.4 BASE-R and MultiGBASE-T PCS high BER (3.32.1)

Change the last sentence of the first paragraph of 45.2.3.15.4 as shown:

This bit is a direct reflection of the state of the `hi_ber` variable in the BER monitor state diagrams as defined in 49.2.13.2.2 for 5/10/25GBASE-R and in 82.2.19.2.2 for 40/100GBASE-R.

45.2.3.15.5 BASE-R and MultiGBASE-T PCS block lock (3.32.0)

Change the third sentence of 45.2.3.15.5 as shown:

For a ~~10GBASE-R~~ or 5/10/25GBASE-R PCS, this bit is a direct reflection of the state of the `block_lock` variable defined in 49.2.13.2.2.

45.2.3.16 BASE-R and MultiGBASE-T PCS status 2 register (Register 3.33)

45.2.3.16.1 Latched block lock (3.33.15)

Change 45.2.3.16.1 as shown:

When read as a one, bit 3.33.15 indicates that the 5/10/25/40/100GBASE-R or a member of the MultiGBASE-T set PCS has achieved block lock. When read as a zero, bit 3.33.15 indicates that the 5/10/25/40/100GBASE-R or a member of the MultiGBASE-T set PCS has lost block lock.

The latched block lock bit shall be implemented with latching low behavior.

This bit is a latching low version of the 5/10/25/40/100GBASE-R and MultiGBASE-T PCS block lock status bit (3.32.0).

45.2.3.16.2 Latched high BER (3.33.14)

Change 45.2.3.16.2 as shown:

When read as a one, bit 3.33.14 indicates that the 5/10/25/40/100GBASE-R or a member of the MultiGBASE-T set PCS has detected a high BER. When read as a zero, bit 3.33.14 indicates that the 5/10/25/40/100GBASE-R or a member of the MultiGBASE-T set PCS has not detected a high BER.

The latched high BER bit shall be implemented with latching high behavior.

This bit is a latching high version of the 5/10/25/40/100GBASE-R and MultiGBASE-T PCS high BER status bit (3.32.1).

45.2.3.16.3 BER(3.33.13:8)

Change the first sentence of 45.2.3.16.3 as shown:

The BER counter is a six-bit count as defined by the `ber_count` variable in 49.2.14.2 and 82.2.19.2.4 for 5/10/25/40/100GBASE-R and defined by counter `lfer_count` in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T.

45.2.3.16.4 Errored blocks (3.33.7:0)

Change the first sentence of 45.2.3.16.4 as shown:

The errored blocks counter is an eight-bit count defined by the counter errored_block_count specified in 49.2.14.2 for 5/10/25GBASE-R, in 82.3.1 for 40/100GBASE-R, in 126.3.7.2 for 2.5GBASE-T and 5GBASE-T, in 55.3.7.2 for 10GBASE-T, and in 113.3.7.2 for 25GBASE-T and 40GBASE-T.

Change the title and the first and second sentences of 45.2.3.17 as shown:

45.2.3.17 5/10/25GBASE-R PCS test pattern seed A (Registers 3.34 through 3.37)

The assignment of bits in the 5/10/25GBASE-R PCS test pattern seed A registers is shown in Table 45–189. This register is only required when the 5GBASE-R, 10GBASE-R, or 25GBASE-R capability is supported.

Change the title of Table 45–189 as shown:

Table 45–189—5/10/25GBASE-R PCS test pattern seed A 0-3 register bit definitions

Change the title and the first and second sentences of 45.2.3.18 as shown:

45.2.3.18 5/10/25GBASE-R PCS test pattern seed B (Registers 3.38 through 3.41)

The assignment of bits in the 5/10/25GBASE-R PCS test pattern seed B registers is shown in Table 45–190. This register is only required when the 5GBASE-R, 10GBASE-R, or 25GBASE-R capability is supported.

Change the title of Table 45–190 as shown:

Table 45–190—5/10/25GBASE-R PCS test pattern seed B 0-3 register bit definitions

45.2.7 Auto-Negotiation registers

45.2.7.2 AN status (Register 7.1)

45.2.7.2.1 Parallel detection fault (7.1.9)

Change 45.2.7.2.1 as shown:

The parallel detection Fault bit (7.1.9) shall be set to one to indicate that more than one of 1000BASE-KX, 2.5GBASE-KX, or 10GBASE-KX4 PMAs have indicated link_status=OK when the autoneg_wait_timer expires. The parallel detection fault bit shall be reset to zero on a read of the AN status register (Register 7.1).

45.2.7.12 Backplane Ethernet, BASE-R copper status (Register 7.48)

Change Table 45–318 by adding the following new rows for 7.48.15 and 7.48.14 in numeric order and deleting the Reserved row as shown (unchanged rows not shown):

**Table 45–318—Backplane Ethernet, BASE-R copper status register (Register 7.48)
bit definitions**

Bit(s)	Name	Description	R/W ^a
7.48.15:14	Reserved	Value always 0	RØ
7.48.15	5GBASE-KR	1 = PMA/PMD is negotiated to perform 5GBASE-KR 0 = PMA/PMD is not negotiated to perform 5GBASE-KR	RO
7.48.14	2.5GBASE-KX	1 = PMA/PMD is negotiated to perform 2.5GGBASE-KX 0 = PMA/PMD is not negotiated to perform 2.5GGBASE-KX	RO

^aRO = Read only

Change the title of 45.2.7.12.3 as shown:

45.2.7.12.3 Negotiated Port Type (7.48.1, 7.48.2, 7.48.3, 7.48.5, 7.48.6, 7.48.8, 7.48.9, 7.48.10, 7.48.11, 7.48.12, 7.48.13, 7.48.14, 7.48.15)

45.2.7.15 EEE advertisement 2 (Register 7.62)

Change Table 45–321 as shown:

Table 45–321—EEE advertisement 2 register (Register 7.62) bit definitions

Bit(s)	Name	Description	Subclause reference; Next Page bit number	R/W ^a
7.62.15:24	Reserved	Value always 0		RO
7.62.3	5GBASE-KR EEE	1 = Advertise that the 5GBASE-KR has EEE capability 0 = Do not advertise that the 5GBASE-KR has EEE capability	73.7.7.1; U17	R/W
7.62.2	2.5GBASE-KX EEE	1 = Advertise that the 2.5GBASE-KX has EEE capability 0 = Do not advertise that the 2.5GBASE-KX has EEE capability	73.7.7.1; U16	R/W
7.62.1	5GBASE-T EEE	1 = Advertise that the 5GBASE-T has EEE capability 0 = Do not advertise that the 5GBASE-T has EEE capability	126.4.2.5.10	R/W
7.62.0	2.5GBASE-T EEE	1 = Advertise that the 2.5GBASE-T has EEE capability 0 = Do not advertise that the 2.5GBASE-T has EEE capability	126.4.2.5.10	R/W

^aR/W = Read/Write, RO = Read only

Insert the following new subclauses (45.2.7.15.a and 45.2.7.15.b) after the introductory text of 45.2.7.15 (i.e., before 45.2.7.15.1):

45.2.7.15.a 5GBASE-KR EEE (7.62.3)

If the device supports EEE operation for 5GBASE-KR as defined in 130.1 and EEE operation is desired, this bit shall be set to one.

45.2.7.15.b 2.5GBASE-KX EEE (7.62.2)

If the device supports EEE operation for 2.5GBASE-KX as defined in 128.1 and EEE operation is desired, this bit shall be set to one.

45.2.7.16 EEE link partner ability 2 (Register 7.63)

Change Table 45–322 as shown:

Table 45–322—EEE advertisement 2 register (Register 7.63) bit definitions

Bit(s)	Name	Description	Subclause reference; Next Page bit number	R/W ^a
7.62.15: 24	Reserved	Value always 0		RO
<u>7.63.3</u>	<u>5GBASE-KR EEE</u>	<u>1 = Link partner is advertising that the 5GBASE-KR has EEE capability</u> <u>0 = Link partner is not advertising that the 5GBASE-KR has EEE capability</u>	<u>73.7.7.1; U17</u>	<u>RO</u>
<u>7.63.2</u>	<u>2.5GBASE-KX EEE</u>	<u>1 = Link partner is advertising that the 2.5GBASE-KX has EEE capability</u> <u>0 = Link partner is not advertising that the 2.5GBASE-KX has EEE capability</u>	<u>73.7.7.1; U16</u>	<u>RO</u>
7.63.1	5GBASE-T EEE	1 = Link partner is advertising that the 5GBASE-T has EEE capability 0 = Link partner is not advertising that the 5GBASE-T has EEE capability	126.4.2.5.10	RO
7.63.0	2.5GBASE-T EEE	1 = Link partner is advertising that the 2.5GBASE-T has EEE capability 0 = Link partner is not advertising that the 2.5GBASE-T has EEE capability	126.4.2.5.10	RO

^aRO = Read only

45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, Management Data Input/Output (MDIO) interface³

45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

45.5.3.2 PMA/PMD MMD options

Change the table in 45.5.3.2 by adding the following new rows for 2.5KX and 5KR as shown (other unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
*2.5T	Implementation of a 2.5GBASE-T PMA	45.2.1.18		PMA:O	Yes [] No []
<u>2.5GKX</u>	<u>Implementation of 2.5GBASE-KX PMA/PMD</u>	<u>45.2.1.18.b</u>		<u>PMA:O</u>	<u>Yes []</u> <u>No []</u>
<u>5GKR</u>	<u>Implementation of 5GBASE-KR PMA/PMD</u>	<u>45.2.1.18.a</u>		<u>PMA:O</u>	<u>Yes []</u> <u>No []</u>
*5T	Implementation of a 2.5GBASE-T PMA	45.2.1.18		PMA:O	Yes [] No []

45.5.3.3 PMA/PMD management functions

Change the MM124 row in the table in 45.5.3.3 as shown (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
MM124	Backplane Ethernet AN ability bit is set to one for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KX ₄ and 10GBASE-KR PHYs.	45.2.7.12.4		<u>2.5GKX:M</u> <u>5GKR:M</u> KX:M KX4:M KR:M	Yes [] N/A []

45.5.3.6 PCS options

Insert the following new rows (for 2.5GX and 5GX) at the end of the table in 45.5.3.6:

Item	Feature	Subclause	Value/Comment	Status	Support
2.5GX	Implementation of 2.5GBASE-X PCS	45.2.3.8		PCS:O	Yes [] No [] N/A []
5GR	Implementation of 5GBASE-R PCS	45.2.3.8		PCS:O	Yes [] No [] N/A []

³Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

46.3 XGMII functional specifications

46.3.3 Error and fault handling

46.3.3.3 Response to received invalid frame sequences

Insert the following new text at the end of 46.3.3.3:

To support 2.5GBASE-X compatibility with a 1000BASE-X PCS/PMA running 2.5 times faster as described in Annex 127A, a 2.5 Gb/s MAC/RS implementation connected to a 2.5GBASE-X PHY is required to support an SFD received on either lane 2 or lane 3.

69. Introduction to Ethernet operation over electrical backplanes

69.1 Overview

69.1.1 Scope

Change the first sentence of the second paragraph of 69.1.1 as shown:

Backplane Ethernet supports the IEEE 802.3 full duplex MAC operating at 1000 Mb/s, 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, 40 Gb/s, or 100 Gb/s providing a bit error ratio (BER) better than or equal to 10^{-12} at the MAC/PLS service interface.

Insert the following new lines after the 1000BASE-KX line in the list after the second paragraph of 69.1.1:

- 2.5GBASE-KX for 2.5 Gb/s operation over a single lane
- 5GBASE-KR for 5 Gb/s operation over a single lane

69.1.2 Relationship of Backplane Ethernet to the ISO OSI reference model

Change the first paragraph of 69.1.2 as shown:

Backplane Ethernet couples the IEEE 802.3 MAC to a family of Physical Layers defined for operation over electrical backplanes. The relationships among Backplane Ethernet, the IEEE 802.3 MAC, and the ISO Open System Interconnection (OSI) reference model are shown in [Figure 69-1](#), [Figure 69-2](#), ~~and~~ [Figure 69-3](#), ~~and~~ [Figure 69-4](#).

Insert the new figure on the next page (Figure 69-4) after Figure 69-3.

Change list item i) in the lettered list of 69.1.2 as shown:

- i) The MDIs for 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, 10GBASE-KR, 25GBASE-KR, and 25GBASE-KR-S use a serial data path while the MDIs for 10GBASE-KX4, 40GBASE-KR4, 100GBASE-KR4, and 100GBASE-KP4 use a four-lane data path.

IEEE Std 802.3cb-2018
IEEE Standard for Ethernet—Amendment 1: Physical Layer Specifications and Management Parameters
for 2.5 Gb/s and 5 Gb/s Operation over Backplane

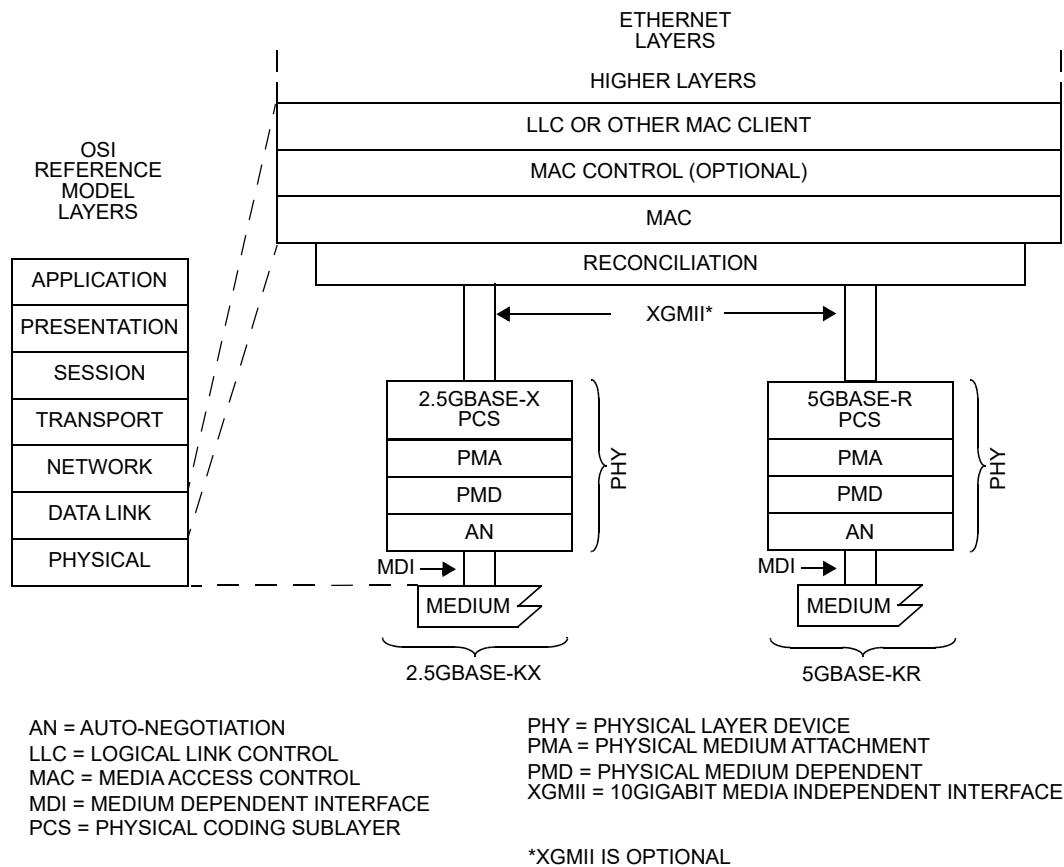


Figure 69-4—Architectural positioning of 2.5 Gb/s and 5 Gb/s Backplane Ethernet

69.2 Summary of Backplane Ethernet Sublayers

69.2.3 Physical Layer signaling systems

Insert the following new paragraphs after the first paragraph (“Backplane Ethernet extends”) in 69.2.3:

Backplane Ethernet also extends the family of 2.5GBASE-X Physical Layer signaling systems to include 2.5GBASE-KX. This embodiment specifies operation at 2.5 Gb/s over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 2.5GBASE-X PCS and PMA as defined in Clause 127. The 2.5GBASE-KX PMD is defined in Clause 128.

Backplane Ethernet also extends the family of 5GBASE-R Physical Layer signaling systems to include the 5GBASE-KR. This embodiment specifies 5 Gb/s operation over two differential, controlled impedance pairs of traces (one pair for transmit, one pair for receive). This system employs the 5GBASE-R PCS and PMA as defined in Clause 129. The 5GBASE-KR PMD is defined in Clause 130.

Change the last paragraph in 69.2.3 as shown:

Table 69-1, Table 69-1a, Table 69-2, and Table 69-3 specify the correlation between nomenclature and clauses. A complete implementation conforming to one or more nomenclatures meets the requirements of the corresponding clauses.

Insert the following new table (Table 69–1a) after Table 69-1:

Table 69–1a—Nomenclature and clause correlation for 2.5 Gb/s and 5 Gb/s Backplane Ethernet Physical Layers

Nomenclature	Clause							
	46		73	78	127	128	129	130
	RS	XGMII	Auto-Negotiation	Energy-Efficient Ethernet (EEE)	2.5GBASE-X PCS/PMA	2.5GBASE-KX PMD	5GBASE-R PCS/PMA	5GBASE-KR PMD
2.5GBASE-KX	M ^a	O ^a	M	O	M	M		
5GBASE-KR	M	O	M	O			M	M

^aO = Optional, M = Mandatory

69.3 Delay constraints

Insert the following new paragraph after the third paragraph (“Table 69-5”) of 69.3:

For 2.5GBASE-KX, normative delay specifications may be found in 127.5 and 128.4. For 5GBASE-KR, normative delay specifications may be found in 129.5 and 130.4. They are also referenced in 125.3.

69.5 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 69.5 as shown:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, [Clause 70](#) through [Clause 74](#), [Clause 84](#), [Clause 91](#), [Clause 93](#), [Clause 94](#), [Clause 108](#), [Clause 111](#), [Clause 128](#), [Clause 130](#), and related annexes demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

70. Physical Medium Dependent sublayer and baseband medium, type 1000BASE-KX

70.5 PMD MDIO function mapping

Change Table 70–2 as shown:

Table 70–2—MDIO/PMD control variable mapping

MDIO control variable	PMA/PMD register name	Register/ bit number	PMD control variable
Reset	Control register 1	1.0.15	PMD_reset
PMD Transmit Disable	1000BASE-KX/2.5GBASE-KX control register	1.160.0	PMD_transmit_disable

Change Table 70–3 as shown:

Table 70–3—MDIO/PMD status variable mapping

MDIO status variable	PMA/PMD register name	Register/ bit number	PMD status variable
Fault	Status register 1	1.1.7	PMD_fault
Transmit fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.13	PMD_Transmit_fault_ability
Receive fault ability	1000BASE-KX/2.5GBASE-KX status register	1.161.12	PMD_Receive_fault_ability
Transmit fault	1000BASE-KX/2.5GBASE-KX status register	1.161.11	PMD_transmit_fault
Receive fault	1000BASE-KX/2.5GBASE-KX status register	1.161.10	PMD_receive_fault
PMD transmit disable ability	1000BASE-KX/2.5GBASE-KX status register	1.161.8	PMD_transmit_disable_ability
Signal detect from PMD	1000BASE-KX/2.5GBASE-KX status register	1.161.0	PMD_signal_detect

73. Auto-Negotiation for backplane and copper cable assembly

73.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

Replace Figure 73–1 with the following figure (which adds 2.5 Gb/s and 5 Gb/s in the medium rates):

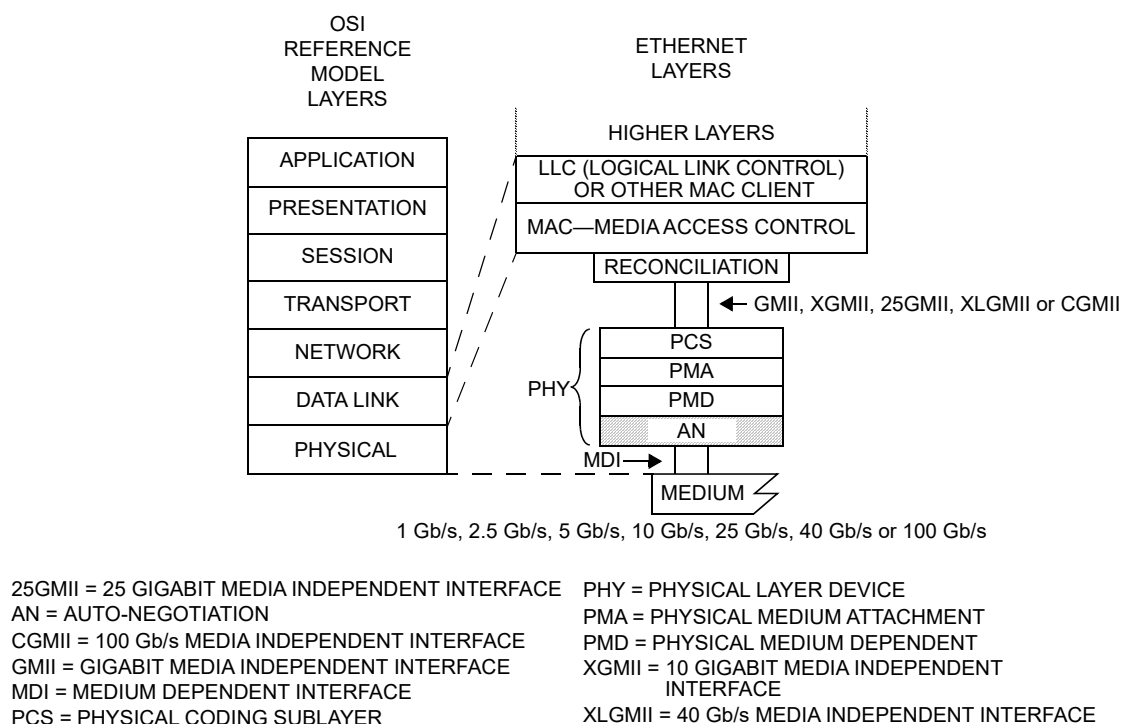


Figure 73–1—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

73.6 Link codeword encoding

73.6.4 Technology Ability Field

Change Table 73–4 by adding the following new rows for A11 and A12 in numeric order and revising the reserved row as shown (unchanged rows not shown):

Table 73–4—Technology Ability Field encoding

Bit	Technology
<u>A11</u>	<u>2.5GBASE-KX</u>
<u>A12</u>	<u>5GBASE-KR</u>
A11 A13 through A22	Reserved for future technology

Change the last paragraph of 73.6.4 as shown:

The fields A[22:13+4] are reserved for future use. Reserved fields shall be sent as zero and ignored on receive.

73.7 Receive function requirements

73.7.4 Arbitration function requirements

73.7.4.1 Parallel Detection function

Change the first two paragraphs of 73.7.4.1 as shown:

The local device detects a link partner that supports Auto-Negotiation by DME page detection. The Parallel Detection function allows detection of link partners that support 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 but have disabled Auto-Negotiation, and detection of legacy devices that can interoperate with 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 devices but do not provide [Clause 73](#) Auto-Negotiation.

A local device shall provide Parallel Detection for 1000BASE-KX, 2.5GBASE-KX, and 10GBASE-KX4 if it supports those PHYs. Additionally, parallel detection may be used for 10GBASE-CX4. Parallel detection of 10GBASE-CX4 will be indicated by the setting of the Negotiated Port Type to “10GBASE-KX4 or 10GBASE-CX4” in the management register bit 7.48.2. The means to distinguish between 10GBASE-KX4 and 10GBASE-CX4 is implementation dependent. Parallel Detection shall be performed by directing the MDI receive activity to the PHY. This detection may be done in sequence between detection of DME pages and detection of each supported PHY. If at least one of the 1000BASE-KX, 2.5GBASE-KX, or 10GBASE-KX4 establishes link_status=OK, the LINK STATUS CHECK state is entered and the autoneg_wait timer is started. If exactly one link_status=OK indication is present when the autoneg_wait timer expires, then Auto-Negotiation shall set link_control=ENABLE for the PHY indicating link_status=OK. If a PHY is enabled, the Arbitration function shall set link_control=DISABLE to all other PHYs and indicate that Auto-Negotiation has completed. On transition to the AN GOOD CHECK state from the LINK STATUS CHECK state, the Parallel Detection function shall set the bit in the AN LP Base Page ability registers (see [45.2.7.7](#)) corresponding to the technology detected by the Parallel Detection function.

73.7.6 Priority Resolution function

Change Table 73-5 by adding the following new rows for Priority 11 and Priority 12 in numeric order and revising the last row as shown (unchanged rows not shown):

Table 73-5—Priority Resolution

Priority	Technology	Capability
<u>11</u>	<u>5GBASE-KR</u>	<u>5 Gb/s 1 lane</u>
<u>12</u>	<u>2.5GBASE-KX</u>	<u>2.5 Gb/s 1 lane</u>
4+13	1000BASE-KX	1 Gb/s 1 lane, lowest priority

73.10 State diagrams and variable definitions

73.10.1 State diagram variables

Insert the following new entries (for 2.5GKX and 5GKR) after the entry for 1GKX in the variable list after the first paragraph ('A variable with "[x]"') in 73.10.1:

2.5GKX; represents the 2.5GBASE-KX PMD.
5GKR; represents the 5GBASE-KR PMD.

Change the PD entry in the variable list after the first paragraph ('A variable with "[x]"') in 73.10.1 as shown:

PD; represents all of the following that are present: 1000BASE-KX PMD, 2.5GBASE-KX PMD, and 10GBASE-KX4 (or 10GBASE-CX4) PMD.

Change the single_link_ready entry in the list after the third paragraph ('Variables of the form "mr_x",') in 73.10.1 as shown:

single_link_ready

Status indicating that an_receive_idle = true and only one of the following indications is being received:

- 1) link_status_[1GKX] = OK
- 2) link_status_[2.5GKX] = OK
- 3) link_status_[5GKR] = OK
- 4) link_status_[10GKX4] = OK
- 5) link_status_[10GKR] = OK
- 6) link_status_[25GR] = OK
- 7) link_status_[40GKR4] = OK
- 8) link_status_[40GCR4] = OK
- 9) link_status_[100GCR10] = OK
- 10) link_status_[100GKP4] = OK
- 11) link_status_[100GKR4] = OK
- 12) link_status_[100GCR4] = OK

73.10.2 State diagram timers

Change the two link_fail_inhibit_timer rows in Table 73-7 as shown (unchanged rows not shown):

Table 73-7—Timer min/max value summary

Parameter	Min	Value and tolerance	Max	Units
link_fail_inhibit_timer (when the link is not <u>neither</u> 1000BASE-KX, 2.5GBASE-KX, 5GBASE-KR, or not 10GBASE-KX4)	500		510	ms
link_fail_inhibit_timer (when the link is 1000BASE-KX, <u>2.5GBASE-KX</u> , <u>5GBASE-KR</u> , or 10GBASE-KX4)	40		50	ms