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AMENDMENT 8
2021-10

Telecommunications and exchange between information technology systems — Requirements for local and metropolitan area networks —

Part 3: Standard for Ethernet

AMENDMENT 8: Physical layer specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s automotive electrical ethernet

Télécommunications et échange entre systèmes informatiques — Exigences pour les réseaux locaux et métropolitains —

Partie 3: Norme pour Ethernet

AMENDEMENT 8: Spécifications des couches physiques et paramètres de gestion pour l'ethernet électrique automobile à 2,5 Gb/s, 5Gb/s et 10 Gb/s

Reference number
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IEEE Std 802.3ch™-2020
(Amendment to IEEE Std 802.3™-2018
as amended by IEEE Std 802.3cb™-2018,
IEEE Std 802.3bt™-2018,
IEEE Std 802.3cd™-2018,
IEEE Std 802.3cn™-2019,
IEEE Std 802.3cg™-2019,
IEEE Std 802.3cq™-2020,
and IEEE Std 802.3cm™-2020)

IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet

Developed by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

Approved 4 June 2020

IEEE SA Standards Board

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Abstract: This amendment to IEEE Std 802.3-2018 adds physical layer specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation on a single balanced pair of conductors suitable for automotive applications.

Keywords: 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1, Ethernet, IEEE 802.3ch™, MASTER-SLAVE, Medium Dependent Interface, Physical Coding Sublayer, Physical Layer, Physical Medium Attachment

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Introduction

This introduction is not part of IEEE Std 802.3ch-2020, IEEE Standard for Ethernet. Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2018 and are not maintained as separate documents.

At the date of IEEE Std 802.3ch-2020 publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2018

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

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services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 126 and Annex 119A through Annex 120E. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well the 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 and Clause 126 include general information on 2.5 Gb/s and 5 Gb/s operation as well as 2.5 Gb/s and 5 Gb/s Physical Layer specifications.

IEEE Std 802.3cb™-2018

Amendment 1—This amendment includes changes to IEEE Std 802.3-2018 and its amendments, and adds Clause 127 through Clause 130, Annex 127A, Annex 128A, Annex 128B, and Annex 130A. This amendment adds new Physical Layers for operation at 2.5 Gb/s and 5 Gb/s over electrical backplanes.

IEEE Std 802.3bt™-2018

Amendment 2—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 145, Annex 145A, Annex 145B, and Annex 145C. This amendment adds power delivery using all four pairs in the structured wiring plant, resulting in greater power being available to end devices. This amendment also allows for lower standby power consumption in end devices and adds a mechanism to better manage the available power budget.

IEEE Std 802.3cd™-2018

Amendment 3—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 131 through Clause 140 and Annex 135A through Annex 136D. This amendment adds MAC parameters, Physical Layers, and management parameters for the transfer of IEEE 802.3 format frames at 50 Gb/s, 100 Gb/s, and 200 Gb/s.

IEEE Std 802.3cn™-2019

Amendment 4—This amendment includes changes to IEEE Std 802.3-2018 and adds 50 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications and management parameters for operation over single-mode fiber with reaches of at least 40 km.

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IEEE Std 802.3cg™-2019

Amendment 5—This amendment includes changes to IEEE Std 802.3-2018 and its amendments and adds Clause 146 through Clause 148 and Annex 146A and Annex 146B. This amendment adds 10 Mb/s Physical Layer specifications and management parameters for operation on a single balanced pair of conductors.

IEEE Std 802.3cq™-2020

Amendment 6—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 33 and related portions of the standard.

IEEE Std 802.3cm™-2020

Amendment 7—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 150. This amendment adds Physical Layer (PHY) specifications and management parameters for 400 Gb/s operation on four pairs (400GBASE-SR4.2) and eight pairs (400GBASE-SR8) of multimode fiber, over reaches of at least 100 m.

IEEE Std 802.3ch™-2020

Amendment 8—This amendment includes changes to IEEE Std 802.3-2018 and adds Clause 149, Annex 149A, Annex 149B, and Annex 149C. This amendment adds physical layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s over a single balanced pair of conductors.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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IEEE Standard for Ethernet

Amendment 8: Physical Layer Specifications and Management Parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Automotive Electrical Ethernet

(This amendment is based on IEEE Std 802.3™-2018 as amended by IEEE Std 802.3cb™-2018, IEEE Std 802.3bt™-2018, IEEE Std 802.3cd™-2018, IEEE Std 802.3cn™-2019, IEEE Std 802.3cg™-2019, IEEE Std 802.3cq™-2020, and IEEE Std 802.3cm™-2020.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.[1]

[1] Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

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1. Introduction

1.3 Normative references

Insert the following references in 1.3 in alphanumeric order as follows:

IEC 62153-4-7, Metallic communication cable test methods—Part 4-7: Electromagnetic compatibility (EMC)—Test method for measuring of transfer impedance Z_T and screening attenuation a_S or coupling attenuation a_C of connectors and assemblies up to and above 3 GHz—Triaxial tube in tube method.[2]

1.4 Definitions

Insert a new definition for 10GBASE-T1 after 1.4.69 10GBASE-T as follows:

1.4.69a 10GBASE-T1: IEEE 802.3 Physical Layer specification for a 10 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for 2.5GBASE-T1 after 1.4.82 2.5GBASE-T and before 1.4.82a 2.5GBASE-X (as inserted by IEEE Std 802.3cb-2018) as follows:

1.4.82aa 2.5GBASE-T1: IEEE 802.3 Physical Layer specification for a 2.5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for 5GBASE-T1 after 1.4.129 5GBASE-T and before 1.4.129a 5GSEI (as inserted by IEEE Std 802.3cb-2018) as follows:

1.4.129aa 5GBASE-T1: IEEE 802.3 Physical Layer specification for a 5 Gb/s Ethernet full duplex local area network over a single balanced pair of conductors. (See IEEE Std 802.3, Clause 149.)

Change the definition of Infofield in 1.4.289 as follows:

1.4.289 Infofield: A 16 octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 55, Clause 113, and Clause 126.) Also a 12-octet frame transmitted at regular intervals containing messages for startup operation by certain PHYs. (See IEEE Std 802.3, Clause 97 and Clause 149.)

Insert a new definition for MultiGBASE-T1 after 1.4.333 MultiGBASE-T (re-numbered from 1.4.334 due to the deletion of 1.4.294 by IEEE Std 802.3bt-2018) as follows:

1.4.333a MultiGBASE-T1: PHYs that belong to the set of specific BASE-T1 PHYs at speeds in excess of 1000 Mb/s, including 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1. (See IEEE Std 802.3, Clause 149.)

Insert a new definition for Type F PoDL System after 1.4.494a Type E PoDL System (as inserted by IEEE Std 802.3cg-2019) as follows:

1.4.494b Type F PoDL System: A system comprising a PoDL PSE, link section, and PD that are compatible with 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1.

[2]IEC publications are available from the International Electrotechnical Commission (https://www.iec.ch/) and the American National Standards Institute (https://www.ansi.org).

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1.5 Abbreviations

Insert the following new abbreviation into the list, in alphanumeric order:

RFER	RS-FEC frame error ratio

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30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 Clause 149 2.5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "5GBASE-T" (and before the entry for "5GBASE-R" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1 Clause 149 5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "10GBASE-T" as follows:

10GBASE-T1 Clause 149 10 Gb/s PAM4

30.3.2.1.3 aPhyTypeList

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1 Clause 149 2.5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "5GBASE-T" (and before the entry for "5GBASE-R" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1 Clause 149 5 Gb/s PAM4

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "10GBASE-T" as follows:

10GBASE-T1 Clause 149 10 Gb/s PAM4

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30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "2.5GBASE-T" (and before the entry for "2.5GBASE-X" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "5GBASE-T" as follows:

5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "10GBASE-T" as follows:

10GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 149

30.5.1.1.4 aMediaAvailable

Change the fifth sentence of the eighth paragraph of the BEHAVIOUR DEFINED AS section of 30.5.1.1.4 as follows:

> Where a Clause 45 MDIO interface is present a zero in the PMA/PMD Receive link status bit (45.2.1.2.4) maps to the enumeration "PMD link fault", a one in the LOF status bit (45.2.2.10.4) maps to the enumeration "WIS frame loss", a one in the LOS status bit (45.2.2.10.5) maps to the enumeration "WIS signal loss", a zero in the PCS Receive link status bit (45.2.3.2.7 or 45.2.3.80.1) maps to the enumeration "PCS link fault", a one in the 10/40/100GBASE-R PCS Latched high BER status bit (45.2.3.16.2) or a one in the MultiGBASE-T1 PCS status 2 Latched high BER status bit (45.2.3.80.4) maps to the enumeration "excessive BER", a zero in the DTE XS receive link status bit (45.2.5.2.7) maps to the enumeration "DXS link fault" and a zero in the PHY XS transmit link status bit (45.2.4.2.7) maps to the enumeration "PXS link fault".;

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "2.5GBASE-T" (and before the entry for "2.5GKX" inserted by IEEE Std 802.3cb-2018) as follows:

2.5GBASE-T1	2.5GBASE-T1 as specified in Clause 149

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "5GBASE-T" (and before the entry for "5GKR" inserted by IEEE Std 802.3cb-2018) as follows:

5GBASE-T1	5GBASE-T1 as specified in Clause 149

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Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "10GBASE-T" as follows:

10GBASE-T1 10GBASE-T1 as specified in Clause 149

30.15 Layer management for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet

30.15.1 PoDL PSE managed object class

30.15.1.1 PoDL PSE attributes

30.15.1.1.4 aPoDLPSEType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.4 after the entry for "typeE" (inserted by IEEE Std 802.3cg-2019) as follows:

typeF Type F PoDL PSE

30.15.1.1.5 aPoDLPSEDetectedPDType

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.15.1.1.5 after the entry for "typeE" (inserted by IEEE Std 802.3cg-2019) as follows:

typeF Type F PoDL PD

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44. Introduction to 10 Gb/s baseband network

44.1 Overview

44.1.1 Scope

Change the first paragraph of 44.1.1 as follows:

10 Gigabit Ethernet uses the IEEE 802.3 MAC sublayer, connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer entities such as 10GBASE-SR, 10GBASE-LX4, 10GBASE-CX4, 10GBASE-LRM, 10GBASE-LR, 10GBASE-ER, 10GBASE-SW, 10GBASE-LW, 10GBASE-EW, ~~and~~10GBASE-T, and 10GBASE-T1.

44.1.2 Objectives

Insert the following text as new item h) and renumber existing item h) to item i) of 44.1.2 as follows:

h) Support operation over a single balanced pair of conductors.

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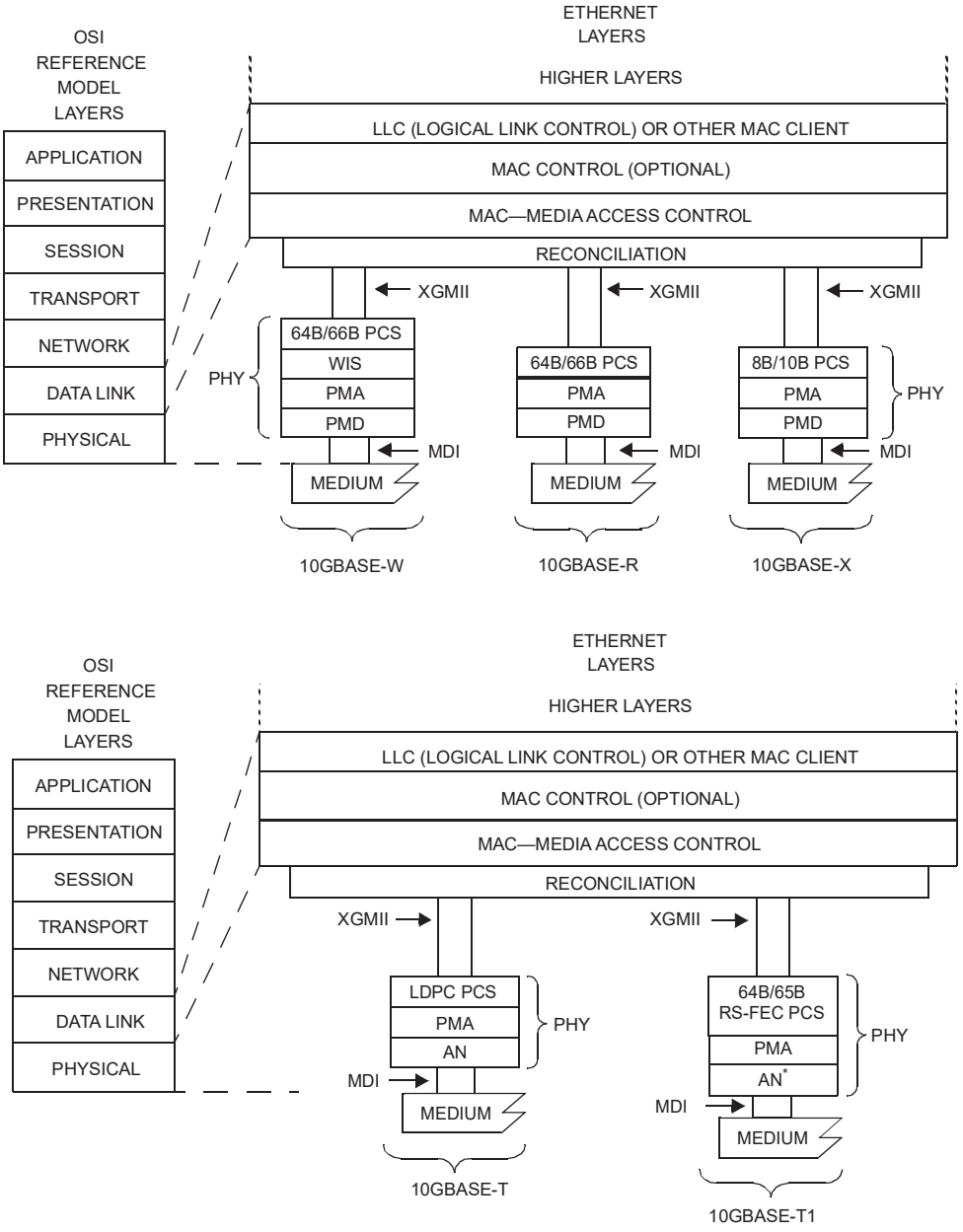
44.1.3 Relationship of 10 Gigabit Ethernet to the ISO OSI reference model

Replace Figure 44-1 with the following figure, which adds 10GBASE-T1:



AN = AUTO-NEGOTIATION SUBLAYER
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER DEVICE
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
WIS = WAN INTERFACE SUBLAYER
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE
* AUTO-NEGOTIATION IS OPTIONAL

Figure 44–1—Architectural positioning of 10 Gigabit Ethernet

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Change item d) of 44.1.3 as follows:

d) The MDI as specified in Clause 53 for 10GBASE-LX4, in Clause 54 for 10GBASE-CX4, in Clause 55 for 10GBASE-T, in Clause 68 for 10GBASE-LRM, in Clause 149 for 10GBASE-T1, and in Clause 52 for other PMD types.

44.1.4 Summary of 10 Gigabit Ethernet sublayers

44.1.4.1 Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

Change the second paragraph of 44.1.4.1 as follows:

While the XGMII is an optional interface, it is used extensively in this standard as a basis for functional specification and provides a common service interface for Clause 47, Clause 48, Clause 49, ~~and~~ Clause 55, and Clause 149.

44.1.4.4 Physical Layer signaling systems

Change Table 44–1 as follows:

Table 44–1—Nomenclature and clause correlation

Nomenclature	Clause[a]											
	48	49	50	51	52			53	54	55	68	149
	8B/10B PCS & PMA	64B/66B PCS	WIS	Serial PMA	850 nm Serial PMD	1310 nm Serial PMD	1550 nm Serial PMD	1310 nm WDM PMD	4-Lane electrical PMD	~~Twisted pair~~ LDPC PCS & 4-pair PMA	1310 nm Serial MMF PMD	RS–FEC PCS & 1-pair PMA
10GBASE-SR		M[a]		M	M							
10GBASE-SW		M	M	M	M							
10GBASE-LX4	M							M				
10GBASE-CX4	M								M			
10GBASE-LR		M		M		M						
10GBASE-LW		M	M	M		M						
10GBASE-ER		M		M			M					
10GBASE-EW		M	M	M			M					
10GBASE-T										M		
10GBASE-LRM		M		M							M	
10GBASE-T1												M

[a] M = Mandatory

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Insert the following paragraph between paragraphs 6 and 7 in 44.1.4.4 as follows:

The term 10GBASE-T1, specified in Clause 149, refers to a specific Physical Layer implementation based upon 64B/65B data coding method placed in an RS-FEC frame that is Gray-code mapped to PAM4 for transmission over a single balanced pair of conductors.

Change former paragraph 7 (now paragraph 8 due to the above insertion) in 44.1.4.4 as follows:

Physical Layer device specifications are contained in Clause 52, Clause 53, Clause 54, Clause 55, ~~and~~ Clause 68, and Clause 149.

44.3 Delay constraints

Insert new rows at the end of Table 44–2 as follows (unchanged rows not shown):

Table 44–2—Round-trip delay constraints (informative)

Sublayer	Maximum (bit time)	Maximum (pause_quanta)	Notes
…			
10GBASE-T1 no interleave	10 240	20	See 149.10.
10GBASE-T1 2x interleave	13 824	27	See 149.10.
10GBASE-T1 4x interleave	20 480	40	See 149.10.

44.4 Protocol implementation conformance statement (PICS) proforma

Change the first paragraph of 44.4 as follows:

The supplier of a protocol implementation that is claimed to conform to any part of IEEE Std 802.3, Clause 45 through Clause 55, ~~and~~ Clause 68, and Clause 149, demonstrates compliance by completing a protocol implementation conformance statement (PICS) proforma.

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45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Insert new rows in Table 45–3 for registers 1.2309 to 1.2315 after row for register 1.2308, and change the appropriate reserved row as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.2309	MultiGBASE-T1 PMA control	45.2.1.192
1.2310	MultiGBASE-T1 PMA status	45.2.1.193
1.2311	MultiGBASE-T1 training	45.2.1.194
1.2312	MultiGBASE-T1 link partner training	45.2.1.195
1.2313	MultiGBASE-T1 test mode control	45.2.1.196
1.2314	MultiGBASE-T1 SNR operating margin	45.2.1.197
1.2315	MultiGBASE-T1 minimum SNR margin	45.2.1.198
1.2316	MultiGBASE-T1 user defined data	45.2.1.199
1.2317	MultiGBASE-T1 link partner user defined data	45.2.1.200
1.~~2309~~2318 through 1.32767	Reserved	
…		

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert a new row in Table 45–9 immediately after the row for "2.5GBASE-T, 5GBASE-T" as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.2
…	

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45.2.1.7.5 Receive fault (1.8.10)

Insert a new row in Table 45–10 immediately after row for "2.5GBASE-T, 5GBASE-T" as follows (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1	149.4.2.3
…	

45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18)

Change the identified reserved row in Table 45–19 (as modified by IEEE Std 802.3cg-2019) and insert new rows immediately below the changed row as follows (unchanged rows not shown):

Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:~~4~~7	Reserved	Value always 0	RO
1.18.6	10GBASE-T1 ability	1 = PMA/PMD is able to perform 10GBASE-T1 0 = PMA/PMD is not able to perform 10GBASE-T1	RO
1.18.5	5GBASE-T1 ability	1 = PMA/PMD is able to perform 5GBASE-T1 0 = PMA/PMD is not able to perform 5GBASE-T1	RO
1.18.4	2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 2.5GBASE-T1 0 = PMA/PMD is not able to perform 2.5GBASE-T1	RO
…			

[a]RO = Read only

Insert 45.2.1.16.1, 45.2.1.16.2, and 45.2.1.16.3 at the end of 45.2.1.16 as follows:

45.2.1.16.1 10GBASE-T1 ability (1.18.6)

When read as a one, bit 1.18.6 indicates that the PMA/PMD is able to operate as a 10GBASE-T1 PMA type. When read as a zero, bit 1.18.6 indicates that the PMA/PMD is not able to operate as a 10GBASE-T1 PMA type.

45.2.1.16.2 5GBASE-T1 ability (1.18.5)

When read as a one, bit 1.18.5 indicates that the PMA/PMD is able to operate as a 5GBASE-T1 PMA type. When read as a zero, bit 1.18.5 indicates that the PMA/PMD is not able to operate as a 5GBASE-T1 PMA type.

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45.2.1.16.3 2.5GBASE-T1 ability (1.18.4)

When read as a one, bit 1.18.4 indicates that the PMA/PMD is able to operate as a 2.5GBASE-T1 PMA type. When read as a zero, bit 1.18.4 indicates that the PMA/PMD is not able to operate as a 2.5GBASE-T1 PMA type.

45.2.1.18 2.5G/5G PMA/PMD extended ability register (Register 1.21)

Insert the following note at the end of 45.2.1.18 (below Table 45–21):

NOTE—2.5GBASE-T1 and 5GBASE-T1 PMA/PMD extended abilities can be found in Register 1.18, see Table 45–19.

45.2.1.185 BASE-T1 PMA/PMD control register (1.2100)

Change the row for bits 1.2100.3:0 in Table 45–149 (as modified by IEEE Std 802.3cg-2019) (unchanged rows not shown) as follows:

Table 45–149—BASE-T1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.3:0	Type Selection	3 2 1 0 1 x x x = Reserved ~~0 1 x x = Reserved~~ 0 1 1 1 = Reserved 0 1 1 0 = 10GBASE-T1 0 1 0 1 = 5GBASE-T1 0 1 0 0 = 2.5GBASE-T1 0 0 1 1 = 10BASE-T1S 0 0 1 0 = 10BASE-T1L 0 0 0 1 = 1000BASE-T1 0 0 0 0 = 100BASE-T1	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.185.2 Type selection (1.2100.3:0)

Insert the following text after the fifth sentence of 45.2.1.185.2 (as modified by IEEE Std 802.3cg-2019) as follows:

When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is 10GBASE-T1.

Insert 45.2.1.192 through 45.2.1.196 after 45.2.1.191 as follows:

45.2.1.192 MultiGBASE-T1 PMA control register (Register 1.2309)

The assignment of bits in the MultiGBASE-T1 PMA control register is shown in Table 45–155a.

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Table 45–155a—MultiGBASE-T1 PMA control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2309.15	PMA/PMD reset	1 = PMA/PMD reset 0 = Normal operation	R/W, SC
1.2309.14	Transmit disable	1 = Transmit disable 0 = Normal operation	R/W
1.2309.13:12	Reserved	Value always 0	RO
1.2309.11	Low-power	1 = Low-power mode 0 = Normal operation	R/W
1.2309.10:0	Reserved	Value always 0	RO

[a]R/W = Read/Write, RO = Read only, SC = Self-clearing

45.2.1.192.1 PMA/PMD reset (1.2309.15)

Resetting the MultiGBASE-T1 PMA/PMD is accomplished by setting bit 1.2309.15 to a one. This action shall set all PMA/PMD registers to their default states. As a consequence, this action may change the internal state of a MultiGBASE-T1 PMA/PMD and the state of the physical link. This action may also initiate a reset in any other MMDs that are instantiated in the same package. Bit 1.2309.15 is self-clearing, and the MultiGBASE-T1 PMA/PMD shall return a value of one in bit 1.2309.15 when a reset is in progress; otherwise, it shall return a value of zero. The MultiGBASE-T1 PMA/PMD is not required to accept a write transaction to any of its registers until the reset process is completed. The control and management interface shall be restored to operation as defined in 149.4.2.1, starting when bit 1.2309.15 is set.

During a reset, the MultiGBASE-T1 PMA/PMD shall respond to reads from register bits 1.2309.15, 1.8.15:14, and 1.0.15. All other register bits shall be ignored.

NOTE—This operation may interrupt data communication.

Bit 1.2309.15 is a copy of bit 1.0.15 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall reset the MultiGBASE-T1 PMA/PMD.

45.2.1.192.2 Transmit disable (1.2309.14)

When bit 1.2309.14 is set to a one, the PMA shall disable output on the transmit path. When bit 1.2309.14 is set to a zero, the PMA shall enable output on the transmit path.

Bit 1.2309.14 is a copy of bit 1.9.0 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall disable the transmitter.

45.2.1.192.3 Low power (1.2309.11)

When the low-power ability is supported, the MultiGBASE-T1 PMA/PMD may be placed into a low-power mode by setting bit 1.2309.11 to one. This action may also initiate a low-power mode in any other MMDs that are instantiated in the same package. The low-power mode is exited by resetting the MultiGBASE-T1 PMA/PMD. The behavior of the MultiGBASE-T1 PMA/PMD in transition to and from the low-power mode is implementation specific and any interface signals should not be relied upon. While in the low-power

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mode, the device shall, at a minimum, respond to management transactions necessary to exit the low-power mode.

The default value of bit 1.2309.11 is zero.

This operation interrupts data communication.

Bit 1.2309.11 is a copy of bit 1.0.11 and setting or clearing either bit shall set or clear the other bit. Setting either bit shall put the MultiGBASE-T1 PMA/PMD in low-power mode.

45.2.1.193 MultiGBASE-T1 PMA status register (1.2310)

The assignment of bits in the MultiGBASE-T1 PMA status register is shown in Table 45–155b.

Table 45–155b—MultiGBASE-T1 PMA status register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2310.15:12	Reserved	Value always 0	RO
1.2310.11	MultiGBASE-T1 OAM ability	1 = PHY has MultiGBASE-T1 OAM ability 0 = PHY does not have MultiGBASE-T1 OAM ability	RO
1.2310.10	EEE ability	1 = PHY has EEE ability 0 = PHY does not have EEE ability	RO
1.2310.9	Receive fault ability	1 = PMA/PMD has the ability to detect a fault condition on the receive path 0 = PMA/PMD does not have the ability to detect a fault condition on the receive path	RO
1.2310.8	Low-power ability	1 = PMA/PMD has low-power ability 0 = PMA/PMD does not have low-power ability	RO
1.2310.7:5	Reserved	Value always 0	RO
1.2310.4:3	PrecodeSel	4 3 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO
1.2310.2	Receive polarity	1 = Receive polarity is reversed 0 = Receive polarity is not reversed	RO
1.2310.1	Receive fault	1 = Fault condition detected 0 = Fault condition not detected	RO/LH
1.2310.0	Receive link status	1 = PMA/PMD receive link up 0 = PMA/PMD receive link down	RO/LL

[a]RO = Read only, LH = Latching High, LL = Latching Low

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45.2.1.193.1 MultiGBASE-T1 OAM ability (1.2310.11)

When read as a one, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY supports MultiGBASE-T1 OAM (see 149.3.9). When read as a zero, bit 1.2310.11 indicates that the MultiGBASE-T1 PHY does not support MultiGBASE-T1 OAM.

45.2.1.193.2 EEE ability (1.2310.10)

When read as a one, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY supports EEE. When read as a zero, bit 1.2310.10 indicates that the MultiGBASE-T1 PHY does not support EEE.

45.2.1.193.3 Receive fault ability (1.2310.9)

When read as a one, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD has the ability to detect a fault condition on the receive path. When read as a zero, bit 1.2310.9 indicates that the MultiGBASE-T1 PMA/PMD does not have the ability to detect a fault condition on the receive path.

45.2.1.193.4 Low-power ability (1.2310.8)

When read as a one, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD supports the low-power feature. When read as a zero, bit 1.2310.8 indicates that the MultiGBASE-T1 PMA/PMD does not support the low-power feature. If the MultiGBASE-T1 PMA/PMD supports the low-power feature, then it is controlled using either bit 1.2309.11 or bit 1.0.11.

45.2.1.193.5 PrecodeSel (1.2310.4:3)

Bits 1.2310.4:3 contain the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

45.2.1.193.6 Receive polarity (1.2310.2)

When read as zero, bit 1.2310.2 indicates that the polarity of the receiver is not reversed. When read as one, bit 1.2310.2 indicates that the polarity of the receiver is reversed.

45.2.1.193.7 Receive fault (1.2310.1)

When read as a one, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has detected a fault condition on the receive path. When read as a zero, bit 1.2310.1 indicates that the MultiGBASE-T1 PMA/PMD has not detected a fault condition on the receive path. Detection of a fault condition on the receive path is optional and the ability to detect such a condition is advertised by bit 1.2310.9. A MultiGBASE-T1 PMA/PMD that is unable to detect a fault condition on the receive path shall return a value of zero for bit 1.2310.1. The receive fault bit shall be implemented with latching high behavior.

45.2.1.193.8 Receive link status (1.2310.0)

When read as a one, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link is up. When read as a zero, bit 1.2310.0 indicates that the MultiGBASE-T1 PMA/PMD receive link has been down one or more times since the register was last read. The receive link status bit shall be implemented with latching low behavior.

45.2.1.194 MultiGBASE-T1 training register (1.2311)

The assignment of bits in the MultiGBASE-T1 training register is shown in Table 45–155c.

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Table 45–155c—MultiGBASE-T1 training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2311.15:13	Reserved	Value always 0	RO
1.2311.12:11	Interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	R/W
1.2311.10:6	Reserved	Value always 0	RO
1.2311.5	Precoder selection	Controls requested precoder setting 0 = PHY 1 = User	R/W
1.2311.4	Slow Wake request	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	R/W
1.2311.3:2	User precoder selection	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	R/W
1.2311.1	MultiGBASE-T1 OAM advertisement	1 = MultiGBASE-T1 OAM ability advertised to link partner 0 = MultiGBASE-T1 OAM ability not advertised to link partner	R/W
1.2311.0	EEE advertisement	1 = EEE ability advertised to link partner 0 = EEE ability not advertised to link partner	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.194.1 Interleave request (1.2311.12:11)

Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated to the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. If bits 1.2311.12:11 are set to these undefined values, the PHY will communicate these values to the link partner, but the requested interleaver depth is out of scope of this standard and may not be supported by the link partner.

45.2.1.194.2 Precoder selection (1.2311.5)

When bit 1.2311.5 is set to a one, the PHY shall use bits 1.2311.3:2 for the value of PrecodeSel, and when set to a zero the PHY controls the value of PrecodeSel. PrecodeSel is the desired precoder setting communicated to the link partner via the Infofield specified in 149.4.2.4.5.

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45.2.1.194.3 Slow Wake request (1.2311.4)

When set as a one, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may only transmit alert immediately following refresh. When set as a zero, bit 1.2311.4 indicates to the link partner that the local MultiGBASE-T1 PHY may transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.194.4 User precoder selection (1.2311.3:2)

When bit 1.2311.5 is a one, bits 1.2311.3:2 are the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see 149.4.2.4.5).

45.2.1.194.5 MultiGBASE-T1 OAM advertisement (1.2311.1)

Support for MultiGBASE-T1 OAM capability shall be advertised if bit 1.2311.1 is set to one. Support for MultiGBASE-T1 OAM capability shall not be advertised if bit 1.2311.1 is set to zero. Support for MultGBASE-T1 OAM capability should only be advertised if it is supported by the PHY.

45.2.1.194.6 EEE advertisement (1.2311.0)

Support for EEE capability shall be advertised if bit 1.2311.0 is set to one. Support for EEE capability shall not be advertised if bit 1.2311.0 is set to zero. Support for EEE operation should only be advertised if it is supported by the PHY.

45.2.1.195 MultiGBASE-T1 link partner training register (1.2312)

The assignment of bits in the MultiGBASE-T1 link partner training register is shown in Table 45–155d. The values in this register are not valid when the link is down.

Table 45–155d—MultiGBASE-T1 link partner training register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2312.15:13	Reserved	Value always 0	RO
1.2312.12:11	Link partner interleave request	12 11 0 0: L=1, no interleaving, default for 2.5GBASE-T1 0 1: L=2, RS-FEC interleaving factor two, default for 5GBASE-T1, undefined for 2.5GBASE-T1 1 0: L=4, RS-FEC interleaving factor four, default for 10GBASE-T1, undefined for 2.5GBASE-T1 and 5GBASE-T1 1 1: Reserved	RO
1.2312.10:5	Reserved	Value always 0	RO
1.2312.4	Link partner Slow Wake requested	1 = Alert window start is only immediate frame after refresh 0 = Alert window start is every 8th RS frame after refresh	RO
1.2312.3:2	Link partner precoder requested	3 2 0 0 = no precoder requested 0 1 = 1–D precoder requested 1 0 = 1+D precoder requested 1 1 = $1–D^2$ precoder requested	RO

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Table 45–155d—MultiGBASE-T1 link partner training register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.2312.1	Link partner MultiGBASE-T1 OAM advertisement	1 = Link partner has MultiGBASE-T1 OAM ability 0 = Link partner does not have MultiGBASE-T1 OAM ability	RO
1.2312.0	Link partner EEE advertisement	1 = Link partner has EEE ability 0 = Link partner does not have EEE ability	RO

[a]RO = Read only

45.2.1.195.1 Link partner interleave request (1.2312.12:11)

Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in 149.3.2.2.15. This is communicated by the link partner via Infofields as specified in 149.4.2.4.5.

The values of L = 2 and L = 4 are not defined for 2.5GBASE-T1 PHYs, and the value of L = 4 is not defined for 5GBASE-T1 PHYs. Bits 1.2312.12:11 will indicate whatever value is received from the link partner, but if the undefined values are received, the requested interleaver depth is out of scope of this standard and may not be supported by the local PHY.

45.2.1.195.2 Link partner Slow Wake requested (1.2312.4)

Bit 1.2312.4 contains the Slow Wake setting received from the link partner. When set as a one, the link partner may only transmit alert immediately following refresh. When set as a zero, the link partner may only transmit an alert at any eighth RS-FEC frame after a refresh.

45.2.1.195.3 Link partner precoder requested (1.2312.3:2)

Bits 1.2312.3:2 contain the precoder setting requested by the link partner. The precoder requested is encoded as the value of precoder_type defined in 149.3.2.2.20.

45.2.1.195.4 Link partner MultiGBASE-T1 OAM advertisement (1.2312.1)

When read as a one, bit 1.2312.1 indicates the link partner is advertising MultiGBASE-T1 OAM capability. When read as a zero, bit 1.2312.1 indicates the link partner is not advertising MultiGBASE-T1 OAM capability. MultiGBASE-T1 OAM capability shall be enabled only when both the local PHY and its link partner are advertising MultiGBASE-T1 OAM capability.

45.2.1.195.5 Link partner EEE advertisement (1.2312.0)

When read as a one, bit 1.2312.0 indicates the link partner is advertising EEE capability. When read as a zero, bit 1.2312.0 indicates the link partner is not advertising EEE capability. EEE capability shall be enabled only when both the local PHY and its link partner are advertising EEE capability.

45.2.1.196 MultiGBASE-T1 test mode control register (1.2313)

The assignment of bits in the MultiGBASE-T1 test mode control register is shown in Table 45–155e. The default values for each bit are chosen so that the initial state of the device upon power up or reset is a normal operational state without management intervention.

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Table 45–155e—MultiGBASE-T1 test mode control register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2313.15:13	Test mode control	15 14 13 1 1 1 = Test mode 7 1 1 0 = Test mode 6 1 0 1 = Test mode 5 1 0 0 = Test mode 4 0 1 1 = Test mode 3 0 1 0 = Test mode 2 0 0 1 = Test mode 1 0 0 0 = Normal (non-test) operation	R/W
1.2313.12	Reserved	Value always 0	RO
1.2313.11	Local transmitter precoder override	0 = Normal operation 1 = User override	R/W
1.2313.10:9	Local transmit precoder setting	10 9 0 0 = transmit with no precoder 0 1 = transmit with 1–D precoder 1 0 = transmit with 1+D precoder 1 1 = transmit with $1–D^2$ precoder	R/W
1.2313.8:2	Reserved	Value always 0	RO
1.2313.1:0	Jitter test control	1 0 0 0 = Square wave 0 1 = JP03A Pattern 1 0 = JP03B Pattern 1 1 = Reserved	R/W

[a]RO = Read only, R/W = Read/Write

45.2.1.196.1 Test mode control (1.2313.15:13)

Transmitter test mode operations defined by bits 1.2313.15:13, are described in 149.5.1 and Table 149–17. The default value for bits 1.2313.15:13 is zero.

45.2.1.196.2 Local transmitter precoder override (1.2313.11)

When bit 1.2313.11 is set to one, the local transmitter's precoder shall be controlled by the value of bits 1.2313.10:9, and the precoder requested by the link partner in PrecodeSel shall be ignored. When bit 1.2313.11 is set to zero, the transmitter shall ignore bits 1.2313.10:9, and the precoder is set according to the value of PrecodeSel received from the link partner as specified in 149.3.2.2.20. The default value of 1.2313.11 is zero.

45.2.1.196.3 Local transmit precoder setting (1.2313.10:9)

When bit 1.2313.11 is set to one, bits 1.2313.10:9 control the precoder setting of the local transmitter, as defined in 149.3.2.2.20 in the variable precoder_type.

45.2.1.196.4 Jitter test control (1.2313.1:0)

When the transmitter is in test mode 2, bits 1.2313.1:0 control the pattern of the jitter test signal. When the transmitter is not in test mode 2, the setting of bits 1.2313.1:0 has no effect. A value of 00 transmits a square

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wave from the transmitter, a value of 01 transmits the JP03A pattern, and a value of 10 transmits the JP03B pattern. See 149.5.2.3.1 and 149.5.2.3.2 for more information.

45.2.1.197 MultiGBASE-T1 SNR operating margin register (Register 1.2314)

Register 1.2314 contains the current SNR operating margin measured at the slicer input for the PMAs in the MultiGBASE-T1 set. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 SNR operating margin register is shown in Table 45–155f.

Table 45–155f—MultiGBASE-T1 SNR operating margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2314.15:8	MultiGBASE-T1 SNR operating margin	Value of current SNR operating margin in dB	RO
1.2314.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.198 MultiGBASE-T1 minimum SNR margin register (Register 1.2315)

Register 1.2315 contains a latched copy of the lowest value observed in the MultiGBASE-T1 SNR operating margin register (1.2314) since the last read. It is reported with 0.1 dB of resolution to an accuracy of 0.5 dB within the range of –12.7 dB to 12.7 dB. The number is in offset binary notation, with 0.0 dB represented by 0x80, 12.7 dB represented by 0xFF, and –12.7 dB represented by 0x01. Implementation of this register is optional.

The assignment of bits in the MultiGBASE-T1 minimum SNR margin register is shown in Table 45–155g.

Table 45–155g—MultiGBASE-T1 minimum SNR margin register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2315.15:8	MultiGBASE-T1 minimum SNR margin	Value of minimum observed SNR margin in dB	RO
1.2315.7:0	Reserved	Value always 0	RO

[a]RO = Read only

45.2.1.199 MultiGBASE-T1 user defined data (Register 1.2316)

The assignment of bits for the MultiGBASE-T1 user defined data register is shown in Table 45–155h. The values of the bits in this register are outside the scope of this standard.

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Table 45–155h—MultiGBASE-T1 user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2316.15:0	MultiGBASE-T1 user defined data	16 bits of vendor specific data that the PHY sends to its link partner	R/W

[a]R/W = Read/Write

45.2.1.199.1 MultiGBASE-T1 user defined data (1.2316.15:0)

Bits 1.2316.15:0 contain vendor specific data that the PHY may communicate to its link partner during training.

45.2.1.200 MultiGBASE-T1 link partner user defined data register (Register 1.2317)

The assignment of bits for the MultiGBASE-T1 link partner user defined data register is shown in 45–155i. The values of the bits in this register are outside the scope of this standard.

Table 45–155i—MultiGBASE-T1 link partner user defined data register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2317.15:0	MultiGBASE-T1 link partner user defined data	16 bits of vendor specific data that the PHY may receive from its link partner	RO

[a]RO = Read only

45.2.1.200.1 MultiGBASE-T1 link partner user defined data register (1.2317.15:0)

Bits 1.2317.15:0 contain vendor specific data that the PHY may receive from its link partner during training.

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45.2.3 PCS registers

Change the rows for registers 3.2308 through 3.2317, insert new rows for registers 1.2318 to 1.2324 after row for register 1.2317 and change the appropriate reserved row in Table 45–176 as follows (unchanged rows not shown):

Table 45–176—PCS registers

Register address	Register name	Subclause
…		
3.~~32~~2308	~~1000~~BASE-T1 OAM transmit	45.2.3.72
3.2309 through 3.2312	~~1000~~BASE-T1 OAM message	45.2.3.73
3.2313	~~1000~~BASE-T1 OAM receive	45.2.3.74
3.2314 through 3.2317	Link partner ~~1000~~BASE-T1 OAM message	45.2.3.75
3.2318 through 3.2319	MultiGBASE-T1 OAM status message	45.2.3.76
3.2320 through 3.2321	Link partner MultiGBASE-T1 OAM status message	45.2.3.77
3.2322	MultiGBASE-T1 PCS control	45.2.3.78
3.2323	MultiGBASE-T1 PCS status 1	45.2.3.79
3.2324	MultiGBASE-T1 PCS status 2	45.2.3.80
3.23~~18~~25 through 3.32767	Reserved	
…		

Change the titles, text, and tables in 45.2.3.72 through 45.2.3.75 as follows:

45.2.3.72 ~~1000~~BASE-T1 OAM transmit register (Register 3.2308)

The assignment of bits in the ~~1000~~BASE-T1 OAM transmit register is shown in Table 45–241.

Table 45–241—~~1000~~BASE-T1 OAM transmit register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2308.15	~~1000~~BASE-T1 OAM message valid	This bit is used to indicate message data in registers 3.2308.11:8, 3.2309, 3.2310, 3.2311, and 3.2312 are valid and ready to be loaded. This bit ~~shall~~ self-clears when registers are loaded by the OAM transmit state diagram. ~~machine.~~ 1 = Message data in registers are valid 0 = Message data in registers are not valid	R/W, SC
3.2308.14	Toggle value	Toggle value to be transmitted with message. This bit is set by the state machine and cannot be overridden by the user.	RO
3.2308.13	~~1000~~BASE-T1 OAM message received	This bit shall self clear on read. 1 = ~~1000~~BASE-T1 OAM message received by link partner 0 = ~~1000~~BASE-T1 OAM message not received by link partner	RO, LH

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Table 45–241—~~1000~~BASE-T1 OAM transmit register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
3.2308.12	Received message toggle value	Toggle value of message that was received by link partner as indicated in 3.2308.13.	RO
3.2308.11:8	Message number	User-defined message number to send	R/W
3.2308.7:4	Reserved	Value always 0	RO
3.2308.3	Ping received	Received PingTx value from latest good ~~1000~~BASE-T1 OAM frame received	RO
3.2308.2	Ping transmit	Ping value to send to link partner	R/W
3.2308.1:0	Local SNR	00 = PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current ~~1000~~BASE-T1 OAM frame. 01 = LPI refresh is insufficient to maintain PHY SNR. Request link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.	RO

[a]RO = Read only, R/W = Read/Write, LH = Latching High, SC = Self-clearing

45.2.3.72.1 ~~1000~~BASE-T1 OAM message valid (3.2308.15)

Bit 3.2308.15 shall be set to one when the ~~1000~~BASE-T1 OAM message to be transmitted in registers 3.2309, 3.2310, 3.2311, and 3.2312 and the message number in 3.2308.11:8 are properly configured to be transmitted. ~~This register shall be cleared by the state machine~~ Bit 3.2308.15 self-clears to indicate whether the next ~~1000~~BASE-T1 OAM message can be written into the registers.

45.2.3.72.2 Toggle value (3.2308.14)

The state machine shall assign a value alternating between zero and one to associate with the ~~8-octet~~ 8-octet ~~1000~~BASE-T1 OAM message transmitted by the ~~1000BASE-T1~~ PHY. Bit 3.2308.14 should be read and recorded prior to setting 3.2308.15 to one. The recorded value can be correlated with 3.2308.12 as a confirmation that the ~~1000~~BASE-T1 OAM message is received by the link partner.

45.2.3.72.3 ~~1000~~BASE-T1 OAM message received (3.2308.13)

Bit 3.2308.13 shall indicate whether the most recently transmitted ~~1000~~BASE-T1 OAM message with a toggle bit value in 3.2308.12 was received, read, and acknowledged by the link partner. This variable shall clear on read.

45.2.3.72.4 Received message toggle value (3.2308.12)

Bit 3.2308.12 indicates the toggle bit value of the ~~1000~~BASE-T1 OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if 3.2308.13 is one.

45.2.3.72.5 Message number (3.2308.11:8)

Bits 3.2308.11:8 contain the ~~1000~~BASE-T1 OAM message number to be transmitted. This field is user defined but it is recommended that it be used to indicate the meaning of the ~~8-octet~~ 8-octet ~~1000~~BASE-T1

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OAM message. If used this way, up to 16 different 8-octet messages can be exchanged. The message number is user defined and its definition is outside the scope of this standard.

45.2.3.72.6 Ping received (3.2308.3)

Bit 3.2308.3 represents the value of the most recent Ping RX received from the link partner (see 97.3.8.2.3).

45.2.3.72.7 Ping transmit (3.2308.2)

Bit 3.2308.2 represents the value to be sent to the link partner via the Ping TX function (see 97.3.8.2.4).

45.2.3.72.8 Local SNR (3.2308.1:0)

Bits 3.2308.1:0 are set by the ~~1000~~BASE-T1 PHY to indicate the status of the receiver. The definitions of good, marginal, when to request idles, and when to request retrain are implementation dependent.

45.2.3.73 ~~1000~~BASE-T1 OAM message register (Registers 3.2309 to 3.2312)

The ~~1000~~BASE-T1 OAM message register contains the 8-octet ~~1000~~BASE-T1 OAM message data to be transmitted. The 8-octet message data is user defined and its definition is outside the scope of this standard. See Table 45–242.

Table 45–242—~~1000~~BASE-T1 OAM message register bit definitions

Bit(s)	Name	Description	R/W[a]
3.2309.15:8	~~1000~~BASE-T1 OAM message 1	Message octet 1. LSB transmitted first.	R/W
3.2309.7:0	~~1000~~BASE-T1 OAM message 0	Message octet 0. LSB transmitted first.	R/W
3.2310.15:8	~~1000~~BASE-T1 OAM message 3	Message octet 3. LSB transmitted first.	R/W
3.2310.7:0	~~1000~~BASE-T1 OAM message 2	Message octet 2. LSB transmitted first.	R/W
3.2311.15:8	~~1000~~BASE-T1 OAM message 5	Message octet 5. LSB transmitted first.	R/W
3.2311.7:0	~~1000~~BASE-T1 OAM message 4	Message octet 4. LSB transmitted first.	R/W
3.2312.15:8	~~1000~~BASE-T1 OAM message 7	Message octet 7. LSB transmitted first.	R/W
3.2312.7:0	~~1000~~BASE-T1 OAM message 6	Message octet 6. LSB transmitted first.	R/W

[a]R/W = Read/Write

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