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GENERAL CHARACTERISTICS OF INTERNATIONAL TELEPHONE CONNECTIONS AND INTERNATIONAL TELEPHONE CIRCUITS

A COMMON DIGITAL PARALLEL INTERFACE FOR SPEECH STANDARDISATION ACTIVITIES

ITU-T Recommendation G.192

(Previously "CCITT Recommendation")

FOREWORD

The ITU-T (Telecommunication Standardization Sector) is a permanent organ of the International Telecommunication Union (ITU). The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

ITU-T Recommendation G.192 was prepared by ITU-T Study Group 15 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 19th of March 1996.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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ABSTRACT

This Recommendation defines the physical, electrical and logical specification of a digital parallel interface which is to be used to interconnect the different devices needed in standardisation activities of speech codecs sponsored by the ITU-T.

Included in this Recommendation are the data formats at the input and output of the encoder, decoder and bit manipulation devices.

Finally, rules for the implementation of codecs to guarantee proper interoperation of devices interconnected using that digital parallel interface are presented.

Recommendation G.192

A COMMON DIGITAL PARALLEL INTERFACE FOR
SPEECH STANDARDISATION ACTIVITIES

(Geneva, 1996)

1 Scope

This Recommendation describes a 16-bit parallel input and output interface for the interconnection of test and reference devices in ITU-T standardisation activities.

2 Introduction

The history of the Digital Parallel Interface (DPI) specification goes back to the CCITT wideband speech 64 kbit/s codec tests that led to the present Recommendation G.722, where a similar parallel interface was used. That interface was simplified to fit into a 25-pin connector for the host laboratory sessions of the subjective tests of the GSM full rate codec. This simplified interface has also been used in the standardisation of the second generation GSM system and in the standardisation of the ITU-T 8 kbit/s speech coder. The interface is simple to build and easy to use and, compared to a serial interface, allows for a simpler access to the data flow for monitoring and measuring codec parameters, e.g. delay and timing.

This Recommendation is structured as follows: initially an overview of the principles of the interface is given, with a functional description of the signals and data lines. Then hardware aspects are considered. Specialisations of the interface are given in the annexes. These specialisations involve:

- the DPI implementation using TTL family integrated circuits;
- description of data formats based on the type of device where the DPI is employed;
- device implementation rules when the device is a speech coder; and
- configuration examples for the DPI.

For information, a description of the specialisation used for the host laboratory work of the ITU-T 8 kbit/s coder is given as an appendix.

3 Definitions

For the purposes of this Recommendation, the following definitions and abbreviations apply.

- 3.1 codec:** An encoder/decoder pair.
- 3.2 coded bitstream signal:** One of the possible signal representations on the DPI, in general representing the signal at the output of an encoder, or the input of a decoder. May also be the representation of a communication channel.
- 3.3 CuT:** Codec under Test.
- 3.4 DPD:** Digital Processing Device.
- 3.5 DPI:** The Digital Parallel Interface defined in this Recommendation.
- 3.6 interface timeslot (INTI):** A rising-edge to rising-edge time interval of the clock signal. A marked INTI refers to a INTI that occurs together with the Mark signal active (high) and an unmarked INTI when Mark is low.
- 3.7 LSb:** Least Significant bit.
- 3.8 mark signal (mark):** A one-bit signal that indicates whether the data on the data bus is valid or not.
- 3.9 MSb:** Most Significant bit.

3.10 normal operation: Mode of operation of the interface used for regular processing by the devices. Alternative to the reset operation.

3.11 reset operation: A procedure started when the Reset signal is active for 16 INTIs, and that lasts 1616 INTIs in total. Used to synchronise all the devices in the chain to their initial reset state. After the end of the Reset Operation, the DPI and the interconnected devices resume Normal Operation.

NOTE – 1616 INTIs represent 1 ms (16 INTIs) plus 100 ms (1600 INTIs) for a 16 kHz clock.

3.12 reset: Active-low, one bit signal used to start the Reset Operation.

3.13 Rx_Clk: Backwards clock signal. Used to clock devices when the clock master lies in one of the intermediate devices of the chain.

3.14 softbit: An element of the coded bitstream signal where logical bits '1' and '0' are represented by 16-bit right adjusted words.

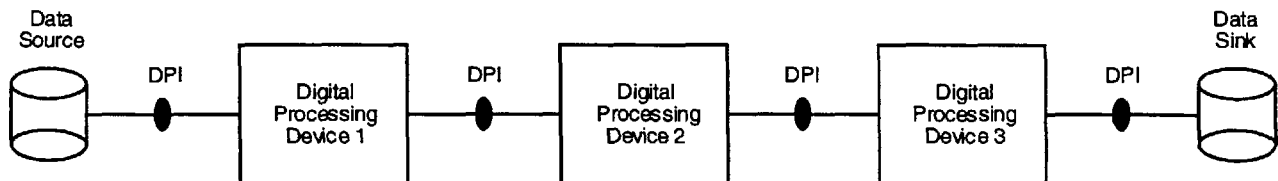
3.15 synchronisation word: An element of the coded bitstream signal provided for synchronisation and frame erasure purposes.

3.16 time signal: Another of the possible signal representations on the DPI, in general representing time samples. Used necessarily between data source, data sink, and codecs.

3.17 Tx_Clk: Forward clock signal. A continuous-time running signal providing the basic rate of the interconnected devices.

4 General Description of the Digital Parallel Interface

Normally, a set of digital test data is processed over different Codecs under Test (CuT) during a standardisation procedure of a speech codec by the ITU-T. Figure 1 shows an example of test configuration where three Digital Processing Devices (DPD) are interconnected by means of the DPI. Each of the DPD have an input and an output DPI.



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FIGURE 1/G.192

A generic test configuration where the DPI is used

A set of digital test data (usually digitised speech) is sent out synchronously from the data source to the first DPD, what could be the encoding portion of a CuT. Processed data is then sent in an appropriate format to the second DPD in the chain, for example a channel model. After processing by the second DPD, data is sent to the final DPD in the example chain, what could be the decoding portion of a CuT. Data out of this last DPD is finally collected by the data sink. It should be noted that the data type in the different usages of the DPI in Figure 1 does not need to have the same format.

Any number of DPD could be connected in principle, allowing to build complex structures (e.g. to simulate a tandem of codecs in two different digital cellular mobile systems). Other application examples are given in Annex D.

The interface is able to transport in parallel up to 16 bits of Data (D15..D0) from one device (transmitter) to another (receiver). Valid data words are identified by mark bits.

A clock signal is transmitted in parallel with the data lines of the interface in the forward direction (Tx_Clk). A clock signal is also available in the backward direction (Rx_Clk), what can be used for special purposes. An active-low /Reset signal is applied for synchronisation of the devices in a chain.

4.1 Logical Description

Test hardware configurations may differ in each standardisation process. However, the basic format for the data passing through the DPI is the same. It is composed of 16-bit data words, clocked in and out at a certain rate (e.g. 16 kHz) and marked as valid or invalid by a special mark bit, as indicated in Figure 2. The transmission throughout the test configuration is processed synchronously and the mark bit identifies whether the preceding device was ready to send out data or not.

Figure 3 describes a generic hardware structure for the DPI. All data, mark and clock lines are buffered in both transmitter and receiver ends. The data and mark bits are stored in a parallel register during one interface timeslot. The hardware structure is independent of the logic family used, but the same family is needed for a given pair transmitter and receiver interconnected ends. If a termination is needed to reduce signal reflections, it needs to be adequate (and possibly specific) to the logic family chosen.

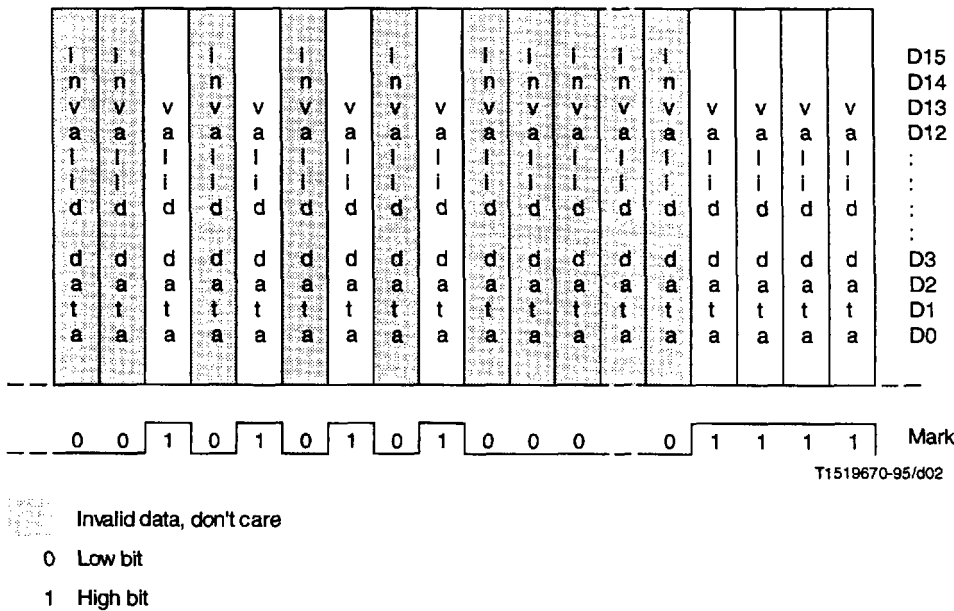


FIGURE 2/G.192
Example for a possible data flow in the DPI

While Figure 3 displays the interface from the point of view of two interconnected devices, Figure 4 displays the interface from a given device's point of view. There it can be seen where the algorithm resides, the data lines it is supposed to use, and how the other control signals are routed inside and through the given DPD. Examples are given in Figure 4 for 3 device setups. This figure is further described in 4.2.

Currently only a TTL (Transistor-Transistor Logic) implementation of the basic hardware has been tested and used. Its description is given in Annex A.

4.2 Master Clock and Reset

The clock signal for devices interconnected by the DPI must be generated by only one device in the chain. This master clock in the simplest case is provided by the data source. In this case, only a clock line in the forward direction is necessary, i.e. from the data source towards the data sink through the interconnected devices.