



INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

G.726

**GENERAL ASPECTS OF DIGITAL
TRANSMISSION SYSTEMS;
TERMINAL EQUIPMENTS**

**40, 32, 24, 16 kbit/s ADAPTIVE
DIFFERENTIAL PULSE CODE
MODULATION (ADPCM)**

Recommendation G.726



Geneva, 1990



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FOREWORD

The CCITT (the International Telegraph and Telephone Consultative Committee) is a permanent organ of the International Telecommunication Union (ITU). CCITT is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The Plenary Assembly of CCITT which meets every four years, establishes the topics for study and approves Recommendations prepared by its Study Groups. The approval of Recommendations by the members of CCITT between Plenary Assemblies is covered by the procedure laid down in CCITT Resolution No. 2 (Melbourne, 1988).

Recommendation G.726 was prepared by Study Group XV and was approved under the Resolution No. 2 procedure on the 14 of December 1990.

CCITT NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication Administration and a recognized private operating agency.

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Recommendation G.726

40, 32, 24, 16 kbit/s ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION (ADPCM)¹⁾

1 General

The characteristics below are recommended for the conversion of a 64 kbit/s A-law or μ -law pulse code modulation (PCM) channel to and from a 40, 32, 24 or 16 kbit/s channel. The conversion is applied to the PCM bit stream using an ADPCM transcoding technique. The relationship between the voice frequency signals and the PCM encoding/decoding laws is fully specified in Recommendation G.711.

The principal application of 24 and 16 kbit/s channels is for overload channels carrying voice in Digital Circuit Multiplication Equipment (DCME).

The principal application of 40 kbit/s channels is to carry data modem signals in DCME, especially for modems operating at greater than 4800 kbit/s.

Sections 1.1 and 1.2 of this Recommendation provide an outline description of the ADPCM transcoding algorithm, §§ 2 and 3 provide the principles and functional descriptions of the ADPCM encoding and decoding algorithms respectively, whilst § 4 is the precise specification for the algorithm computations. Networking aspects and digital test sequences are addressed in Appendices I and II, respectively, to this Recommendation.

Simplified block diagrams of both the ADPCM encoder and decoder are shown in Figure 1/G.726.

In § 4, each sub-block in the encoder and decoder is precisely defined using one particular logical sequence. If other methods of computation are used, extreme care should be taken to ensure that they yield *exactly* the same value for the output processing variables. Any further departures from the processes detailed in § 4 will incur performance penalties which may be severe.

Note 1 – Prior to the definition of this Recommendation, other ADPCM algorithms of performance similar to the 40 kbit/s algorithm specified here have been incorporated in DCME designs and used in telecommunications networks. These algorithms may be considered by bilateral agreement for limited DCME applications under certain circumstances. Technical descriptions providing information on two such algorithm approaches can be found in COM XVIII No. 101 and COM XVIII No. 102 of the 1984-1988 Study Period.

Note 2 – The assignment of 16, 24, 32 and 40 kbit/s DCME channels and the associated selection of coding rates are beyond the scope of this Recommendation; see, for example, Recommendation G.763 (revised, 1990).

Note 3 – Signalling and multiplexing considerations are beyond the scope of this Recommendation; see, for example, Recommendations G.761 and G.763 (revised, 1990).

¹⁾ This Recommendation completely replaces the text of Recommendations G.721 and G.723 published in Volume III.4 of the Blue Book. It should be noted that systems designed in accordance with the present Recommendation will be compatible with systems designed in accordance with the Blue Book version.

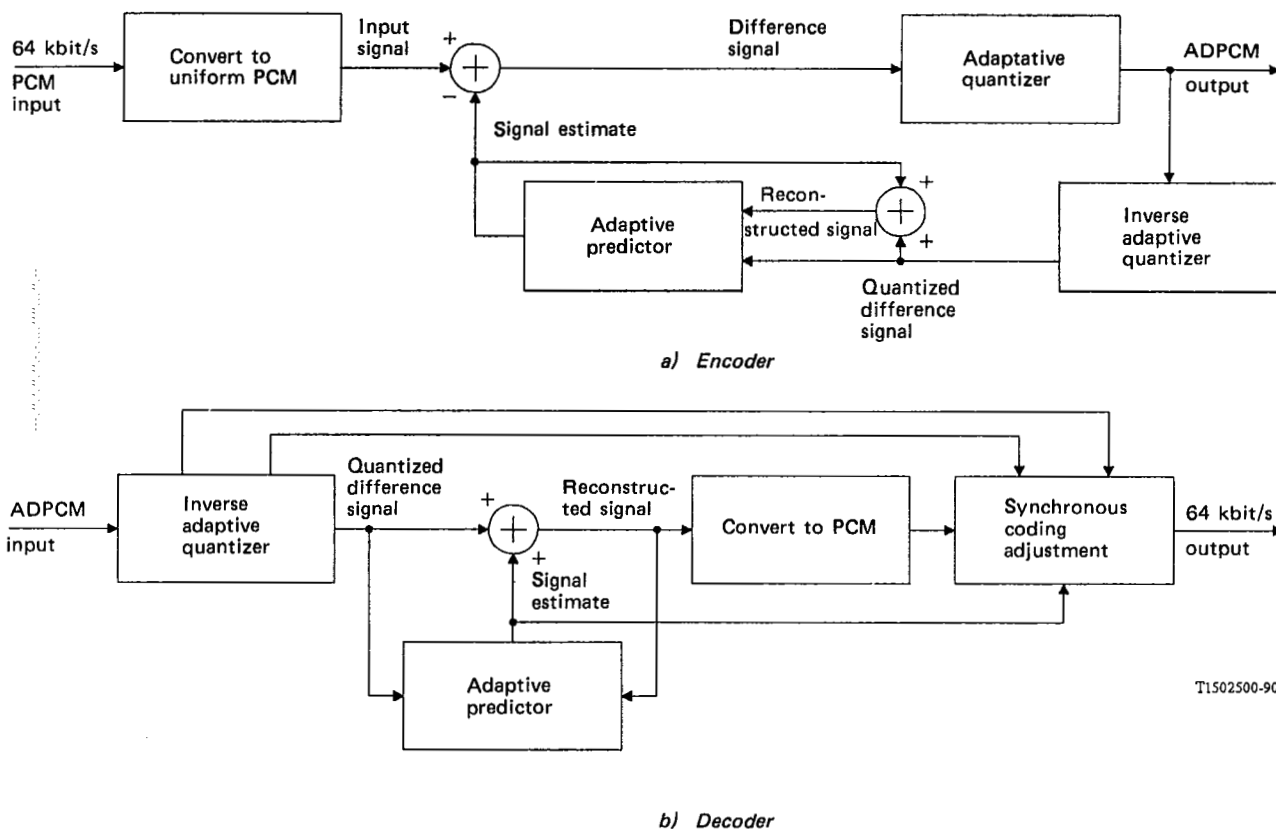


FIGURE 1/G.726
Simplified block diagrams

1.1 ADPCM encoder

Subsequent to the conversion of the A-law or μ -law PCM input signal to uniform PCM, a difference signal is obtained, by subtracting an estimate of the input signal from the input signal itself. An adaptive 31-, 15-, 7-, or 4-level quantizer is used to assign five, four, three or two binary digits, respectively, to the value of the difference signal for transmission to the decoder. An inverse quantizer produces a quantized difference signal from these same five, four, three or two binary digits, respectively. The signal estimate is added to this quantized difference signal to produce the reconstructed version of the input signal. Both the reconstructed signal and the quantized difference signal are operated upon by an adaptive predictor which produces the estimate of the input signal, thereby completing the feedback loop.

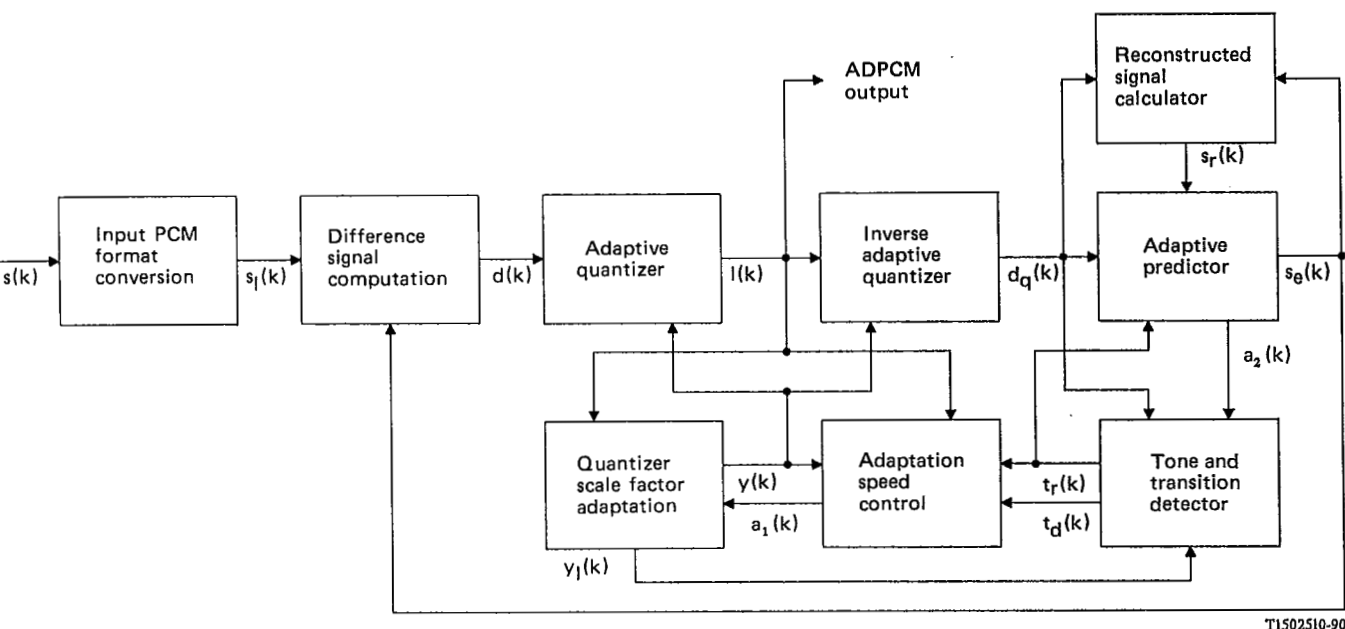
1.2 ADPCM decoder

The decoder includes a structure identical to the feedback portion of the encoder, together with a uniform PCM to A-law or μ -law conversion and a synchronous coding adjustment.

The synchronous coding adjustment prevents cumulative distortion occurring on synchronous tandem codings (ADPCM-PCM-ADPCM, etc., digital connections) under certain conditions (see § 3.7). The synchronous coding adjustment is achieved by adjusting the PCM output codes in a manner which attempts to eliminate quantizing distortion in the next ADPCM encoding stage.

2 ADPCM encoder principles

Figure 2/G.726 is a block schematic of the encoder. For each variable to be described, k is the sampling index and samples are taken at $125 \mu s$ intervals. A fundamental description of each block is given below in §§ 2.1 to 2.8.



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FIGURE 2/G.726
Encoder block schematic

2.1 Input PCM format conversion

This block converts the input signal $s(k)$ from A-law or μ -law PCM to a uniform PCM signal $s_l(k)$.

2.2 Difference signal computation

This block calculates the difference signal $d(k)$ from the uniform PCM signal $s_l(k)$ and the signal estimate $s_e(k)$:

$$d(k) = s_l(k) - s_e(k) \quad (2-1)$$

2.3 Adaptive quantizer

A 31-, 15-, 7- or 4-level non-uniform adaptive quantizer is used to quantize the difference signal $d(k)$ for operating at 40, 32, 24 or 16 kbit/s, respectively. Prior to quantization, $d(k)$ is converted to a base 2 logarithmic representation and scaled by $y(k)$ which is computed by the scale factor adaptation block. The normalized input/output characteristic (infinite precision values) of the quantizer is given in Tables 1/G.726 through 4/G.726.

2.3.1 Operation at 40 kbit/s

Five binary digits are used to specify the quantized level representing $d(k)$ (four for the magnitude and one for the sign). The 5-bit quantizer output $I(k)$ forms the 40 kbit/s output signal; $I(k)$ takes on one of 31 non-zero values, $I(k)$ is also fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks that operate on a 5-bit $I(k)$ having one of 32 possible values. $I(k) = 00000$ is a legitimate input to these blocks when used in the decoder, due to transmission errors.

TABLE 1/G.726
Quantizer normalized input/output characteristic
for 40 kbit/s operation

Normalized quantizer input range $\log_2 d(k) - y(k)$	$ I(k) $	Normalized quantizer output $\log_2 d_q(k) - y(k)$
$[4.31, +\infty)$	15	4.42
$[4.12, 4.31)$	14	4.21
$[3.91, 4.12)$	13	4.02
$[3.70, 3.91)$	12	3.81
$[3.47, 3.70)$	11	3.59
$[3.22, 3.47)$	10	3.35
$[2.95, 3.22)$	9	3.09
$[2.64, 2.95)$	8	2.80
$[2.32, 2.64)$	7	2.48
$[1.95, 2.32)$	6	2.14
$[1.54, 1.95)$	5	1.75
$[1.08, 1.54)$	4	1.32
$[0.52, 1.08)$	3	0.81
$[-0.13, 0.52)$	2	0.22
$[-0.96, -0.13)$	1	-0.52
$(-\infty, -0.96)$	0	$-\infty$

Note – In Tables 1/G.726 through 4/G.726, “[” indicates that the endpoint value is included in the range, and “(” or “)” indicates that the endpoint value is excluded from the range.

2.3.2 Operation at 32 kbit/s

Four binary digits are used to specify the quantized level representing $d(k)$ (three for the magnitude and one for the sign). The 4-bit quantizer output $I(k)$ forms the 32 kbit/s output signal; it is also fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks. $I(k) = 0000$ is a legitimate input to these blocks when used in the decoder, due to transmission errors.

TABLE 2/G.726

**Quantizer normalized input/output characteristic
for 32 kbit/s operation**

Normalized quantizer input range $\log_2 d(k) - y(k)$	$ I(k) $	Normalized quantizer output $\log_2 d_q(k) - y(k)$
$[3.12, +\infty)$	7	3.32
$[2.72, 3.12)$	6	2.91
$[2.34, 2.72)$	5	2.52
$[1.91, 2.34)$	4	2.13
$[1.38, 1.91)$	3	1.66
$[0.62, 1.38)$	2	1.05
$[-0.98, 0.62)$	1	0.031
$(-\infty, -0.98)$	0	$-\infty$

2.3.3 Operation at 24 kbit/s

Three binary digits are used to specify the quantized level representing $d(k)$ (two for the magnitude and one for the sign). The 3-bit quantizer output $I(k)$ forms the 24 kbit/s output signal, where $I(k)$ takes on one of seven non-zero values. $I(k)$ is also fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks, each of which is modified to operate on a 3-bit $I(k)$ having any of the eight possible values. $I(k) = 000$ is a legitimate input to these blocks when used in the decoder, due to transmission errors.

TABLE 3/G.726

**Quantizer normalized input/output characteristic
for 24 kbit/s operation**

Normalized quantizer input range $\log_2 d(k) - y(k)$	$ I(k) $	Normalized quantizer output $\log_2 d_q(k) - y(k)$
$[2.58, +\infty)$	3	2.91
$[1.70, 2.58)$	2	2.13
$[0.06, 1.70)$	1	1.05
$(-\infty, -0.06)$	0	$-\infty$

2.3.4 Operation at 16 kbit/s

Two binary digits are used to specify the quantized level representing $d(k)$ (one for the magnitude and one for the sign). The 2-bit quantizer output $I(k)$ forms the 16 kbit/s output signal; it is also fed to the inverse adaptive quantizer, the adaptation speed control and the quantizer scale factor adaptation blocks.

TABLE 4/G.726
Quantizer normalized input/output characteristic
for 16 kbit/s operation

Normalized quantizer input range $\log_2 d(k) - y(k)$	$ I(k) $	Normalized quantizer output $\log_2 d_q(k) - y(k)$
$[2.04, +\infty)$	1	2.85
$(-\infty, -2.04)$	0	0.91

Unlike the quantizers described in § 2.3.1 for operation at 40 kbit/s, in § 2.3.2 for operation at 32 kbit/s and in § 2.3.3 for operation at 24 kbit/s, the quantizer for operation at 16 kbit/s is an even-level (4-level) quantizer. The even-level quantizer for the 16 kbit/s ADPCM has been selected because of its superior performance over a corresponding odd-level (3-level) quantizer.

2.4 Inverse adaptive quantizer

A quantized version $d_q(k)$ of the difference signal is produced by scaling, using $y(k)$, specific values selected from the normalized quantizing characteristic given in Tables 1/G.726 through 4/G.726 and then transforming the result from the logarithmic domain.

2.5 Quantizer scale factor adaptation

This block computes $y(k)$, the scaling factor for the quantizer and the inverse quantizer. The inputs are the 5-bit, 4-bit, 3-bit, 2-bit quantizer output $I(k)$ and the adaptation speed control parameter $a_l(k)$.

The basic principle used in scaling the quantizer is bimodal adaptation:

- fast for signals (e.g. speech) that produce difference signals with large fluctuations;
- slow for signals (e.g. voiceband data, tones) that produce difference signals with small fluctuations.

The speed of adaptation is controlled by a combination of fast and slow scale factors.

The fast (unlocked) scale factor $y_u(k)$ is recursively computed in the base 2 logarithmic domain from the resultant logarithmic scale factor $y(k)$:

$$y_u(k) = (1 - 2^{-5}) y(k) + 2^{-5} W[I(k)], \tag{2-2}$$

where $y_u(k)$ is limited by $1.06 \leq y_u(k) \leq 10.00$.

For 40 kbit/s ADPCM, the discrete function $W(I)$ is defined as follows (infinite precision values):

$ I(k) $	15	14	13	12	11	10	9	8
$W[I(k)]$	43.50	33.06	27.50	22.38	17.50	13.69	11.19	8.81

$ I(k) $	7	6	5	4	3	2	1	0
$W[I(k)]$	6.25	3.63	2.56	2.50	2.44	1.50	0.88	0.88

For 32 kbit/s ADPCM, the discrete function $W(I)$ is defined as follows (infinite precision values):

$ I(k) $	7	6	5	4	3	2	1	0
$W[I(k)]$	70.13	22.19	12.38	7.00	4.00	2.56	1.13	-0.75

For 24 kbit/s ADPCM, the discrete function $W(I)$ is defined as follows (infinite precision values):

$ I(k) $	3	2	1	0
$W[I(k)]$	36.38	8.56	1.88	-0.25

For 16 kbit/s ADPCM, the discrete function $W(I)$ is defined as follows (infinite precision values):

$ I(k) $	1	0
$W[I(k)]$	27.44	-1.38

The factor $(1 - 2^{-5})$ introduces finite memory into the adaptive process so that the states of the encoder and decoder converge following transmission errors.

The slow (locked) scale factor $y_l(k)$ is derived from $y_u(k)$ with a low pass-filter operation:

$$y_l(k) = (1 - 2^{-6}) y_l(k - 1) + 2^{-6} y_u(k) \quad (2-3)$$

The fast and slow scale factors are then combined to form the resultant scale factor:

$$y(k) = a_l(k) y_u(k - 1) + [1 - a_l(k)] y_l(k - 1) \quad (2-4)$$

where $0 \leq a_l(k) \leq 1$ (see § 2.6).

2.6 Adaptation speed control

The controlling parameter $a_l(k)$ can assume values in the range $[0, 1]$. It tends towards unity for speech signals and towards zero for voiceband data signals. It is derived from a measure of the rate-of-change of the difference signal values.

Two measures of the average magnitude of $I(k)$ are computed:

$$d_{ms}(k) = (1 - 2^{-5}) d_{ms}(k - 1) + 2^{-5} F[I(k)] \tag{2-5}$$

and

$$d_{ml}(k) = (1 - 2^{-7}) d_{ml}(k - 1) + 2^{-7} F[I(k)] \tag{2-6}$$

For 40 kbit/s ADPCM, $F[I(k)]$ is defined by:

I(k)	15	14	13	12	11	10	9	8
F[I(k)]	6	6	5	4	3	2	1	1

I(k)	7	6	5	4	3	2	1	0
F[I(k)]	1	1	1	0	0	0	0	0

For 32 kbit/s ADPCM, $F[I(k)]$ is defined by:

I(k)	7	6	5	4	3	2	1	0
F[I(k)]	7	3	1	1	1	0	0	0

For 24 kbit/s ADPCM, $F[I(k)]$ is defined by:

I(k)	3	2	1	0
F[I(k)]	7	2	1	0

For 16 kbit/s ADPCM, $F[I(k)]$ is defined by:

$ I(k) $	1	0
$F[I(k)]$	7	0

Thus $d_{ms}(k)$ is a relatively short term average of $F[I(k)]$ and $d_{ml}(k)$ is a relatively long term average of $F[I(k)]$.

Using these two averages, the variable $a_p(k)$ is defined:

$$a_p(k) = \begin{cases} (1 - 2^{-4})a_p(k-1) + 2^{-3}, & \text{if } |d_{ms}(k) - d_{ml}(k)| \geq 2^{-3} d_{ml}(k) \\ (1 - 2^{-4})a_p(k-1) + 2^{-3}, & \text{if } y(k) < 3 \\ (1 - 2^{-4})a_p(k-1) + 2^{-3}, & \text{if } t_d(k) = 1 \\ 1, & \text{if } t_r(k) = 1 \\ (1 - 2^{-4})a_p(k-1), & \text{otherwise} \end{cases} \quad (2-7)$$

Thus, $a_p(k)$ tends towards the value 2 if the difference between $d_{ms}(k)$ and $d_{ml}(k)$ is large (average magnitude of $I(k)$ changing) and $a_p(k)$ tends towards the value 0 if the difference is small (average magnitude of $I(k)$ relatively constant). $a_p(k)$ also tends towards 2 for idle channel (indicated by $y(k) < 3$) or partial band signals (indicated by $t_d(k) = 1$ as described in § 2.8). Note that $a_p(k)$ is set to 1 upon detection of a partial band signal transition (indicated by $t_r(k) = 1$, see § 2.8).

$a_p(k-1)$ is then limited to yield $a_l(k)$ used in Equation (2-4) above:

$$a_l(k) = \begin{cases} 1, & a_p(k-1) > 1 \\ a_p(k-1), & a_p(k-1) \leq 1. \end{cases} \quad (2-8)$$

This asymmetrical limiting has the effect of delaying the start of a fast to slow state transition until the absolute value of $I(k)$ remains constant for some time. This tends to eliminate premature transitions for pulsed input signals such as switched carrier voiceband data.

2.7 Adaptive predictor and reconstructed signal calculator

The primary function of the adaptive predictor is to compute the signal estimate $s_e(k)$ from the quantized difference signal $d_q(k)$. Two adaptive predictor structures are used, a sixth order section that models zeros and a second order section that models poles in the input signal. This dual structure effectively caters for the variety of input signals which might be encountered.

The signal estimate is computed by:

$$s_e(k) = \sum_{i=1}^2 a_i(k-1) s_r(k-i) + s_{ez}(k), \quad (2-9)$$

where

$$s_{ez}(k) = \sum_{i=1}^6 b_i(k-1) d_q(k-i),$$

and the reconstructed signal is defined as

$$s_r(k-i) = s_e(k-i) + d_q(k-i).$$

Both sets of predictor coefficients are updated using a simplified gradient algorithm:

for the second order predictor:

$$a_1(k) = (1 - 2^{-8})a_1(k-1) + (3 \cdot 2^{-8}) \operatorname{sgn}[p(k)] \operatorname{sgn}[p(k-1)], \quad (2-10)$$

$$a_2(k) = (1 - 2^{-7})a_2(k-1) + 2^{-7} \{ \operatorname{sgn}[p(k)] \operatorname{sgn}[p(k-2)] - f[a_1(k-1)] \operatorname{sgn}[p(k)] \operatorname{sgn}[p(k-1)] \}, \quad (2-11)$$

where

$$p(k) = d_q(k) + s_{ez}(k),$$

$$f(a_1) = \begin{cases} 4a_1, & |a_1| \leq 2^{-1} \\ 2 \operatorname{sgn}(a_1), & |a_1| > 2^{-1}, \end{cases}$$

and $\operatorname{sgn}[0] = 1$, except $\operatorname{sgn}[p(k-i)]$ is defined to be 0 only if $p(k-i) = 0$ and $i = 0$;

with the stability constraints:

$$|a_2(k)| \leq 0.75 \text{ and } |a_1(k)| \leq 1 - 2^{-4} - a_2(k).$$

If $t_r(k) = 1$ (see § 2.8), then $a_1(k) = a_2(k) = 0$.

For the sixth order predictor:

$$b_i(k) = (1 - 2^{-8})b_i(k-1) + 2^{-7} \operatorname{sgn}[d_q(k)] \operatorname{sgn}[d_q(k-i)], \quad (2-12A)$$

for $i = 1, 2, \dots, 6$.

For 40 kbit/s coding, the adaptive predictor is changed to decrease the leak factor used for zeros coefficient operation. In this case, Equation 2.12A becomes:

$$b_i(k) = (1 - 2^{-9})b_i(k-1) + 2^{-7} \operatorname{sgn}[d_q(k)] \operatorname{sgn}[d_q(k-i)]. \quad (2-12B)$$

If $t_r(k) = 1$ (see § 2.8), then $b_1(k) = b_2(k) = \dots = b_6(k) = 0$.

As above, $\operatorname{sgn}[0] = 1$, except $\operatorname{sgn}[d_q(k-i)]$ is defined to be 0 only if $d_q(k-i) = 0$ and $i = 0$. Note that $b_i(k)$ is implicitly limited to ± 2 .

2.8 Tone and transition detector

In order to improve performance for signals originating from frequency shift keying (FSK) modems operating in the character mode, a two-step detection process is defined. First, partial band signal (e.g. tone) detection is invoked so that the quantizer can be driven into the fast mode of adaptation:

$$t_d(k) = \begin{cases} 1, & a_2(k) < -0.71875 \\ 0, & \text{otherwise} \end{cases} \quad (2-13)$$

In addition, a transition from a partial band signal is defined so that the predictor coefficients can be set to zero and the quantizer can be forced into the fast mode of adaptation:

$$t_r(k) = \begin{cases} 1, & a_2(k) < -0.71875 \text{ and } |d_q(k)| > 24 \cdot 2^{y_l(k)} \\ 0, & \text{otherwise} \end{cases} \quad (2-14)$$

3 ADPCM decoder principles

Figure 3/G.726 is a block schematic of the decoder. A functional description of each block is given in §§ 3.1 to 3.7 below.

3.1 Inverse adaptive quantizer

The function of this block is described in § 2.4.

3.2 Quantizer scale factor adaptation

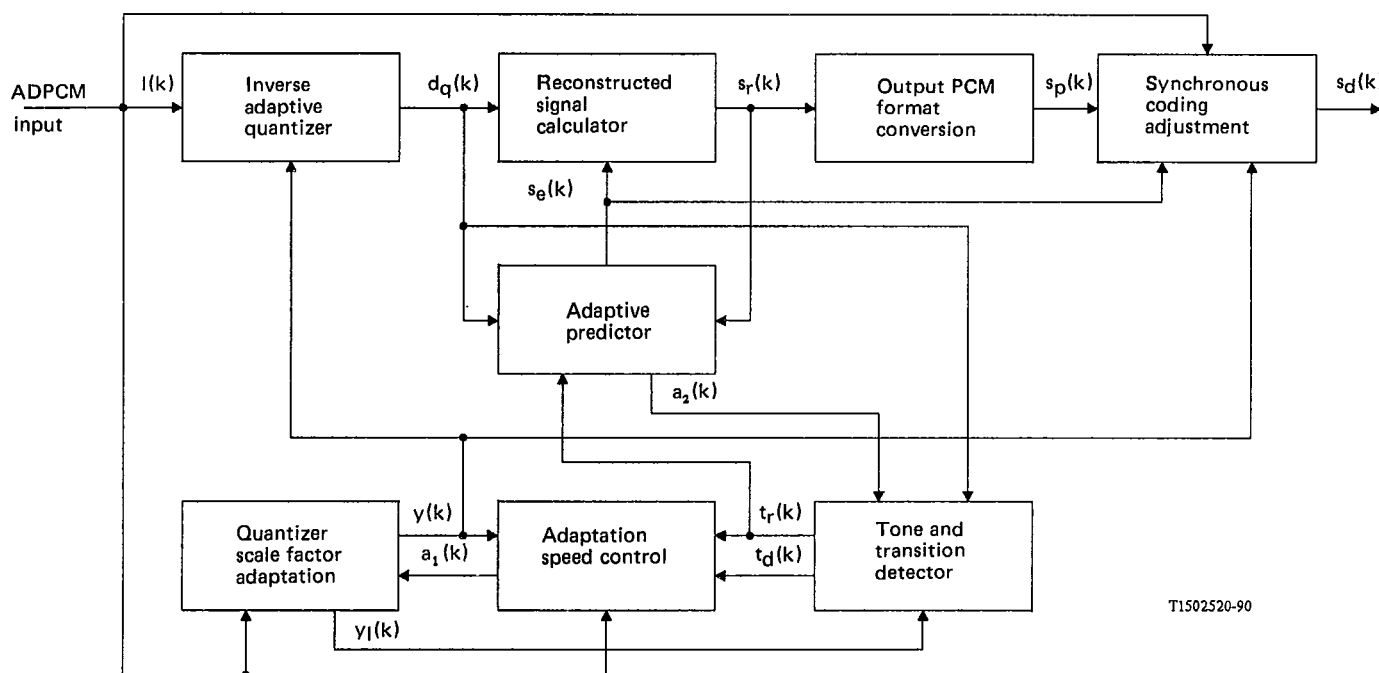
The function of this block is described in § 2.5.

3.3 Adaptation speed control

The function of this block is described in § 2.6.

3.4 Adaptive predictor and reconstructed signal calculator

The functions of this block are described in § 2.7.



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FIGURE 3/G.726
Decoder block schematic

3.5 Tone and transition detector

The function of this block is described in § 2.8.

3.6 Output PCM format conversion

This block converts the reconstructed uniform PCM signal $s_r(k)$ into an A-law or μ -law PCM signal $s_p(k)$ as required.

3.7 Synchronous coding adjustment

The synchronous coding adjustment prevents cumulative distortion occurring on synchronous tandem codings (ADPCM-PCM-ADPCM, etc. digital connections), when:

- the transmission of the ADPCM and the intermediate 64 kbit/s PCM signals is error free, and,
- the ADPCM and intermediate 64 kbit/s PCM bit streams are not disturbed by digital signal processing devices.

If the coder and decoder have different initial conditions, as may occur after switching for example, then the synchronous tandeming may take time to establish. Furthermore, if this property is disturbed or not acquired initially then it may be recovered for those signals of sufficient level with spectra that occupy the majority of the 200 to 3400 Hz band (e.g. speech, 4800 bit/s voiceband data).

When a decoder is synchronously connected to an encoder, the synchronous coding adjustment block estimates quantization in the encoder. If all state variables in both the decoder and the encoder have identical values and there are no transmission errors, the forced equivalence of both 4-bit quantizer output sequences for all values of k guarantees the property of non-accumulation of distortion.

This is accomplished by first converting the A-law or μ -law signal $s_p(k)$ to a uniform PCM signal $s_{lx}(k)$ and then computing a difference signal $d_x(k)$:

$$d_x(k) = s_{lx}(k) - s_e(k). \quad (3-1)$$

The difference signal $d_x(k)$ is then compared to the ADPCM quantizer decision interval determined by $I(k)$ and $y(k)$. The signal $s_d(k)$ is then defined as follows:

$$s_d(k) = \begin{cases} s_p^+(k), & d_x(k) < \text{lower interval boundary} \\ s_p^-(k), & d_x(k) \geq \text{upper interval boundary} \\ s_p(k), & \text{otherwise} \end{cases} \quad (3-2)$$

where

$s_d(k)$ is the output PCM code word of the decoder,

$s_p^+(k)$ is the PCM code word that represents the next more positive PCM output level (when $s_p(k)$ represents the most positive output level, then $s_p^+(k)$ is constrained to be the value $s_p(k)$),

$s_p^-(k)$ is the PCM code word that represents the next more negative PCM output level (when $s_p(k)$ represents the most negative output level, then $s_p^-(k)$ is constrained to be the value $s_p(k)$).

4 Computational details

Sections 4.1 and 4.2 provide the computational details for each of the encoder and decoder elements.

Proper timing for the encoder and decoder is obtained by executing all of the delay blocks simultaneously and proceeding to calculate the signals which can be derived using this information. For example, SE signal of Figure 9/G.726 is calculated using delay values and then SE signal is used as shown in Figure 4/G.726.

Implementations of the algorithm may be confirmed with a reasonable level of confidence by using the digital test sequences described in Appendix II to this Recommendation. The sequences are given in terms of encoder PCM input words, ADPCM words and decoder PCM output words.

4.1 Input and output signals

Table 2/G.726 defines the input and output signals for the encoder and decoder.

An optional signal R represents a reset function that sets all internal memory elements to a specified condition so that an encoder or decoder can be forced into a known state, for applications which require an immediate reset function (e.g. digital circuit multiplication equipment, in which case the reset is mandatory, not optional).

TABLE 5/G.726
Input and output signals

ENCODER			
	Name	Number of bits	Description
Input	S	8	PCM input word
Input	LAW	1	PCM law select, 0 = μ -law, 1 = A-law
Input	R (<i>optional</i>)	1	Reset
Output	I	5	40 kbit/s ADPCM word
Output	I	4	32 kbit/s ADPCM word
Output	I	3	24 kbit/s ADPCM word
Output	I	2	16 kbit/s ADPCM word
DECODER			
	Name	Number of bits	Description
Input	I	5	40 kbit/s ADPCM word
Input	I	4	32 kbit/s ADPCM word
Input	I	3	24 kbit/s ADPCM word
Input	I	2	16 kbit/s ADPCM word
Input	LAW	1	PCM law select, 0 = μ -law, 1 = A-law
Input	R (<i>optional</i>)	1	Reset
Output	SD	8	Decoder PCM output word

4.2 Description of variables and detailed specification of sub-blocks

This section contains a detailed expansion of all blocks in Figures 2/G.726 and 3/G.726 described in §§ 2 and 3. The expansions are illustrated in Figures 4/G.726 to 11/G.726 with the internal processing variables as defined in Table 6/G.726. A brief functional description and full specification is given for each sub-block.

The notations used in the sub-block descriptions are as follows:

- $\ll n$ denotes an n -bit shift left operation (zero fill),
- $\gg n$ denotes an n -bit shift right operation (in the direction of the least significant bit and zero fill),
- $\&$ denotes the logical “and” operation,
- $+$ denotes arithmetic addition,
- $-$ denotes arithmetic subtraction,
- $*$ denotes arithmetic multiplication,
- $**$ denotes the logical “exclusive or” operation,
- $|$ delineates comments to equations.

TABLE 6/G.726

Internal processing variables

Name	Bits	Binary representation	Optional reset values	Description
A1 ^a , A2 ^a	16 TC	S, 0,..., -14	0	Delayed predictor second order coefficients
A1P, A2P	16 TC	S, 0,..., -14		Second order predictor coefficients
A1R, A2R	16 TC	S, 0,..., -14		Triggered second order predictor coefficients
A1T	16 TC	S, 0,..., -14		Unlimited a_1 coefficient
A2T	16 TC	S, 0,..., -14		Unlimited a_2 coefficient
AL	7 SM	0,..., -6		Limited speed control parameter
AP ^a	10 SM	1,..., -8	0	Delayed unlimited speed control parameter
APP	10 SM	1,..., -8		Unlimited speed control parameter
APR	10 SM	1,..., -8		Triggered unlimited speed control parameter
AX	1 SM	1		Speed control parameter update
B1 ^a ,..., B6 ^a	16 TC	S, 0,..., -14	0	Delayed sixth order predictor coefficients
B1P, ..., B6P	16 TC	S, 0,..., -14		Sixth order predictor coefficients
B1R, ..., B6R	16 TC	S, 0,..., -14		Triggered sixth order predictor coefficients
D	16 TC	S, 14,..., 0		Difference signal, only in encoder
DL	11 SM	3,..., -7		Log_2 (difference signal), only in encoder
DLN	12 TC	S, 3,..., -7		Log_2 (normalized difference), only in encoder
DLNX	12 TC	S, 3,..., -7		Log_2 (normalized difference), only in decoder
DLX	11 SM	3,..., -7		Log_2 (difference signal), only in decoder
DML ^a	14 SM	2,..., -11	0	Delayed long term average of F(I) sequence
DMLP	14 SM	2,..., -11		Long term average of F(I) sequence
DMS ^a	12 SM	2,..., -9	0	Delayed short term average of F(I) sequence
DMSP	12 SM	2,..., -9		Short term average of F(I) sequence
DQ ^b	15 SM	S, 13,..., 0		Quantized difference signal (16, 24 or 32 kbit/s operation)
DQ ^b	16 SM	S, 14,..., 0		Quantized difference signal (16, 24, 32 or 40 kbit/s operation)
DQ0	11 FL	S, 4e, 6m		Quantized difference signal with delay 0
DQ1 ^a , ..., DQ6 ^a	11 FL	S, 4e, 6m	32	Quantized difference signal with delays 1 to 6
DQL	12 TC	S, 3,..., -7		Log_2 (quantized difference signal)

a) Indicates variables that are set to specific values by the optional reset. When reset is invoked, the output of the DELAY sub-block (see § 4.2.4) is given in column 4.

b) For 40 kbit/s ADPCM, DQ must be implemented as a 16 bit signed magnitude. For 16, 24 and 32 kbit/s, DQ may be implemented as a 15 or 16 bit signed magnitude.

TC denotes two's complement e denotes exponent bits
 SM denotes signed magnitude m denotes mantissa bits
 FL denotes floating point S denotes sign bit