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G.726

Appendix II
Test Vectors
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**SERIES G: TRANSMISSION SYSTEMS AND MEDIA,
DIGITAL SYSTEMS AND NETWORKS**

**Digital transmission systems – Terminal equipments –
Coding of analogue signals by methods other than PCM**

**Description of the digital test sequences
for the verification of the G.726
40, 32, 24 and 16 kbit/s ADPCM algorithm**

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DESCRIPTION OF THE DIGITAL TEST SEQUENCES FOR THE VERIFICATION OF THE G.726 40, 32, 24 AND 16 KBIT/S ADPCM ALGORITHM

1 Introduction

This guide describes the test sequences (vectors) for the ADPCM algorithms of Recommendation G.726 at the four fixed bit rates (16 kbit/s, 24 kbit/s, 32 kbit/s, 40 kbit/s) for both A-law and μ -law. It reproduces mainly the text of the CCITT collective letter No. 11/XV, dated 21/03/1991, the only amendments corresponding to the grouping on two 3½" disks of the files which were previously on four 5¼" disks.

The tests are arranged in two separate diskettes, one for the μ -law and one for the A-law. For each law, the diskette contains the reset test vectors and the homing test vectors. The diskettes are of the 3½ MS-DOS format¹. Within each diskette, the files are distributed in subdirectories that correspond to individual bit rates for the homing and reset case. A READ.ME file lists the contents of each diskette.

2 General description

The verification testing procedure consists in applying an input sequence to an ADPCM implementation and verifying that the output sequence is the same sequence in the output file for the same test conditions (PCM coding law, type of input, initial state of the implementation).

There are three types of input sequences. The first type consists of various sinusoidal PCM inputs that are representative of the signals expected in normal operation. These are called "normal inputs". A second group of input sequences is the set of "overload inputs" that contain PCM signals of very large amplitudes. The third group is the set of ADPCM sequences that can exercise the algorithm in a manner that is not possible with any PCM input sequence. They test the arithmetic and algorithmic performance of the ADPCM decoder by driving it to states that are unreachable by PCM signals under normal conditions. For example, these states may result from errors on the transmission line. These intermediate sequences will be denoted as "I-inputs".

The values (or samples) contained in a test file are given in ASCII hexadecimal representation with two hexadecimal characters per 8-bit value. In files with 5-bit ADPCM values, the three most significant bits are set to 0. Files containing 4-bit ADPCM values have the four most significant bits of each value set to 0. Files that contain 3-bit ADPCM values have the five most significant bits of each word set to 0. For files containing 2-bit ADPCM values, the six most significant bits are set to 0. All PCM A-law inputs are in the format specified by Table 1a/G.711, i.e. the even bits are inverted.

Each line in any file contains up to 32 values (or 64 characters) and ends with a line feed character. Two more hexadecimal characters representing the result of a checksum computation over the entire file are appended to each file. This checksum is the remainder of the division of 255 of the sum of all sample values (two hexadecimal characters comprise a sample value) in the file.

¹ It has been noted that these diskettes do not always copy correctly using DISKCOPY due to the interaction of DISKCOPY with certain character sequences found in the test sequences. Either files should be copied individually using COPY, or XCOPY should be used instead of DISKCOPY.

3 Test configurations

Test sequences are derived for the two configurations shown in Figures 1 and 2, respectively. The configuration of Figure 1 is the arrangement with the encoder transmitting to the decoder for error-free operation. The configuration of Figure 2 allows for input ADPCM words that would not normally emanate from an encoder and a PCM input word. The word formats of the various sequences are detailed in Table 1.

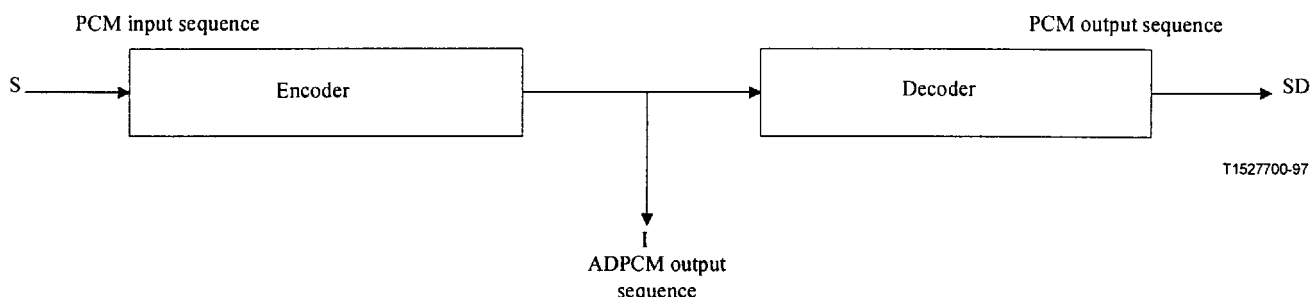


Figure 1 – Encoder and decoder configuration

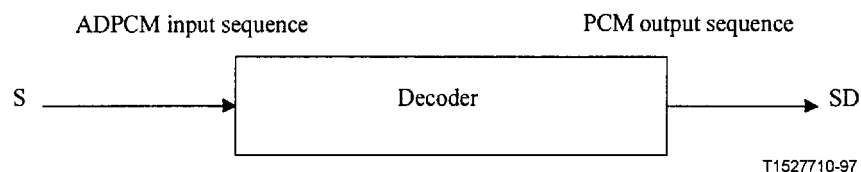


Figure 2 – Decoder only configuration

Table 1 – Word format of test sequences

Name	Description	Word format
S	PCM input word	Identical to that of SP described in the sub-block COMPRESS of the synchronous coding adjuster (4.2.8/G.726).
I	ADPCM word	As specified in the sub-block RECONST of the inverse adaptive quantizer (4.2.3/G.726).
SD	PCM output word	Identical to that of SP described in the sub-block COMPRESS (4.2.8/G.726).

4 Test combinations

The initial state of the implementation may be either the reset state of the algorithm defined in Table 2 or a well-defined initial state that follows the application of an initialization (or homing) sequence. Accordingly, there are two types of test sequences, reset sequences and homing sequences.

Table 2 – State values at reset

Variable	Value
A_1, A_2	0
$B_1, \dots, B_6$	0
$DQ_1, \dots, DQ_6$	32
PK_1, PK_2	0
SR_1, SR_2	32
TD	0
YL	34 816
YU	544

The homing sequences are based on the initial states that follow the application of an initialization (homing) sequence. These initialization sequences are described in further detail in 6.4.

For each initial state, both PCM laws (A-law and μ -law) are considered. To allow for the interoperation of both PCM laws, four possible input/output combinations must be considered as shown in Table 3.

Table 3 – Input/output combinations

Input	Output
A-law	A-law
μ -law	μ -law
A-law	μ -law
μ -law	A-law

5 Test organization

Tables 4 to 7 contain the names of files containing various reset/homing sequences for the following cases:

- 1) μ -law;
- 2) A-law;
- 3) $\mu \rightarrow A$; and
- 4) $A \rightarrow \mu$.

Files whose names start with an "R" contain reset sequences while the names of files for the homing sequences start with an "H". The suffix ".I" is reserved for the intermediate ADPCM encoder response to a PCM input. Files with the suffix ".O" are the output PCM files.