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Appendix I
Test vectors
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SERIES G: TRANSMISSION SYSTEMS AND MEDIA,
DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Terminal equipments –
Coding of analogue signals by methods other than PCM

**Description of the digital test sequences
for the verification of
the G.727 5-, 4-, 3- and 2-bit/sample
embedded ADPCM algorithm**

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DESCRIPTION OF THE DIGITAL TEST SEQUENCES FOR THE VERIFICATION OF THE G.727 5-, 4-, 3- AND 2-BIT/SAMPLE EMBEDDED ADPCM ALGORITHM

1 Introduction

This technical report describes the test sequences (vectors) for the embedded ADPCM algorithms of Recommendation G.727.

The test sequences are arranged in six separate diskettes, three for the μ -law and three for the A-law:

- 1) Diskettes 1 and 2 contain the reset and the homing test sequences for the embedded ADPCM algorithms (5,2), (5,3) and (5,4) for both the μ -law and A-law respectively.
- 2) Diskettes 3 and 4 contain the reset and the homing test sequences for the embedded ADPCM algorithms (4,2), (4,3) and (4,4) for both the μ -law and A-law respectively.
- 3) Diskettes 5 and 6 contain the reset and the homing test sequences for the embedded ADPCM algorithms (2,2), (3,2) and (3,3) for both the μ -law and A-law respectively.

The diskettes are of the 3½" MS-DOS format¹. A READ.ME file lists the contents of each diskette.

2 General description

The verification testing procedure consists in applying an input sequence to an embedded ADPCM implementation and verifying that the output sequence is the same sequence in the output file for the same test conditions (PCM coding law, type of input, initial state of the implementation).

There are three types of input sequences. The first type consists of various sinusoidal PCM inputs that are representative of the signals expected in normal operation. These are called "normal inputs". A second group of input sequences is the set of "overload inputs" that contain PCM signals of very large amplitudes. The third group is the set of ADPCM sequences that can exercise the algorithm in a manner that is not possible with any PCM input sequence. They test the arithmetic and algorithmic performance of the ADPCM decoder by driving it to states that are unreachable by PCM signals under normal conditions. For example, these states may result from errors on the transmission line. These intermediate sequences will be denoted as "I-inputs".

The values (or samples) contained in a test file are given in ASCII hexadecimal representation with two hexadecimal characters per 8-bit value. In files with 5-bit ADPCM values, the three most significant bits are set to 0. Files containing 4-bit ADPCM values have the four most significant bit of each value set to 0. Files that contain 3-bit ADPCM values have the five most significant bits of each word set to 0. For files containing 2-bit ADPCM values, the six most significant bits are set to 0. All PCM A-law inputs are in the format specified by Table 1a/G.711, i.e. the even bits are inverted.

Each line in any file contains up to 32 values (or 64 characters) and ends with a line feed character. Two more hexadecimal characters representing the result of a checksum computation over the entire file are appended to each file. This checksum is the remainder of the division of 255 of the sum of all sample values (two hexadecimal characters comprise a sample value) in the file.

¹ It has been noted that these diskettes do not always copy correctly using DISKCOPY due to the interaction of DISKCOPY with certain character sequences found in the test sequences. Either files should be copied individually using COPY, or XCOPY should be used instead of DISKCOPY.

3 Test configurations

Test sequences are derived for the two configurations shown in Figures 1 and 2, respectively. The configuration of Figure 1 is the arrangement with the encoder transmitting to the decoder for error-free operation. The configuration of Figure 2 allows for input ADPCM words that would not normally emanate from an encoder and a PCM input word. The word formats of the various sequences are detailed in Table 1.

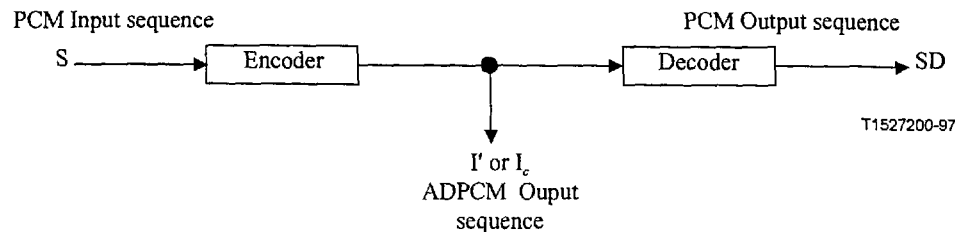


Figure 1 – Encoder and decoder configuration

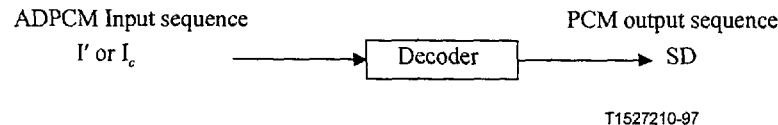


Figure 2 – Decoder only configuration

Table 1 – Word format of test sequences

Name	Description	Word format
S	PCM input word	Identical to that of SP described in the sub-block COMPRESS of the synchronous coding adjuster (6.2.10/G.727)
I, I _c	ADPCM word	As specified in the sub-block RECONST of the inverse adaptive quantizer (6.2.4/G.727)
SD	PCM output word	Identical to that of SP described in the sub-block COMPRESS (6.2.10/G.727)

4 Test combinations

The initial state of the implementation may be either the reset state of the algorithm defined in Table 2 or a well-defined initial state that follows the application of an initialization (or homing) sequence. Accordingly, there are two types of test sequences, reset sequences and homing sequences.

Table 2 – State values at reset

Variable	Value
A_1, A_2	0
$B_1, \dots, B_6$	0
$DQ_1, \dots, DQ_6$	32
PK_1, PK_2	0
SR_1, SR_2	32
TD	0
YL	34 816
YU	544

The homing sequences are based on the initial states that follow the application of an initialization (homing) sequence. These initialization sequences are described in further detail in 6.4.

For each initial state, both PCM laws (A-law and μ -law) are considered. To allow for the interoperation of both PCM laws, four possible input/output combinations must be considered as shown in Table 3.

Table 3 – Input/output combinations

Input	Output
A-law	A-law
μ -law	μ -law
A-law	μ -law
μ -law	A-law

5 Test organization

Tables 4-7 contain the names of files containing various reset/homing sequences for the following cases:

- 1) μ -law;
- 2) A-law;
- 3) $\mu \rightarrow A$; and
- 4) $A \rightarrow \mu$.

Files whose names start with an "R" contain reset sequences while the names of files for the homing sequences start with an "H". The suffix ".I" is reserved for the intermediate ADPCM encoder response to a PCM input. Files with the suffix ".O" are the output PCM files.

Table 4 – Reset and homing sequences for μ -law

Algorithm	Normal			I-input		Overload		
	Input (PCM)	Intermediate (ADPCM)	Output (PCM)	Input (ADPCM)	Output (PCM)	Input (PCM)	Intermediate (ADPCM)	Output (PCM)
5,2	NRM.M	RN52_M.I HN52_M.I	RN52_M.O HN52_M.O	I40	RI52_M.O HI52_M.O	OVR.M	RV52_M.I HV52_M.I	RV52_M.O HV52_M.O
4,2	NRM.M	RN42_M.I HN42_M.I	RN42_M.O HN42_M.O	I32	RI42_M.O HI42_M.O	OVR.M	RV42_M.I HV42_M.I	RV42_M.O HV42_M.O
3,2	NRM.M	RN32_M.I HN32_M.I	RN32_M.O HN32_M.O	I24	RI32_M.O HI32_M.O	OVR.M	RV32_M.I HV32_M.I	RV32_M.O HV32_M.O
2,2	NRM.M	RN22_M.I HN22_M.I	RN22_M.O HN22_M.O	I16	RI22_M.O HI22_M.O	OVR.M	RV22_M.I HV22_M.I	RV22_M.O HV22_M.O
5,3	NRM.M	RN53_M.I HN53_M.I	RN53_M.O HN53_M.O	I40	RI53_M.O HI53_M.O	OVR.M	RV53_M.I HV53_M.I	RV53_M.O HV53_M.O
4,3	NRM.M	RN43_M.I HN43_M.I	RN43_M.O HN43_M.O	I32	RI43_M.O HI43_M.O	OVR.M	RV43_M.I HV43_M.I	RV43_M.O HV43_M.O
3,3	NRM.M	RN33_M.I HN33_M.I	RN33_M.O HN33_M.O	I24	RI33_M.O HI33_M.O	OVR.M	RV33_M.I HV33_M.I	RV33_M.O HV33_M.O
5,4	NRM.M	RN54_M.I HN54_M.I	RN54_M.O HN54_M.O	I40	RI54_M.O HI54_M.O	OVR.M	RV54_M.I HV54_M.I	RV54_M.O HV54_M.O
4,4	NRM.M	RN44_M.I HN44_M.I	RN44_M.O HN44_M.O	I32	RI44_M.O HI44_M.O	OVR.M	RV44_M.I HV44_M.I	RV44_M.O HV44_M.O