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CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

O.152

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SPECIFICATIONS OF MEASURING EQUIPMENT

ERROR PERFORMANCE MEASURING EQUIPMENT FOR BIT RATES OF 64 kbit/s AND $N \times 64$ kbit/s



Recommendation O.152

FOREWORD

The CCITT (the International Telegraph and Telephone Consultative Committee) is a permanent organ of the International Telecommunication Union (ITU). CCITT is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

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Recommendation O.152 was revised by Study Group IV and was approved under the Resolution No. 2 procedure on the 5th of October 1992.

CCITT NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized private operating agency.

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Recommendation O.152

**ERROR PERFORMANCE MEASURING EQUIPMENT
FOR BIT RATES OF 64 kbit/s AND $N \times 64$ kbit/s**

(Published 1984; revised 1988, 1992)

Abstract

Defines the requirements for an equipment to measure bit-error performance at 64 kbit/s and $N \times 64$ kbit/s.

Keywords

- digital error detector;
- digital pattern generator;
- error performance measurement;
- measurement;
- tester.

PREAMBLE

The requirements for the characteristics of a bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipment produced by different manufacturers.

1 General

The equipment is designed to measure the bit-error performance of digital paths (operating at 64 kbit/s and $N \times 64$ kbit/s) by the direct comparison of a pseudo-random test pattern with locally generated test pattern identical to the transmitted test pattern.

2 Test patterns

The following patterns are recommended (see Recommendation O.150 [8], for further details).

2.1 Pseudo-random pattern of $2^{11} - 1$ (2047 bit) pattern length

This pattern is primarily intended for error and jitter measurements on circuits operating at bit rates of 64 kbit/s and $N \times 64$ kbit/s.

The pattern may be generated in an eleven-stage shift register whose 9th and 11th stage outputs are added in a modulo-two addition stage, and the result is fed back to the input of the first stage.

Number of shift register stages	11
Length of pseudo-random sequence	$2^{11} - 1 = 2047$ bits
Longest sequence of ZEROs	10 (non-inverted signal)

Note 1 – In the case of international testing where the measurement includes systems based on 1544 kbit/s, it is necessary to modify the test sequence in such a way that more than seven consecutive ZEROs are avoided. This is achieved by forcing the output bit to ONE whenever the previous 7 bits of the sequence are all ZEROs.

Note 2 – It is recommended to use the test pattern of 2047 bit length also at other bit rates in the range of 48 kbit/s to 168 kbit/s.