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SERIES G: DIGITAL NETWORKS, DIGITAL SECTIONS AND DIGITAL LINE SYSTEMS

Guidelines concerning the measurement of wander

ITU-T G-series Recommendations – Supplement 35

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NOTES

1 Supplement 35 to the G-series Recommendations was approved in Melbourne (1988) and published in Fascicle III.5 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Supplement, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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3.3 *Conclusion*

The temperature in the underground housing depends on site climate, type of soil, depth, time of the year, equipment dissipation.

A mathematical analysis of the heat transmission makes it possible to evaluate the maximum temperature in the housing taking into account the effect of the parameters involved.

The use of selected backfilling material can be considered and the resulting effect evaluated.

HOUSING TYPE : CAI/24

Temperature at steady state (° C)

Housing dimensions (m) ∅ 0.85 h 0.9

Dissipated power (watt)	100
Month	8
Mean temperature of the site (° C)	12.7
Amplitude of the thermal variation (° C)	11.7
Thermal conductivity of the soil (W m^{-1} K^{-1})	0.44
Density of the soil (kg · m^{-3})	1550
Specific heat of the soil (J kg^{-1} K^{-1})	1255
Thermal conductivity of the backfilling material (W m^{-1} K^{-1})	0.8
Depth of the backfilling material (m)	0.4
External radius of the backfilling material (m)	1.2

Reference

[1] JEN-HU-CHANG: Ground Temperature, *Blue Hill Meteorological Observatory, Harward University*, Vol. I, II – Hilton 86, Massachusetts, 1958.

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Supplement No. 35

GUIDELINES CONCERNING THE MEASUREMENT OF WANDER

(Contribution from United States of America, referred to in Recommendations G.812 and G.824)

Wander measurement methodology

The purpose of this Supplement is to present one suitable method of verification of timing accuracy of clocks. Guidelines concerning the measurement of jitter are contained in Supplement No. 38 of the O-Series.

1 Output wander measurement

1.1 *Slave clock*

The measurement strategy is to be able to derive the values of the model parameters contained in the Annex to Recommendation G.812 for the slave clock under test.

Once these parameter values have been obtained compliance with the specifications contained in Recommendation G.812 may be verified.

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To adequately characterize the performance of e clock a series of tests must be performed. In general, the test fall into the three categories of operatio

1) ideal operation;

2) stressed operation;

3) holdover operation.

1.1.1 *Test configuration*

The objective of the test procedure is to be able nate the parameters in the clock model described above for a given clock under test. The architecture for a clock testing arrangement is shown in Figure 1. The components and their interconnection are described next.

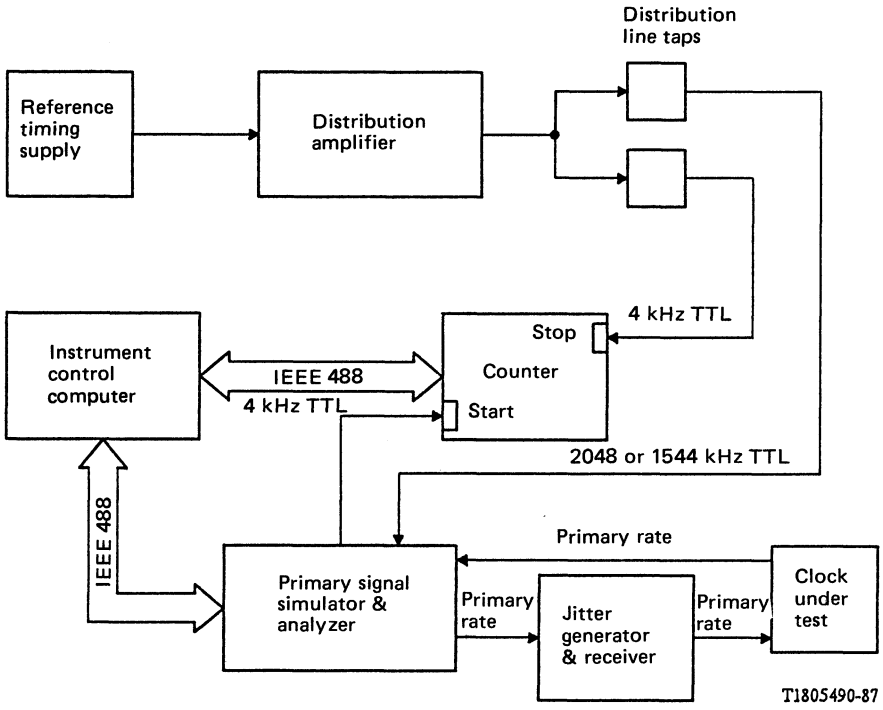

FIGURE 1

Test configuration

1.1.1.1 *Reference clock*

The test configuration is designed to provide the clock under test with a primary rate digital reference timed from a stable reference oscillator. In clock testing, it is the relative phase-time compared to the reference input that is critical[1]. Thus, the absolute accuracy of the reference input is not critical. What is important is that short-term instability of the reference oscillator be small to ensure low measurement noise and a low background tracking error in the control loop of the clock being tested.

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[1] In holdover testing, the longer term stability and drift of the reference oscillator is important.

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1.1.1.2 *Digital reference simulation*

The testing arrangement is designed to provide a primary rate digital reference with impairment to the clock to allow for stress testing of the clock. To accomplish this a primary rate digital signal simulator and analyzer is employed that has the capability to be externally synchronized. For the 1544 kHz primary rate digital signal[2] a 1544 kHz timing signal is supplied to the simulator/analyzer to control outgoing transmit timing. The 1544 kHz signal is produced via a distribution amplifier and synthesizer line tap. This distribution arrangement allows one to develop multiple taps of timing signals synthesized from the 10 MHz input from the reference oscillator. Each line tap is a dedicated synthesizer producing the timing signal required. The jitter produced from these synthesizers should be less than 1000 ps rms.

The primary rate impairment simulator is programmed via an IEEE 488 control bus to produce the desired interruption events to stress the clock. The primary rate digital signal is next bridged through a jitter generator and receiver. The jitter generator is used to insert background jitter to the digital signal. It is important to simulate a realistic level of background jitter for several reasons. Primarily, when interruptions occur the background jitter can be a major source of phase build-out error as the synchronization unit attempts to bridge the interruption. Secondly, the jitter transfer characteristics of the clock can be evaluated.

The jitter generation unit is provided an external jitter modulation input. The jitter signal used is bandlimited white noise. A signal from a white noise source is filtered using a low pass single pole filter with 150 Hz 3 dB cutoff. The main reason for lowpass filtering the jitter is to avoid producing bit errors from high frequency alignment jitter. The jitter power should be set to reflect realistic jitter levels in the network. It is important that sinusoidal jitter be avoided as a test jitter input, as certain phase detection techniques are very insensitive to sinusoidal jitter.

1.1.1.3 *Output timing signal recovery*

To test a clock, reference input is provided from the output of the jitter generator. To recover the output timing signal from the clock, an outgoing primary rate signal is selected from the unit controlled by the clock under test. This digital signal is connected to the receive portion of the Primary Rate Signal Simulator and Analyzer. In this unit the receiver timing function is decoupled from the transmit timing used in the generator. The receiver extracts a 4 kHz frame timing signal from the input signal and provides this timing signal at an external port. This 4 kHz timing signal is phase coherent with the outgoing timing from the clock under test.

1.1.1.4 *Phase-time data collection*

A counter is used to observe the relative phase-time error of the output 4 kHz timing signal compared to a reference 4 kHz timing signal. The reference 4 kHz timing signal is derived from the distribution amplifier and synthesizer units. The synthesizer jitter in generating the 4 kHz reference signal is less than 1000 ps. By performing the phase comparison at 4 kHz the observation range of phase variation is 250 µs. If care is given to start a test near the centre of this range, there should not be a problem associated with cycle slipping for all tests except holdover testing. However, even this range can be extended by resolving cycle slips in the data collection software.

In reality, the measurement resolution is limited by the intrinsic jitter in the counter as well as trigger error. Experience has shown that the measurement resolution jitter can be maintained below 100 ps rms with reasonable care given to cabling and trigger levels. More importantly, the overall background jitter noise level can be checked prior to testing to ensure proper performance. For the components used in the particular system described, overall jitter levels of 1000 ps rms are typically attainable. This is more than adequate for measuring the levels of phase stability expected from clocks.

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[2] The following discussion is applicable in an analogous manner to the 2048 kHz primary rate digital signal.

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