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Supplement 11 to ITU-T K-series Recommendations

ITU-T K.131 – Soft error measures of field programmable gate arrays

Summary

Supplement 11 to ITU-T K-series of Recommendations describes soft error mitigation for field programmable gate arrays (FPGAs). FPGAs are a mainstream component of recent large-scale integrated circuits (LSIs), and many FPGAs are used as the main component in equipment for communication. First, this Supplement describes trends of soft error rates corresponding with the miniaturization of manufacturing process rules for semiconductors, and outlines mitigation techniques such as materials, physical layout and design tools that FPGA vendors provide to users. Second, this Supplement discusses the design methodology of communication equipment, including consideration of reliability specification by using these mitigation measures. Finally, this Supplement discusses recent trends for mitigation measures for FPGAs.

History

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Introduction

The field programmable gate array (FPGA) is the mainstream component in recent large-scale integrated circuits (LSIs). The configuration data for determining the circuit configuration of an FPGA is stored in static random access memory (SRAM) so that arbitrary functions can be implemented. For that reason, an FPGA may be susceptible to soft errors which have a large influence on the system. Therefore, it is important to implement mitigation measures into the circuit design stage of an FPGA. This Supplement summarizes design examples of soft error mitigation measures for the SRAM-type FPGA.

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