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V.41

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

ITU-T Recommendation V.41

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.41 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression “Administration” is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation V.41

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

(Mar del Plata, 1968, amended at Geneva, 1972)

1 General

This Recommendation is primarily intended for error control when implemented as an intermediate equipment which may be provided either with data terminal equipment or with the data circuit-terminating equipment. The appropriate interfaces are shown in Figures 1/V.41 and 2/V.41. The system is not primarily intended for use with multi-access computing systems. The Recommendation does not exclude the use of any other error-control system that may be better adapted to special needs.

The modems used must provide simultaneous forward and backward channels. The system uses synchronous transmission on the forward channel and asynchronous transmission on the backward channel. When modems to Recommendation V.23 are used with data signalling rates of 1200 or 600 bit/s in the general switched telephone network, Recommendation V.5 applies, the error-control equipment being classed as communication equipment. The margin of the synchronous receiver should be at least $\pm 45\%$.

The system employs block transmission of information in fixed units of 240, 480, 960 or 3840¹⁾ bits and is therefore most suited to the transmission of medium or long data messages, but a fast starting procedure is incorporated to improve the transmission efficiency for shorter messages.

Error control is achieved by means of automatic repetition of a block upon request (ARQ) from the data receiver. If storage is provided at the receiver, detected errors can be removed before the system output (clean copy). Storage for at least two data blocks must be provided at the transmitter.

The forward bit stream is divided into blocks each consisting of four service bits, the information bits, and 16 error-detection (or check) bits in that order, the check bits being generated in a cyclic encoder. Thus each block transmitted to line contains 260, 500, 980 or 3860¹⁾ bits.

The system will detect:

- a) all odd numbers of errors within a block;
- b) any error burst not exceeding 16 bits in length and a large percentage of other error patterns.

Assuming a distribution of errors as recorded in reference [1], the error-rate improvement factor has been indicated by a computer simulation to be of the order of 50 000 for a block size of 260 bits.

The fixed block system employed limits the use of the system to those lines having a loop propagation time not greater than the figures given in Table 1/V.41. Allowances of 40 ms for total modem delay and 50 ms for the detection of the RQ signal have been made.

1) This block length is suitable for circuits provided by means of geostationary orbit satellites.

TABLE 1/V.41

Maximum permissible line loop propagation times (ms)

Data signalling rate (bit/s) Block size (bits)	200	600	1200	2400	3600	4800
260	1 210	343	127	18	-	-
500	2 410	743	327	118	49	14
980	4 810	1543	727	318	182	114
3860	19 210	6343	3127	1518	982	714

2 Encoding and checking process

The service bits and information bits, taken in conjunction, correspond to the coefficients of a message polynomial having terms from x^{n-1} (n = total number of bits in a block or sequence) down to x^{16} . This polynomial is divided, modulo 2, by the generating polynomial $x^{16} + x^{12} + x^5 + 1$. The check bits correspond to the coefficients of the terms from x^{15} to x^0 in the remainder polynomial found at the completion of this division. The complete block, consisting of the service and information bits followed by the check bits, corresponds to the coefficients of a polynomial which is integrally divisible in modulo 2 fashion by the generating polynomial.

At the transmitter the service bits and information bits are subjected to an encoding process equivalent to a division by the generator polynomial. The resulting remainder is transmitted to line immediately after the information bits, commencing with the highest order bits.

At the receiver, the incoming block is subjected to a decoding process equivalent to a division by the generator polynomial which in the absence of errors will result in a zero remainder. If the division results in other than a zero remainder, errors are indicated.

The above processes may conveniently be carried out by a 16-stage cyclic shift register with appropriate feedback gates (see Figures I-1/V.41 and I-2/V.41) which is set to the all 0 position before starting to process each block; at the receiver the all 0 condition after processing a block indicates error-free reception.

Use of scramblers - Where self-synchronizing scramblers (i.e. scramblers which effectively divide the message polynomial by the scrambler polynomial at the transmitter and multiply the received polynomial by the scrambler polynomial at the receiver) are used, in order to ensure satisfactory performance of the error-detecting system, the scrambler polynomial and the Recommendation V.41 generating polynomial must have no common factors. Where this condition cannot be maintained, the scrambling process must precede the error detection encoding process and the descrambler process must follow the error detection decoding process. Where additive (i.e. non-self-synchronizing) scramblers are used, this precaution need not be observed.

3 The service bits

3.1 Block sequence indication

The four service bits at the beginning of each block transmitted to the line indicate the block sequence and convey control information external to the message information. One of these control functions is to ensure that the information block order can be checked during repetitions, thus ensuring that information is not lost, gained or transposed. Three block sequence indicators A, B and C are used cyclically in that order.