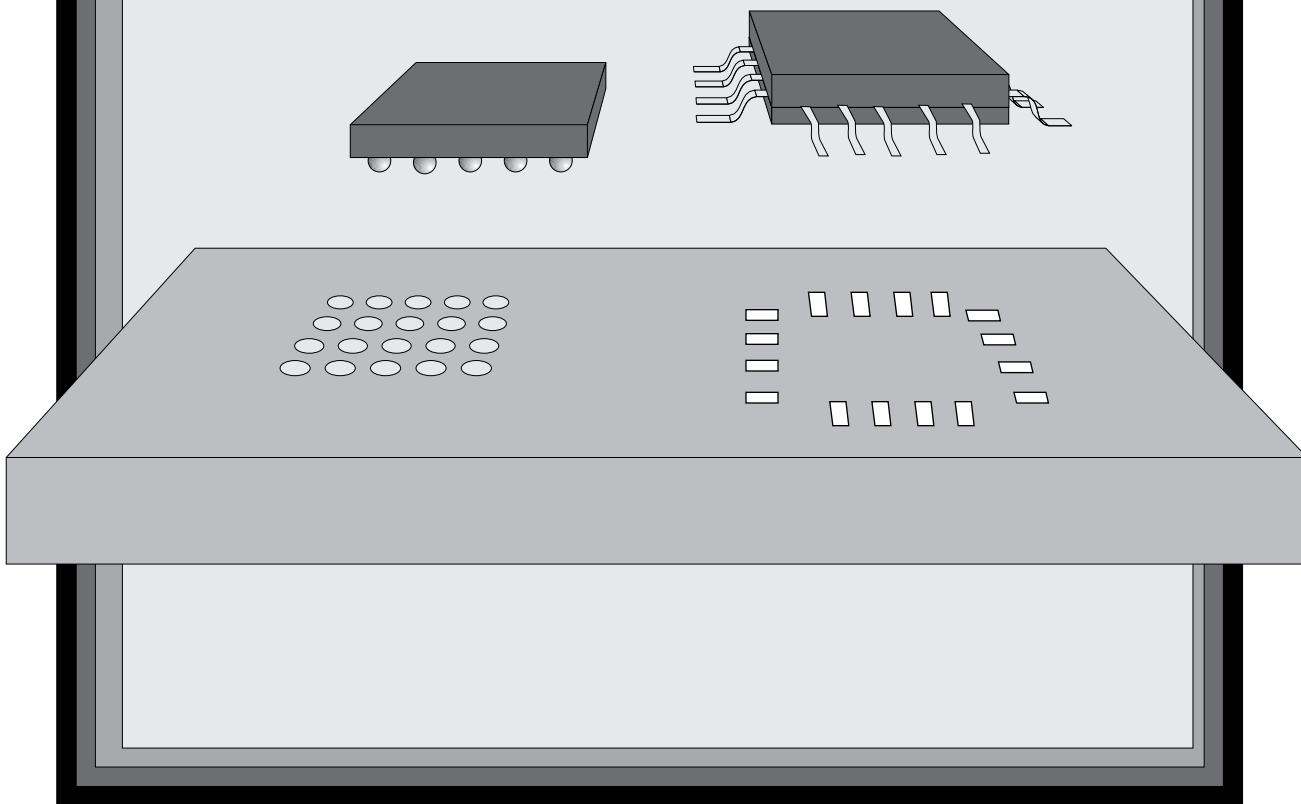


J-STD-013
JULY 1996

JOINT INDUSTRY STANDARD

IMPLEMENTATION of BALL GRID ARRAY and other HIGH DENSITY TECHNOLOGY



COORDINATED BY THE SURFACE MOUNT COUNCIL



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Material in this standard was voluntarily coordinated by the Surface Mount Council (SMC), and established by Technical Committees of IPC and EIA. Committee members of the two organizations contributed their time, knowledge and expertise to blend a cohesive report on the topic covered by this document. Proposals were sent to key individuals in each of the individual organizations for consensus. Meetings were held to resolve differences or conflicts prior to documenting the information in the final released version.

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Comments Welcome

The J-STD-013 is intended to serve as a roadmap for ball grid array and other high-density technology implementation.

In order to keep the document current, the Surface Mount Council welcomes comments from individuals reading the document, or implementing the suggested concepts.

Comments may be sent to the EIA or IPC. All comments will be organized and sent to representatives of the Ad Hoc Committee responsible for the J-STD-013 for a yearly review and incorporation into the updating procedures.

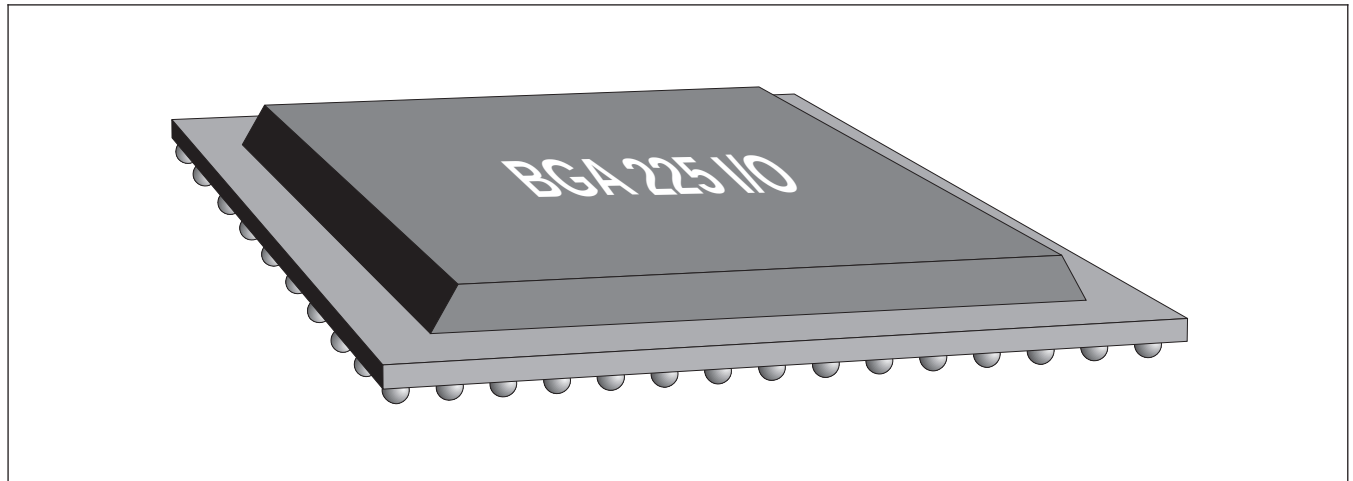
Final Ballot Edition

The Surface Mount Council has authorized the special printing of this document in order to make the information available to industry experts for final ballot approval.

The official publication will be released for full industry circulation after the final editorial revision and completion of the balloting process by representatives of JEDEC. The results of those processes may initiate some changes. Once consensus has been reached, the official J-STD-013 will be printed and be supported by the three organizations, EIA, IPC, and JEDEC, and endorsed by Sematech and MCNC whose representatives participated and contributed to the development of this document.

J-STD-013

IMPLEMENTATION OF BALL GRID ARRAY AND OTHER HIGH-DENSITY TECHNOLOGY



About this Document

This document is intended to report on the work being done by a variety of organizations concerned with surface mounting of area array packages or other high pin count package configurations. The details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade association any comments or observations regarding details published in this document, or provide additional ideas and details that would serve the industry.

Section 8 of this document represents a listing of standards that are being developed, being updated, or need to be created in order to provide for the orderly implementation of Ball Grid Array, or other High-Density Technology. Members of the industry are invited to participate in the ongoing standardization process.

For additional information regarding material published herein or inquiries regarding the status of standardization activities, we urge you to contact the organization listed below.

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Implementation of Ball Grid Array and Other High Density Technology

1 SCOPE

This document establishes the requirements and interactions necessary for Printed Board Assembly processes for interconnecting high performance/ high pin count I/C packages. Included is information on design principles, material selection, board fabrication, assembly technology, testing strategy, and reliability expectations based on end-use environments.

The focus of the document is on design through testing issues related to Ball Grid Array and other high performance packages including fine pitch, ultra fine pitch and thru-hole PGA.

1.1 Purpose

The purpose of this document is to provide confidence in the Design through Testing processes to ensure that the final assembly will meet the intended goals for product performance. Reliability is established through end use environments that consider the performance requirements of assemblies that are used in electronic products in such markets as consumer, computer, telecommunication, commercial aircraft, industrial & automotive passenger compartment, military ground & ship, space (both LEO and GEO), military avionics, and automotive underhood electronics and the customary use of those equipments.

1.2 Categorization

The details contained herein are organized according to the various issues and are correlated to the specific high pin count, high performance type I/C packages. These include:

- BGA Ball Grid Array
- CBGA Ceramic Ball Grid Array
- CCGA Ceramic Column Grid Array
- TBGA Tab Ball Grid Array
- MBGA Metal Ball Grid Array
- PPGA Plastic Pin Grid Array
- PGA Pin Grid Array (Standard and Staggered Pins)
- SGA Stud Grid Array (Surface Mount Version of PGA)
- LGA Land Grid Array
 - * Plastic
 - * Ceramic
- QFP Quad Flat Pack
- CQFP Ceramic Quad Flat Pack
- SSOP Shrink Small Outline Package
- TSOP Thin Small Outline Package
- TQFP Thin Quad Flat Pack

- FQFP Fine Pitch Quad Flat Pack
- LQFP Low Profile Quad Flat Pack
- SVP Surface Vertical Package (Post Stand/Lead Stand)

Organization of the information is initially provided in accordance to the specific processes (i.e. Design-Fabrication-Assembly-Test). Component information is organized with emphasis on area array type packages. Although there is some discussion of the peripheral format, the major emphasis is on the decision process that forces the manufacturing direction into the area array type package. Table 1-1 indicates the packages of choice in various integration of semiconductor technology. Usually the trade-offs switch from peripheral packages to array type packages at 208 pins or below 0.5 mm pitch on the peripheral package.

Table 1-1 Choice of Packages

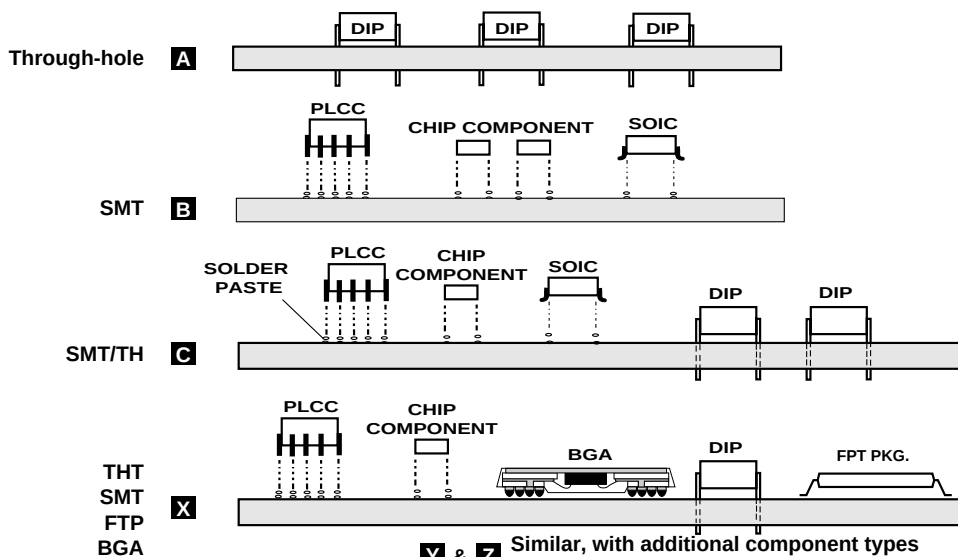
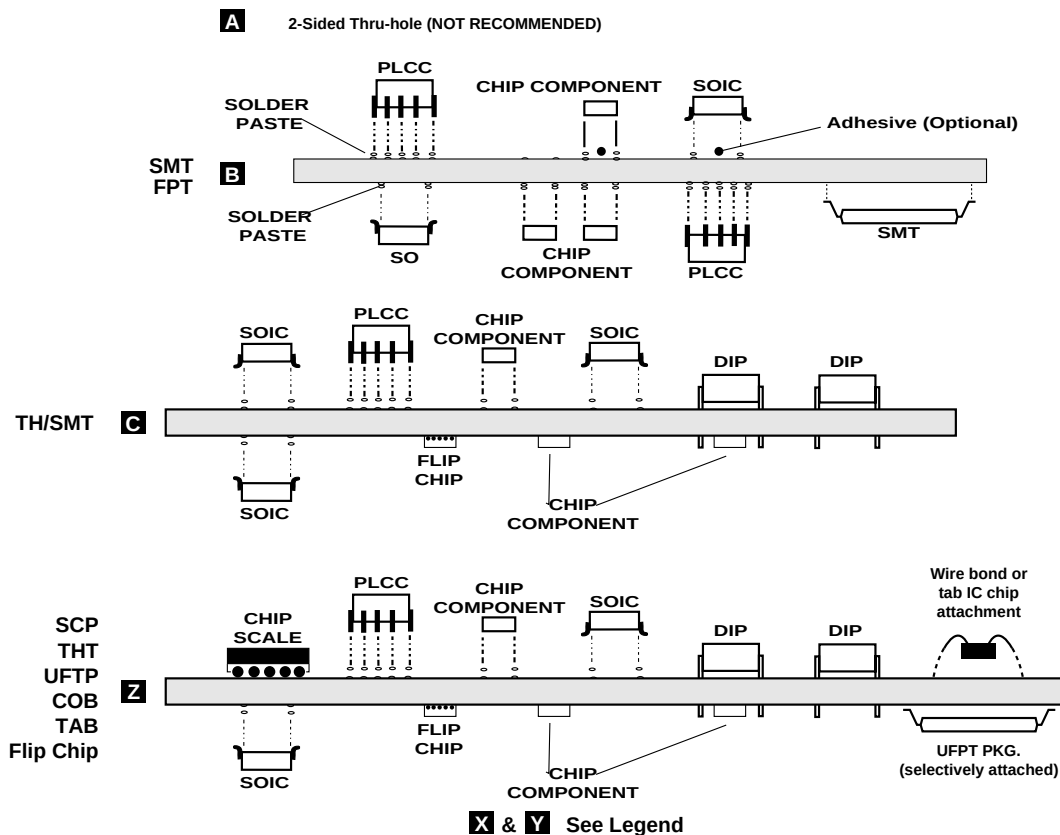
Semiconductor Integration	Number of Pins, Leads or Balls	Package Types
SSI	16-48	SOIC
MSI	48-156	QFP/PGA/BGA
LSI	156-256	BGA/QFP (0.5, 0.4, 0.3 mm pitch) and PGA
VLSI	256-500	BGA/PGA
ULSI	>500	BGA

1.3 Presentation

All dimensions and tolerances in this standard are expressed in metric units, with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off concept or the required precision. Users are cautioned to employ a single dimensioning system and not intermix millimeters and inches. Reference information is shown in parentheses ().

1.4 Producibility Levels

The Surface Mount Council, in their "Status of the Technology, Industry Activities and Action Plan" identified several levels of complexity based on manufacturing and assembly processes for electronic assembly. A differentiation was developed that correlated the ease with which an assembly process could place, and attach all the parts and test the final product. Letters were assigned to reflect progressive increases in sophistication of tooling, materials or number of processing steps.

Type 1 Components (mounted) on only one side of the board**Type 2** Components (mounted) on both sides of the board**Legend:**

- Class A = Through-hole component mounting only
- Class B = Surface mounted components only
- Class C = Simplistic through-hole and surface mounting intermixed assembly
- Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch BGA
- Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
- Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

Figure 1-1 Electronic Assembly Types

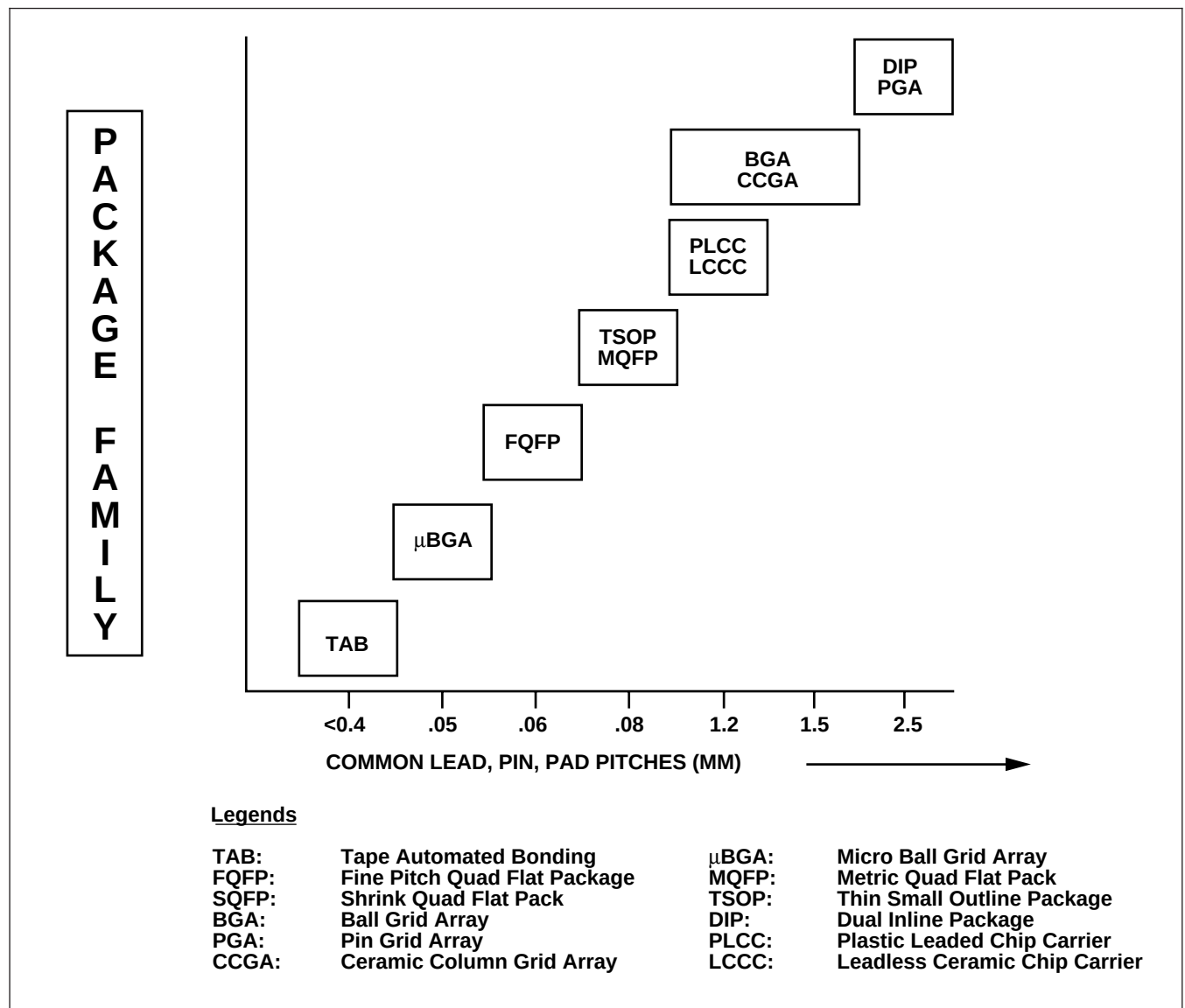


Figure 2-1 Common Lead Pitches in Package Family

The six classes identified were:

- Class A = Through-hole component mounting only
- Class B = Surface mounted Components only
- Class C = Simplistic through-hole and surface mounting intermixed assembly
- Class X = Complex intermixed assembly, through-hole, surface mount, fine pitch BGA
- Class Y = Complex intermixed assembly, through-hole, surface mount, ultra fine pitch, chip scale
- Class Z = Complex intermixed assembly, through-hole, ultra fine pitch, COB, flip chip, TAB

It should be noted that most of the applications for components in this document fall into the Class X or Y category.

In addition, a type designation signifies further sophistication describing whether components are mounted on one or both sides of the printed circuit board or interconnecting structure. Figure 1-1 shows some of the electronic assem-

bly types where Type One has components mounted only on one side, while Type Two has components mounted on both sides. The definition of assembly types discussed in this publication would be Type 1X, 1Y, 2X and 2Y.

2 TECHNOLOGY OVERVIEW OF BOARD AND ASSEMBLY REQUIREMENTS

Continued emphasis on faster, smaller and lighter electronics systems is making component, board and system packaging more complex. The complexity is increased due to increasing use of surface mount packages, which are the key to miniaturization of electronics products. Most of the components on a typical mother board for desktop systems are 1.27 mm [0.050 in] pitch surface mount components with increasing use of fine pitch [0.65 mm and 0.5 mm pitch] packages. See figure 2-1 for various types of packages commonly used today on a typical printed circuit board.

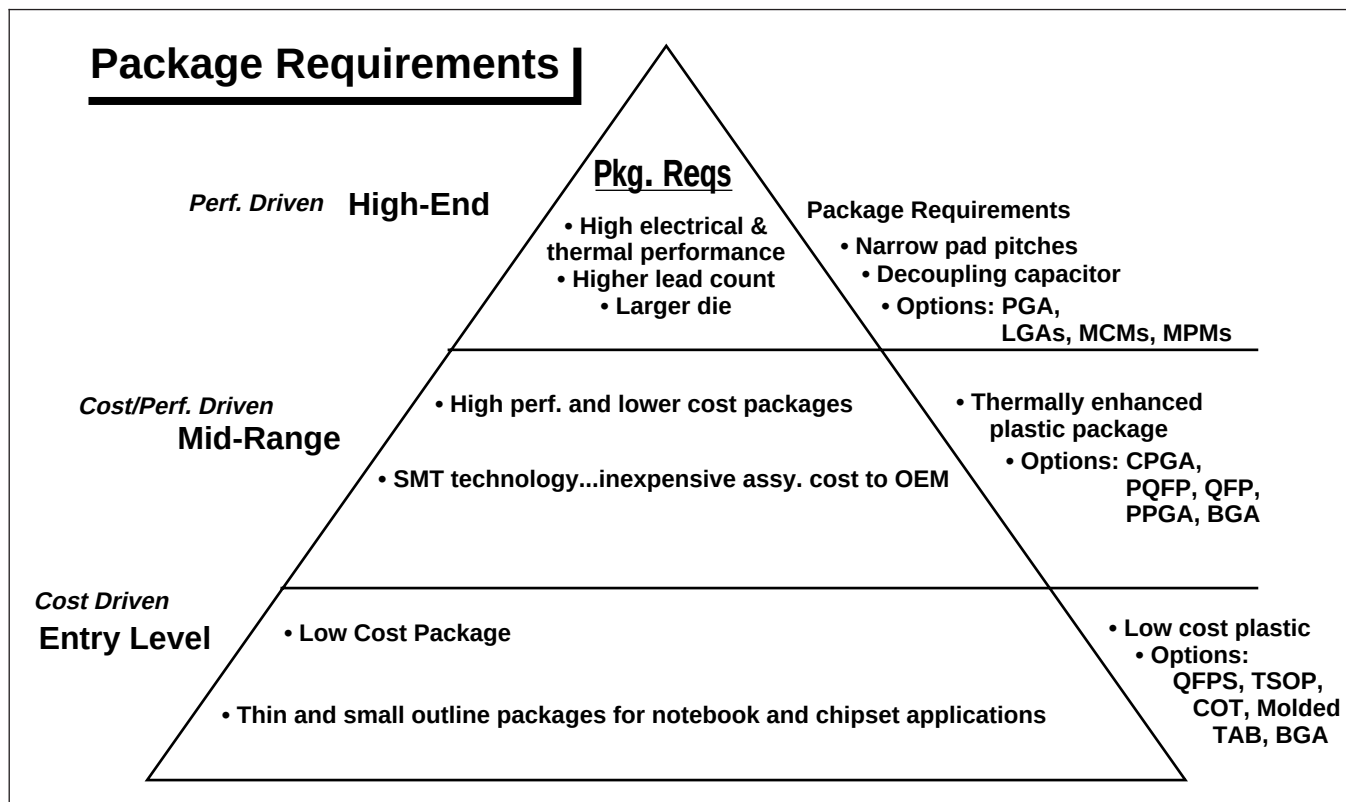


Figure 2-2 Component Packaging Requirements for Different Types of Systems

Lead pitch plays a critical role in the complexity of the manufacturing process. Demands on solder paste printing, pick-and-place accuracy, reflow, and rework become more precise. And since surface mounting generally requires automation for precision placement and paste printing, hundreds of assemblies may be built before a problem is discovered. Use of very fine pitch only compounds the problem in board manufacturing since with increased complexity, yields drop and rework becomes either more difficult or impossible. Thus, a design with parts with large I/O count (i.e. over 208), or below 0.5 mm pitch is the time to consider crossover from peripheral packages to array packages.

The combination of various drivers described in 2.1, will establish a dynamic cross-over point based on assembly capability (i.e. equipment precision), and relative state of the art, for each company mounting BGAs or QFPs.

2.1 The Drivers for Component Packaging

Component packaging in general, and microprocessor packaging in particular, drive the rest of board packaging issues. The driving forces for component packaging are thermal and electrical performance, real estate constraint and cost. As shown in Figure 2-2, the component packaging requirement varies for different types of systems. For example, the high end microprocessors run at higher frequencies and require thermally and electrically enhanced packages.

Enhancements are thermal vias, heat slugs, heat sink and fan heat-sink (fan mounted on heat sink) etc. and examples of electrical enhancements are multi-layer packages and in-package capacitance. Generally hermetic ceramic package are used for this application. For mid-range systems, performance is important but so is cost (not that cost is not important for high end systems.) Thermally enhanced, multilayer packages (Plastic PGA or QFP, BGA) may be appropriate for this application. For low end entry level and portable systems, cost and form factors are critical and generally surface mount packages such as QFP, TSOP and TAB are used.

2.1.1 The Thermal Drivers

With the introduction of new generations of microprocessors, power dissipation has continually moved upward. There is every indication that this will be true in the future. As speed increases, power goes up. This problem is somewhat mitigated, fortunately because die shrink is made possible by finer feature semi-conductor processes and the trend towards lower power supply voltages. For higher wattage packages, ceramic PGA (CPGA) packages have been commonly used, however, TBGA, Metal BGA and enhanced TBGA packages are gaining some attention. For the mid range systems, thermally enhanced plastic packages are being evaluated by the industry. An example of a thermally enhanced SMT plastic package is shown in Figure 2-3.

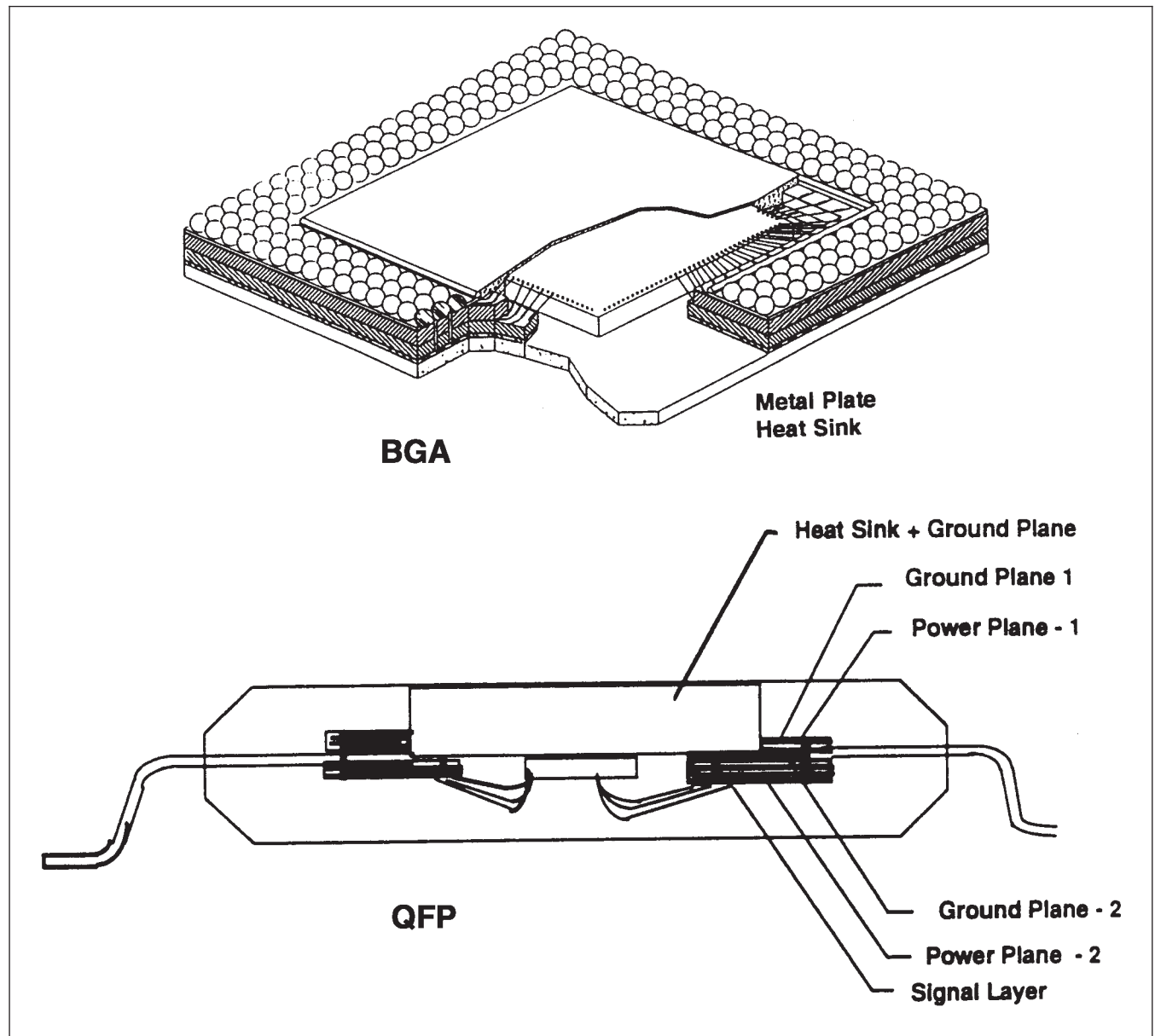


Figure 2-3 Thermally Enhanced Package

2.1.2 The Electrical Drivers

Increasing functionality and speed requires more power, a higher number of bond pads on the die and more pins on the package. Fortunately, even with the increase in bond pads, the pin count is kept to a minimum by using de-coupling capacitors in the package and on the die. In addition, by adding power and ground planes in the package, the number of pins can be further reduced. For example, if no electrical enhancement is used, the number of package pins will equal the number of die bond pads. If this was the case, the number of pins for some microprocessors would be staggering. By using in-package capacitance and multi-layer packages, the pin count is kept to a minimum. In enhanced plastic packages, the pin count is higher since addition of too many layers and in-package capacitance is generally not feasible. For example, a micro-

processor that has 168 pins in a ceramic PGA, might require 196 pins in a plastic surface mount package.

2.1.3 The Real Estate Drivers

The real estate constraint is also one of the important driving forces in component packaging. This has been one of the main reasons for wide spread usage of surface mount devices which are not only smaller in size but facilitate component mounting on both sides of the board. Above certain pin counts, the pitch must drop to keep the body size within a practical range for manufacturing. For example, when the pin count increases above 84 pins, the pitches drop from 1.27 mm to 0.65 mm. However, if the pin count goes beyond 200 pins, finer pitches such as 0.4/0.3mm TAB or fine pitch QFPs become necessary which complicates the manufacturing process.

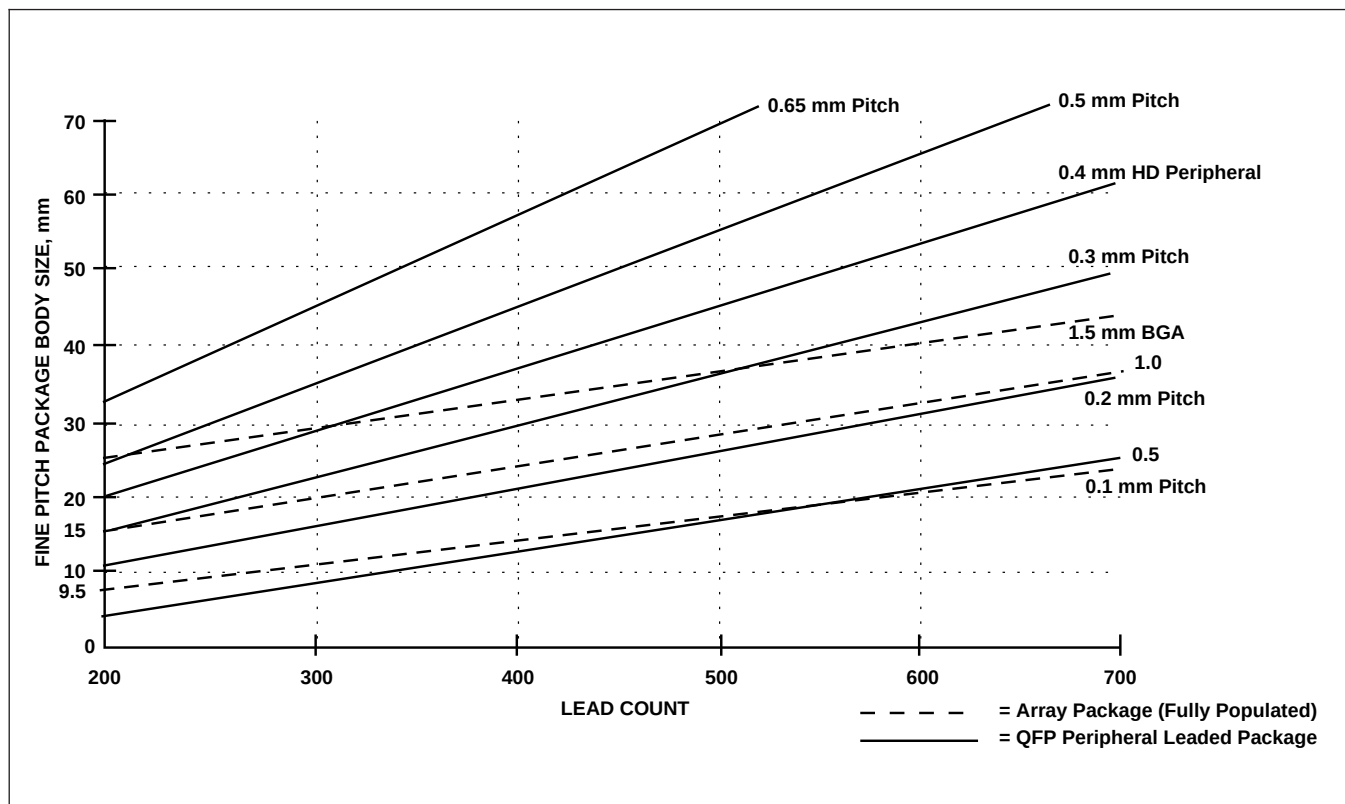


Figure 2-4 I/O Pitch Mounting Area Comparisons

finer pitches is larger body sizes, with the associated real estate penalties. Thus, the move to array type packages where the processes are more robust and provide assemblies with higher first pass yields. See figure 2-4.

2.1.4 Specific Package Drivers

There are generic package drivers such as cost, thermal and electrical enhancements, assembly yield, reliability, and real estate constraints. These relate to the package style and the ability of the form factor to fit into the main process for the product assembly.

Although not every integrated circuit is available in every package style, meeting the requirements of the assembly application become paramount. Package performance in both assembly and ability to withstand the end use environment are the main criteria for the selection. It is incumbent on the user to determine the requirements of the product's end use environment, and select the proper combination of package styles and the interconnecting substrate to be used.

The relationship of substrate and package is extremely important because the reliability of the joint, using a lead from a peripheral package, a ball for an array package, or a pin from a through hole package, determines the cyclic predicted failure rate that can be achieved.

2.1.4.1 Ball Grid Array (BGA) Drivers

A package known as the Ball Grid Array (BGA) has two main advantages over peripheral leaded packages. First, a

BGA with a 1.5 mm ball pitch occupies less real estate than a 0.4 mm pitch QFP with 300 pins. The second advantage is that the BGA is easier to assemble than an equivalent fine pitch high lead count package.

The complexity of the board assembly increases dramatically with a reduction in lead pitch. Even at 0.5 mm pitch, considerable problems, such as lead bend, sweep and coplanarity are encountered.

Absence of fragile leads susceptible to handling damage helps make the BGA a much more robust package. Hence it provides much better manufacturing yield. There have been reports by some users that even today the yield of a BGA package is much better than that of 0.63 and 0.5 mm fine pitch peripheral lead packages. Currently BGAs are being used by several computer companies with very high assembly yields.

The BGA allows the use of conventional surface mount placement equipment, solder dispensing and reflow processes.

Companies using BGA are reporting major improvement in manufacturing efficiency. For example, a large multinational company using 0.5 mm pitch quad flat pack devices could not improve the assembly process defect ratio below 200 to 300 ppm. When the same product was redesigned using ball grid array packages, the defect factor dropped to 3 ppm (parts per million).

2.1.4.2 PGA Drivers

The Pin Grid Array (PGA) was the first area array package adapted for high pin count and high performance applications. Most packages are based on inch grid spacing [0.100 in].

Some of the advantages of a PGA are that it can either be socketed or directly soldered with minimum reliability concerns. Many OEMs directly solder PGAs to achieve lower cost even though they use sockets during development stages. Most important of all, socketing allows system upgrade by the end user without buying a whole new system. Tariff on the imported mother board also plays a role in favor of socketing PGAs. To minimize tariff on mother boards assembled overseas, processors (the most expensive component on the board), are inserted in the home country.

2.1.4.3 Fine Pitch Plastic Drivers

The primary driver for fine pitch is real estate constraint. In addition, there is significant cost saving in using FQFPs, in some cases well above 50 percent over PGA. In other cases, fine pitch plastic packages provide a lower profile package necessary for portable electronics. This fine pitch plastic package is also a common package for high pin count (over 100) ASIC (application specific integrated circuit) devices. In many cases, ASICs are used for reducing thermal load by combining 10 to 20 programmable logic array devices which would consume 5 to 10 watts each into a 2 to 4 watt single ASIC device. These packages allow thermal and electrical enhancements by use of heat slugs and multilayer boards while significantly reducing cost. However, package reliability and moisture susceptibility are some of the concerns that must be addressed before using thermally and electrically enhanced plastic packages.

2.2 Issues in Component Packaging

It should be noted that there are issues with every package option. Issues include:

- Package assembly
- Repair
- Susceptibility to moisture absorption
- Inspectability of final solder joint
- Handling of parts prior to assembly
- Handling of parts during assembly

Depending on pitch and contact density, BGA packages may require additional layers for conductor routing since it is more difficult to route area array land patterns than peripheral land patterns. Raising layer count will raise board cost.

Repair of BGAs may also be difficult. BGAs cannot be soldered by laser or hot bar processes. Since BGA solder joints cannot be inspected, one must primarily depend upon process control. The lack of inspectability of BGAs may not be a significant barrier for using the BGA if one con-

siders the alternative of using an ultra fine pitch package. A quantum jump in surface mount manufacturing technology is required to establish a complete infrastructure for 0.4 mm and smaller pitch packages.

The major issues with fine pitch QFPs will be handling, lead coplanarity, paste printing and placement. Availability of boards with an even thickness of solder may also be a problem. It should be noted that there are issues with every package option. Issues include package assembly, repair, susceptibility to moisture absorption and inspectability of the final solder joint. Companies are still going through the learning curve with moisture susceptibility of some plastic packages.

Handling of packages prior to and during the assembly operation must be approved. Solder may be applied by the board vendor by paste printing or plating or use of a protected copper surface may be necessary. Even if such a capability is developed, the yield differential between fine pitch QFP and BGA may remain.

There are some additional issues such as the foot length on gull wing leads to allow reflow and hot bar soldering of QFP especially if packages are shipped trimmed and formed. Hot bar or other equivalent processes may be required if the packages are susceptible to moisture induced package cracking. Additional handling incurred in moisture protected packages during baking and bagging may further compound the costs associated with using QFPs.

Finer pitches (below 0.4 mm) of high pin count devices may require the use of tape carrier packaging (TCP) or wire bonding of the chip to the device lead frame. Some have suggested skipping the QFP or plastic package altogether and moving directly to direct chip attach using TCP. Tape carrier packages will require the resolution of the same board and assembly related issues as fine pitch QFP. In addition, the technology for chip encapsulation needs to be defined. The lack of industry infrastructure for TCP is one of the major issues.

The Pin Grid Array has some problems as well. While it has served well for lower pin counts, it may not be the package of choice for higher pin counts with large heat sinks attached to it. The high pin count PGA packages used for high performance processors cannot afford to use a high inductance socket. The LGA package has a concern with socketing reliability since the LGA may require selectively gold plated lands on the PCB for connection. This adds to the cost of the board.

2.2.1 Future Considerations

Additional work is necessary for full acceptance of the processes. Figure 2-5 summarizes the issues that need to be resolved before new packages such as QFP, TCP and BGA are widely used by the industry. There is a mature infrastructure in place for dealing with PGA and QFP (U.S. SMT

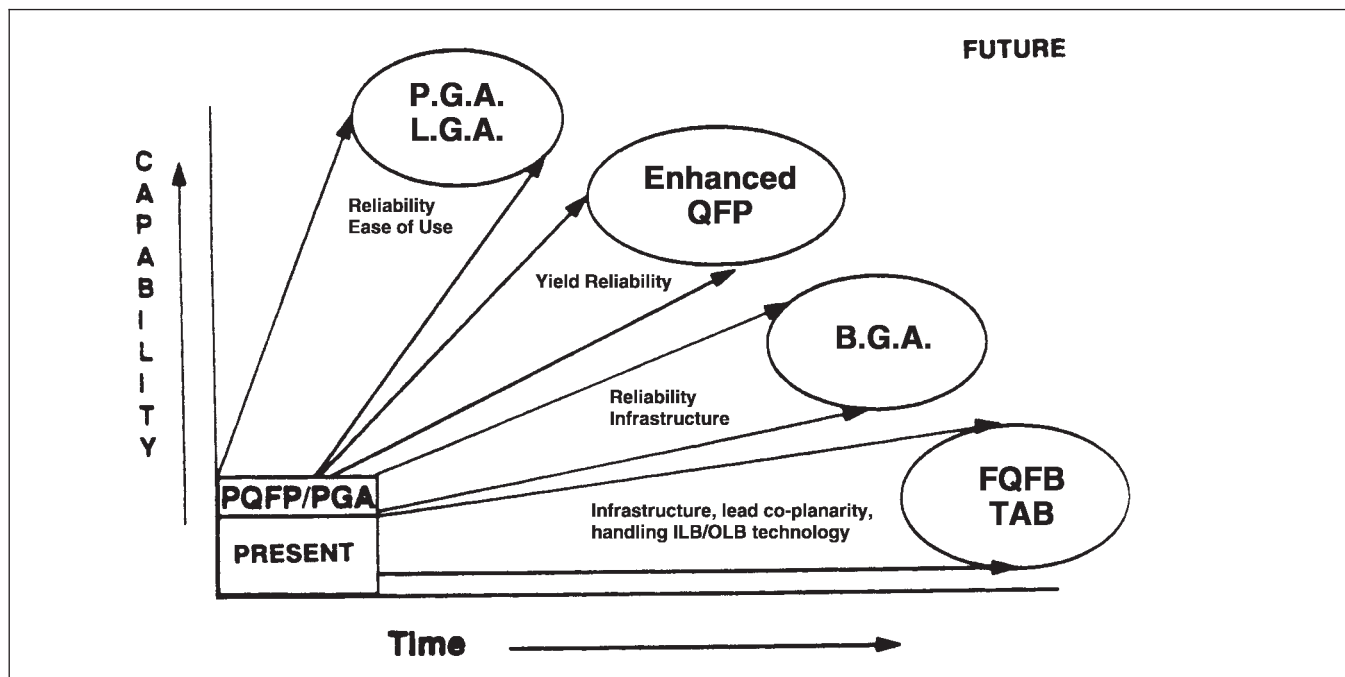


Figure 2-5 The Move from Present to Future Requirements

pitch and above) packages. They do not address all our needs, so we have to explore high pin count CPGAs, enhanced plastics, BGAs, TCP and QFP. In turning that vision into reality, there is much to be done. Here are some specific options: heat spreader or heat slug or some other form of thermal enhancement is needed for high power devices most likely to be packaged in ceramic PGAs. A multilayer thermally and electrically enhanced plastic package is needed for a lower cost option. This can be either in fine pitch QFP or BGA with a preference for BGA over fine pitch QFP packages.

As the performance and speed of microprocessors increase, pin counts increase. This trend will continue despite the fact that these packages will be electrically enhanced by using multilayer packages with in-package capacitance for decoupling. For cost reduction, thermally and electrically enhanced plastic QFP and BGA packages will become common.

To reduce board complexity and to increase manufacturing yield, ball grid array package use will become commonplace. Despite increased complexity in packaging and assembly, the primary driver will be cost. The winners will be those suppliers who not only meet the technical challenge to provide a solution, but do so at a continuously decreasing price.

2.3 Impact on Interconnecting (Printed Board) Technology

Printed boards must accommodate building intermixed component technology assemblies. Hot air solder leveling (HASL) is a commonly used process for applying solder to the top layers. The solder thickness on the lands of various

types of packages on the same board vary widely from a low of 0.1 mm to a high of .25 mm. Too much solder thickness may result in solder opens due to coplanarity variation and too little solder may result in dewetting. In order to achieve a more uniform thickness, various other options such as plating, applying solder by screen printing or flattening solder after HASL are some of the options for the industry.

The other concern that the board industry must address are building four to six layer boards while keeping board thickness under 0.5 mm for PCMCIA (Personal Computer Memory Card Information Association) applications for the mobile market. It is also difficult to maintain bow and twist to a minimum in thin boards. Even for standard 1.5 mm thick boards, warpage needs to be kept under 0.5 percent as opposed to 1 percent now common.

The use of different packages impact layer count and board area. For example, peripheral fine pitch packages such as FQFP and TCP require more board area, but lower layer count. PGA and BGA packages require less board area, but higher layer count. One should also take into account the total area needed for routing. A BGA occupies less real estate, but could require additional layers for routing.

In addition to the type of package and its pin counts, conductor density also impacts layer count requirement. The number of conductors means the number of lines that can be routed between lands of a PGA on 2.5 mm centers with 1.2 mm lands leaving 1.3 mm for routing between lands. Four conductors for PGA means four lines can be routed between two lands. This is equivalent for a BGA with one

0.65 mm via lands on 1.5 mm centers, allowing three conductors to be routed between the lands.

Effect of pin count on number of layers needed for routing (assuming only 10 percent for power and ground pins) for a BGA and PGA is shown in Figure 2-6. Note that using four conductor density (0.15 mm conductors and spaces) a PGA with 280 pins can be interconnected in four layers, but a BGA with the same pin count will require six layers.

expected, defect rates climb dramatically. The major contributors to assembly defects are PCB (solderability, bow and twist, warpage and uneven solder on lands), components (lead coplanarity, lead pitch, solderability), and incapable assembly processes.

The effect of QFP lead pitch on solder defects is dramatic. As the lead pitch decreases, defects go up, due to the problems associated with a fragile lead (coplanarity, sweep,

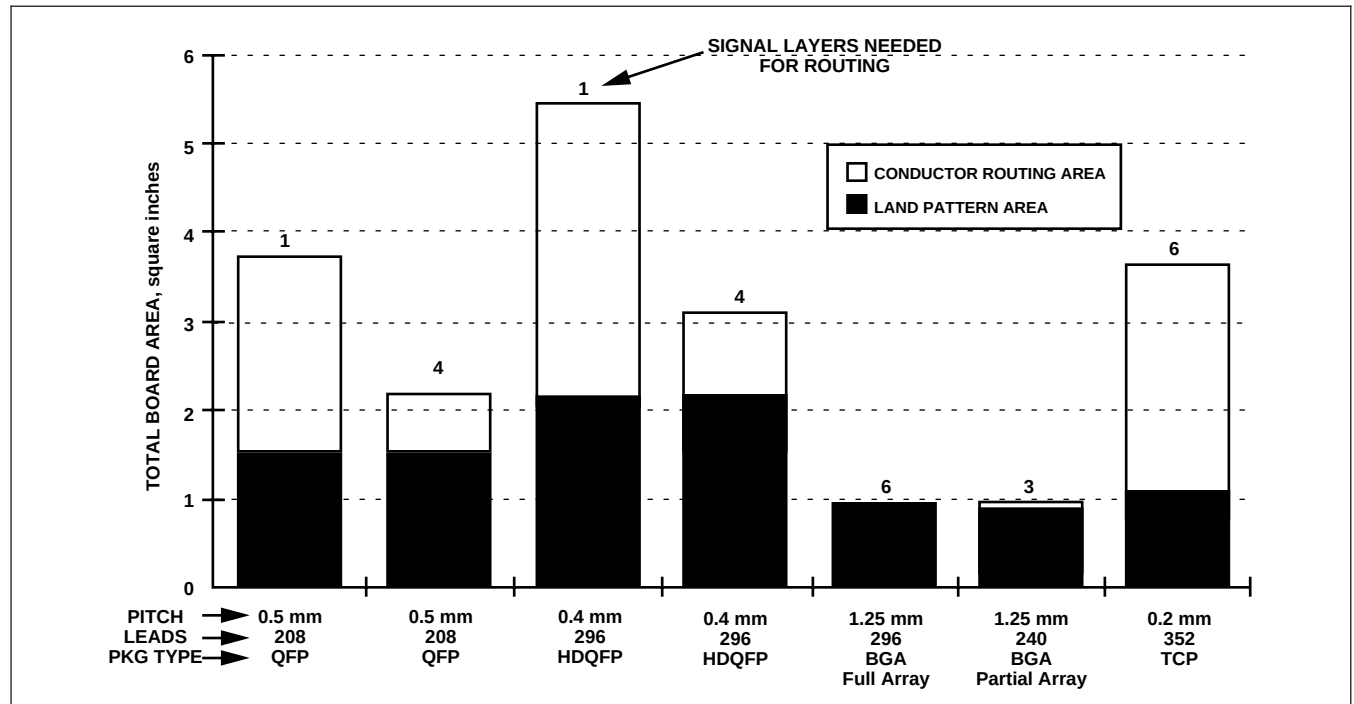


Figure 2-6 Board Routing Area Study

Via hole size, conductor density and layer count are important to keep in mind when selecting a package since they determine board cost. As shown in figure 2-7, board cost shoots up rapidly if the finished via hole size is reduced below .4 mm. Costs increase because drilling and plating yields begin to drop for small vias. It should also be noted that very fine via holes are also susceptible to cracking. One must maintain an aspect ratio of about 4:1 to ensure via hole reliability. Aspect ratio is defined as board thickness divided by preplated or drilled hole size.

As shown in figure 2-8, the layer count and conductor density impact board cost. Board cost dramatically increases if the layer count goes above 8. But in a very competitive market, layer count is kept as low as possible. For example, there is distinct shift from 6 to 4 layer boards. Existing 6 layer designs are being redesigned into 4 layers to lower cost.

2.4 Impact on Assembly

Component packaging not only affects the printed board design, its impact on the board assembly process is even more significant. With increased board complexity, as

bend). This results in solder defects (shorts and opens). As the lead pitches drop below 0.65 mm, it becomes difficult or impossible to provide soldermask between lands, adding to solder bridging if a paste printing process is used. Also, for extremely fine pitch devices, it is difficult or impossible to determine how far off the leads are from target, even for the supplier. It is nearly impossible for some users since they are generally not set up with a method of determining lead or ball array coplanarity.

For the fine pitch package at or below 0.65 mm pitch, there may be significant solder opens primarily due to lead coplanarity as shown in Figure 2-9. The finer the contact pitch of a peripheral or area array package, the more susceptible it is to lead or ball damage, such as lack of coplanarity. And greater coplanarity deviation means more solder opens as shown in Figure 2-9, which shows how a minor coplanarity deviation causes an order of magnitude increase in solder defects.

Special solder paste with finer particles (20 to 45 microns), with higher viscosity and slower printing speed is needed for fine pitch packages. New methods of solder printing (slower speed) and laser cut stencil may be necessary.

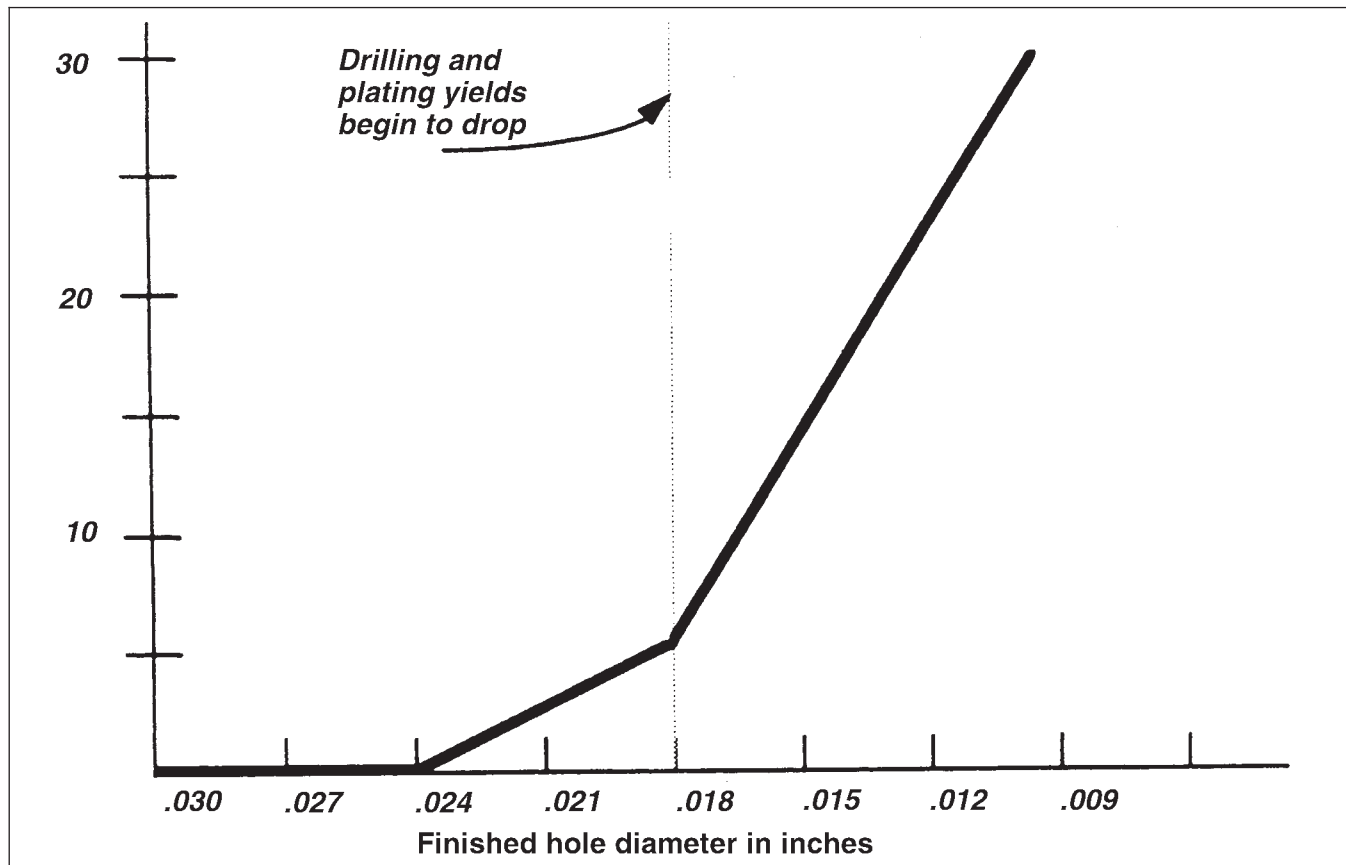


Figure 2-7 Typical Cost Curves - Cost vs. Finished VIA Hole

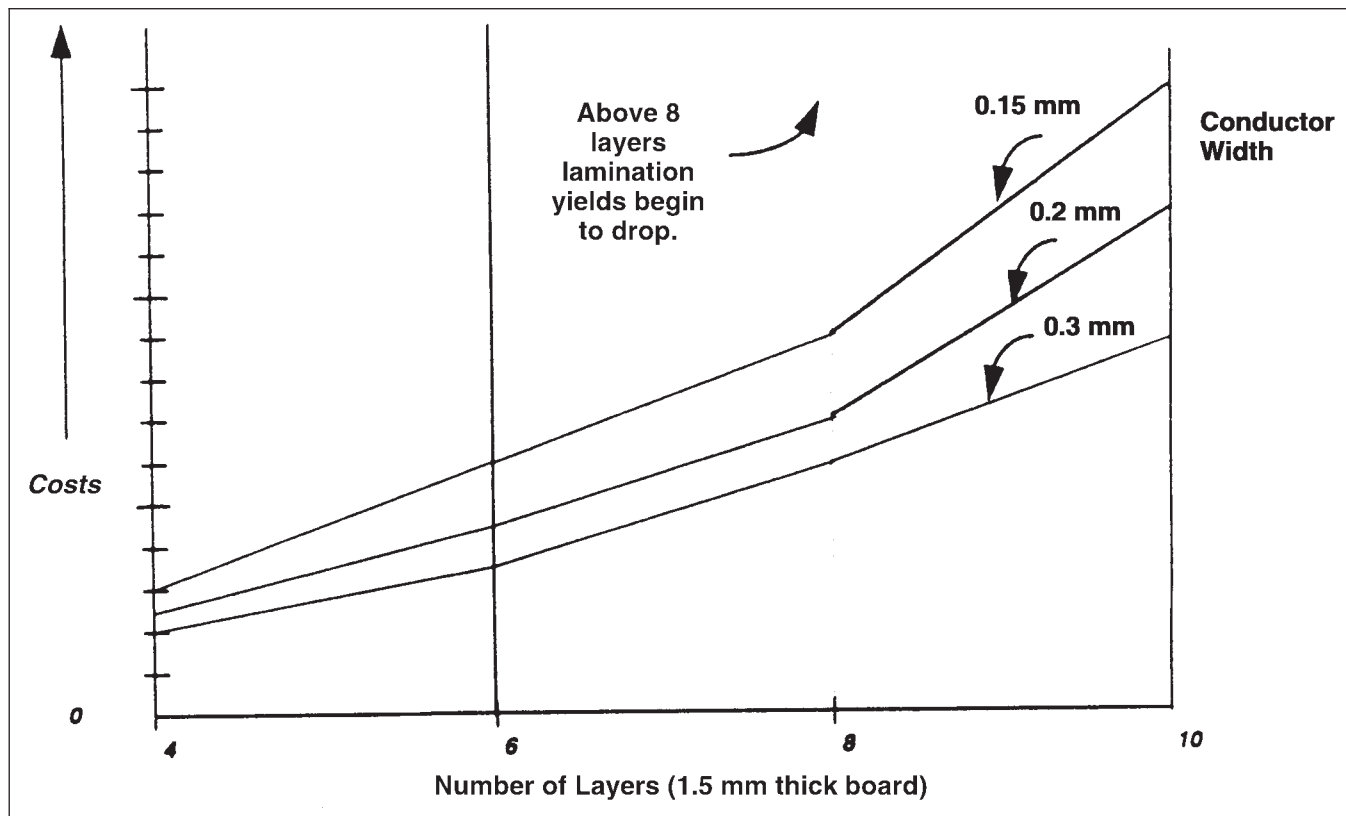


Figure 2-8 Typical Cost Curves - Cost vs. Number of Layers

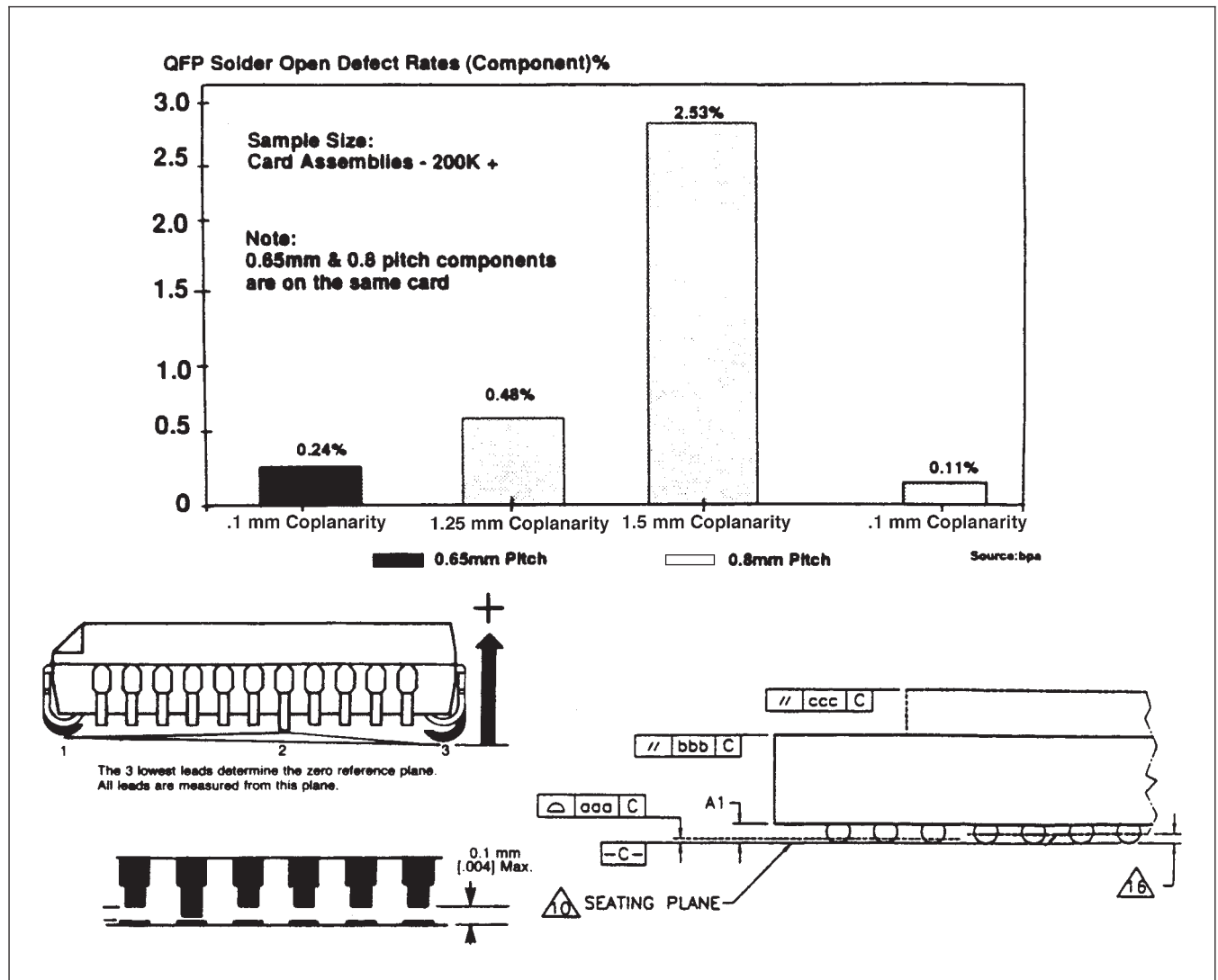


Figure 2-9 Coplanarity Example of QPF Solder Opens

These variables will be even more critical for pitches lower than 0.5 mm.

With emphasis on no clean or low active fluxes, it is becoming popular to use a neutral reflow environment such as nitrogen to achieve good soldering results. It is difficult to clean under these packages, since many have very low stand-off. Figure 2-10 shows the ability to clean under a package is determined by its area and stand-off from the board.

Some packages, especially EIAJ (Japanese) packages have zero stand-off. One cannot perform adequate cleaning under these packages.

Special cleaning consideration is required for a mixed assembly (one requiring wave soldering for through-hole components, after surface mount components have been reflow soldered). Cleanability can be assured only if vias under the packages are filled, or tented to prevent seepage of flux during wave soldering. Filling of vias is accomplished by temporary solvent soluble mask in the via or

permanently by permanent solder mask or plating in the hole. Tenting is usually accomplished using a dry film soldermask.

2.5 Future Implementation Strategies

Increased performance and speed also mean that thermal enhancements such as heat sinks, heat spreader and heat slugs will become more common. Despite these thermal enhancements, higher airflow even in desktop systems will be needed. To ensure quietness in an office or home environment, noise dampening technologies may become essential for systems.

For cost reduction, thermally and electrically enhanced plastic packages will become common. For this to happen, however, the reliability concerns in such packages must be addressed. The complexity of board assemblies will increase because the packages of varying lead pitches, including through-hole will be used. Increasingly wider usage of finer pitch packages will complicate the process.

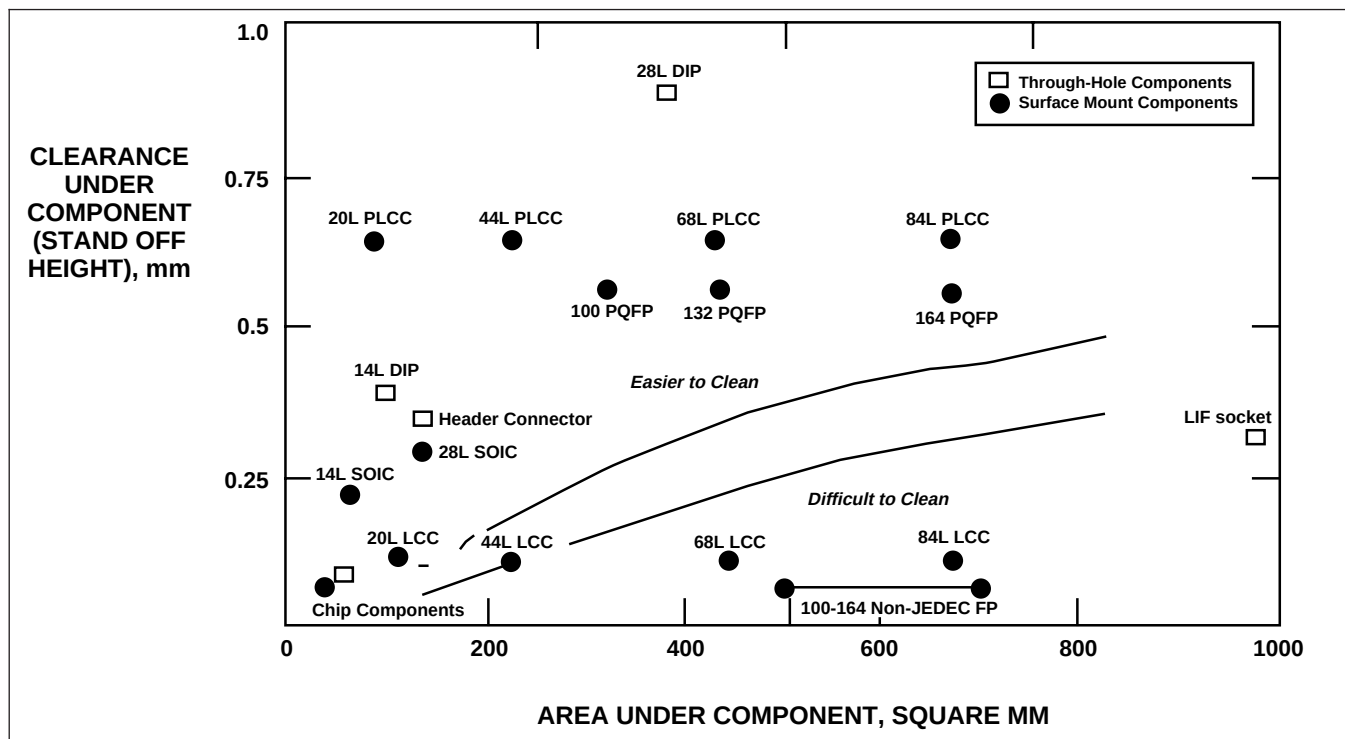


Figure 2-10 Stand-off vs. Cleanability

Some relief may be possible because ball grid array packages will become common, since they reduce process complexity for the user. The effect of complexity in general will be felt by the suppliers and users.

2.5.1 Complexity Matrix

With the advent of such I/C package styles as the Ball Grid Array (BGA), Land Grid Array (LGA), and Column or Ceramic Grid Array (CGA), electronic equipment designers are carefully reviewing their options. Array Surface Mount (ASM) has its benefits and its risks. Positioning tolerances are more liberal. However, quality is achieved through process control as opposed to visual inspection.

Figure 2-11 shows a complexity matrix for packaged parts with leads or terminations around their perimeter; figure 2-12 shows the relationship or evaluation of parts with their leads or terminations on the underside of the package in an array format.

The complexity matrices could help establish the parameters for definition of high pin count and fine pitch. Complexity is judged on a scale of 1 to 10, where 1 is easy and 10 is very difficult. The first number reflects design complexity. Although some designs are easy, others are more difficult because of the number of I/O's that are needed to be interconnected or the board real estate available for accomplishing the interconnection.

A second number in the matrices reflects the difficulty of manufacturing. Manufacturing includes both the manufacture and testing of the bare board as well as the manufacturing and testing of the completed assembly.

Pitch Pin Count	Std. Pitch 2.54 mm	Ultra Std. 1.0 mm	Fine Pitch .63/.5 mm	Ultra Fine Pitch .4/.3 mm	Very Ultra Fine Pitch .25 & Less mm
≤ 68	1-1	1-3	1-6	3-8	4-10
70 - 136	1-1	1-4	1-7	3-9	5-10
138 - 408	7-1	7-4	6-7	6-9	Not Practical
410 - 720	10-3	10-4		N O T	
720 - 1000			P R A C T I C A L		

Figure 2-11 Component Packages with Leads Around Perimeter

Pitch Pin Count	Std. Pitch 2.54 mm	Ultra Std. 1.0 mm	Fine Pitch .63/.5 mm	Ultra Fine Pitch .4/.3 mm	Very Ultra Fine Pitch .25 & Less mm
≤ 68	1-1	1-1	1-1	1-1	1-1
70 - 136	1-1	1-1	1-1	1-1	1-1
138 - 406	2-1	2-1	2-1	2-1	2-1
410 - 720	4-4	4-4	4-4	N O T	
720 - 1000	7-7	7-7	7-7	P R A C T I C A L	

Figure 2-12 Component Packages with Leads Underneath in Array Format



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3 COMPONENT PACKAGES

Packages are essentially only one link in the varied and complex electric interconnect chain that has its beginning at the semiconductor wafer, where transistor feature size defines the first metal interconnecting process. Industry packaging interconnect schemes are varied to meet the electrical, mechanical, manufacturing, cost and reliability expectation of the I/C manufacturer and user applications.

The industry's first I/C packages were simple six-to-eight lead hermetic glass/ceramic or metal/ceramic packages. The assembly processes were restricted to socketing, thermal insertion, wave soldering or welding to the circuit board. Since that time, a multitude of package concepts and several assembly technologies and techniques have been developed, including the most recent development of surface mount technology. The options are a direct reflection of the manufacturing, application, performance and reliability expectations of both the devices and the circuits to which they are interconnected.

Each of the package options fulfills a unique circuit requirement with respect to I/C device and the interconnection application. These factors have therefore led to a proliferation of packaging options. Uniquely, as new package options are added, old ones have not become obsolete, resulting in an ever increasing number of available options. This section defines the interrelationship of the package options to the device and assembly and product requirements.

3.1 Component Identification

I/C packages are described in two basic lead or terminal classifications.

- Area Array
- Peripheral

Since this document is limited to high lead counts/high performance device packages, no definitions will be covered for packages that are effectively restricted to a maximum of 40 leads.

3.1.1 Area Array Component Types

Array lead packages are those types where the emanating terminations or leads are based on some form of grid network that positions the I/O into the output matrix. Originally starting as pins emanating from the package, this concept was an extension of the terminations of the chip contained in the package.

Beginning with four sets of rows around the periphery of the package or near the edge of package, it soon became apparent that additional rows could be added moving toward the center of the device. The concept continued until all available positions in the pin output matrix were occupied; thus the term pin grid array became synonymous with the image of the output pins. See figure 3-1.

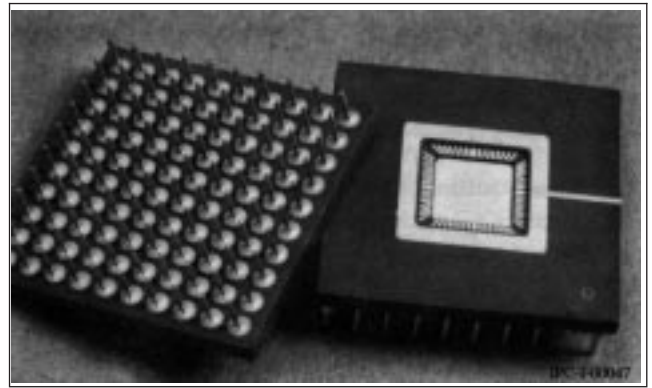


Figure 3-1 Pin Grid Array

Various perpetrations of area array type packages have evolved. The format is ideal for translating the chip bonding sites to the next level interconnect; however, increased use of surface mounting has become less desirable. Also there is a need to increase the utilization of the interconnecting real estate for making all electrical interconnections of the I/C package to the substrate.

Because of the move from through-hole technology, surface mount packages such as Land Grid Array, Ball Grid Array and Column Grid Array have evolved. Ball grid and stud grid array are intended to be close or soldered to the surface. The land grid array may also be soldered; however, in most instances it is a pressure bondable interconnection system that works well for connectors and other electrical and electronic parts.

The spacing of matrix or grid output lands is more forgiving than in the fine pitch peripheral type packages; therefore, the processes are achieving a higher yield (less solder bridging or solder skipping).

Area array packages offer some high density interconnection concepts without the penalties of density pitch. Six-sigma soldering can be achieved although proof through visual inspection is not possible. The desire to do visual inspection could be a detriment to future acceptance of the array type packages in either Ball Grid Array, Column Grid Array or Land Grid Array formats.

3.1.2 Peripheral Ledged Device Packages

Peripheral device packages are semiconductor device packages with terminals extending from one or more of the four sides of the package. The leads are formed in a shape that is compatible with printed board surface mount land pattern. Historically, the device packaging has been an evolutionary process that depends heavily upon the installed manufacturing base, materials, infrastructure of assembly equipment and cost effective piece-part suppliers. Peripheral lead packaging is most effective for smaller parts with a low lead count.

3.1.3 Component Marking

Most semiconductor I/C Packages are marked with a company logo and part number identification. The marking characteristics are extremely important and many times are related to the company who makes the part. The marking is significant advertisement that the product belongs to a particular company. Part number identification provides correlation to ordering or replacement of the part.

In addition, if the part family meets a standard such as defined by the Joint Electron Device Engineering Council (JEDEC), many times the registered and standard outline for the solid state and related product is identified by its particular standard number. Thus, as an example MS-016 might indicate that a particular part meets a standard outline. This assists in the evaluation of the land pattern in which the part belongs.

Another important element of marking is the location of pin #1 in the package device. The Peripheral packages many times have pin #1 identified with a small circle. Sometimes these marks are molded into the plastic body, thus assisting in the inspection and identification of properly placed and interconnected devices.

Sometimes, pin #1 is located in the center of the package, sometimes pin #1 is in one of the corners. In any event, this is an important piece of information. In addition to part number, there is usually an index area that may also be associated with the pin #1 marking. A similar condition exists for the Area Array Packages. In many instances, pin #1 is located in one of the corners. Figure 3-2 shows the difference between Peripheral and Area Array markings, and the pin wire bonding sequence from the point-of-origin.

3.2 Component Materials

The material and process technology steps used to manufacture or assemble the basic types of component packages differ only in detail. Package families in area array or peripheral format provide the functional specialization and diversity required for the user.

Material and construction attributes of individual family members are provided by the following package technologies:

- Cofired (Multilayer) Ceramics
- Pressed Ceramic
- Molded Plastic
- Laminated Printed Board

Not all combinations of package families (form, fit, function) and package assembly technologies are available in all forms. Nevertheless, multilayer structures have used the laminated ceramic approach in many products, as this has been most beneficial for leaded and leadless chip carriers and for various aspects of the array packages as well.

When single layer interconnection is feasible, pressed ceramic and molded plastic are used for the package family. This is normally accomplished in the leaded type packages; however, with the advent of the array packages and the SMT format, new ideas are being explored that use both single layer and multilayer organic substrates in the pressed and the molded plastic family.

In some cases, Ball Grid Arrays are being packaged using standard organic material substrates, such as BT resin or modified polyimide interconnection substrates systems and glass reinforcement. These standard printed board technologies provide a coefficient of thermal expansion

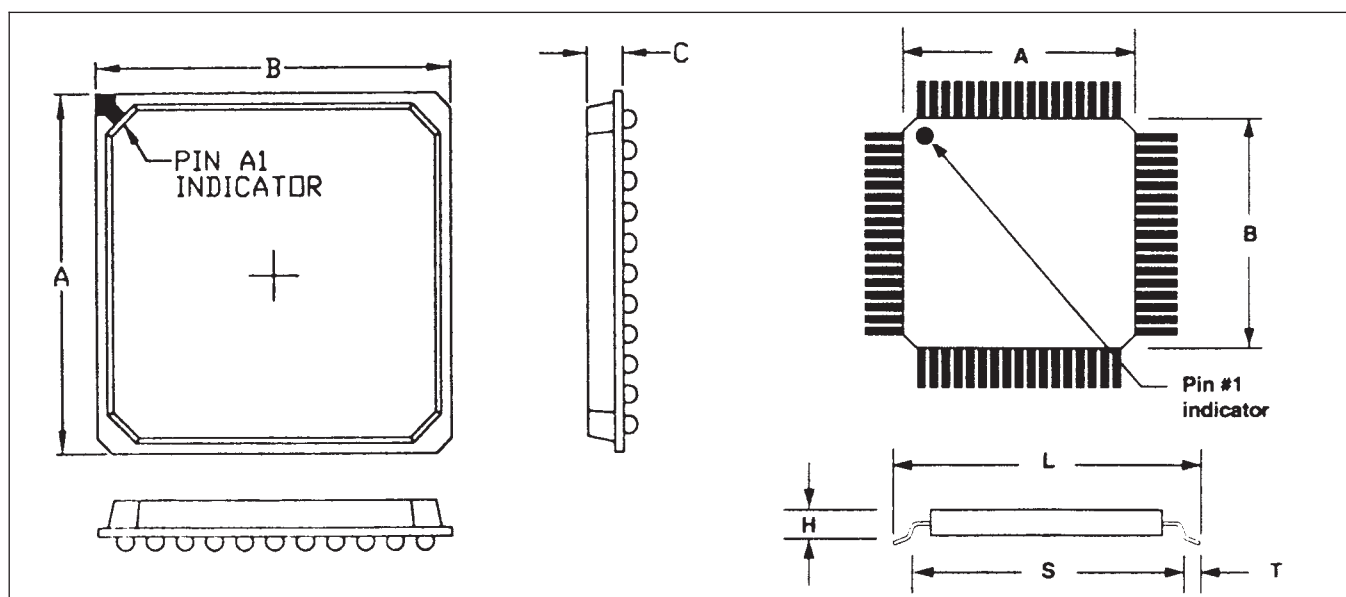


Figure 3-2 Example of Device Package Marking

between that of the component and the interconnecting structure resulting in a greatly reduced CTE mismatch.

During the development phase of the interconnecting strategy, it is important to consider all the variables such as temperature, material characteristics, package moisture content and package reliability under environmental stress due to the materials selected.

Component materials must be completely characterized before introduction to the assembly production line. Many experiments are necessary in the validation stage to provide cost-effective manufacturing processes.

3.2.1 Ball/Column Termination

The solder balls or solder columns form the electrical and mechanical bridge between the area array package and the next level assembly. The solder absorbs the stress between the package and the next level assembly caused by variations in the relative thermal expansion rates.

The solder composition of the area array bumps varies according to required mechanical and thermal properties. Common solder compositions include:

- 90 Pb–Sn
- 97 Pb–Sn
- 63 Sn–Pb
- 50 In–Pb
- 95 Pb–Sn

3.2.1.1 Bump Preparation

Bumps can be assembled into a solder-mask-defined area. They may be separately produced and attached through a fusing process, or they may be deposited and fused to form the round shape.

Usually a ball mask is attached to the underside of the part, and the bumps are plated to the size required where they represent a truncated cone, and a reflow process causes the final round diameter shape.

Electrodeposition offers a wider range of Sn-Pb compositions than evaporation and thus affords greater control over mechanical and thermal properties. Electrodeposition also produces smaller diameter balls.

A variety of solder paste compositions can be screen-printed. Here bumps are reflowed at lower processing temperatures, and improved compliance and failure life in some instances may result.

3.2.2 Termination Leads

Leads emanate from the I/C package and peripheral packages and must be formed in order to meet the final configuration. Lead forming is a two-fold assembly operation that bends and trims plated or solder dipped-leads to meet specified dimensional accuracy. Leads can be formed into three standard configurations: gull wing, “J” leads for sur-

face mount packages, and straight form for through hole mounting. During the forming process extreme care is taken to expose the tin plating or solder coated leads to minimum stress and abrasion, thus ensuring maximum strength and reliability.

The lead finishes used on component packages are usually one of five basic lead finishes. These are:

- gold plate
- tin plate
- solder coating
- tin-lead plate
- palladium plating

Each type of lead finish offers advantages for specific applications and for internal and external processing.

3.2.3 Plating and Coating Technologies

3.2.3.1 Gold Plate

The gold plate finish is recommended for socket applications only. The packages most often involved are the ceramic laminated family, including pin grid arrays (PGA), side brazed dual-in-lines and its other cousins.

At one time gold was considered a universal superior lead finish because of its solderability and electrical and non-oxidizing properties. However, it has been determined that soldering gold-plated component leads directly into printed circuit boards has some clear disadvantages.

Excess gold in solder joints can result in the formation of a brittle alloy, causing the joints to fail over time and under high-vibration or board-flexing environments. Currently, requirements demand that a solder coat replace gold and direct soldering used for both leadless and leaded components. Gold plating remains the lead finish of choice however, for socketed units.

3.2.3.2 Tin Plate

Some leaded components are offered with tin plating. This is usually for selected ceramic type leaded packages. The tin-plating finish can be either directly soldered or socketed with non-gold socket contact finishes.

Tin offers the advantage of a slightly higher melting point (232 °C) than solder (180 °C), and it can be burned in at higher temperatures without melting. However, when compared to solder coating, tin plating does not age as well in long term storage from the stand-point of solderability. This may occur because tin plating is more porous than solder coating. In general, pure tin plating is more susceptible to tin whisker growth under certain mechanical and environmental conditions.

3.2.3.3 Solder Coat

Solder coat component leads offer the distinct advantage of the low melting point (183 °C), and resistance to aging. A

typical composition of solder coat is the eutectic alloy of 63% tin and 37% lead.

Base coatings are normally applied in the following sequence:

1. Clean the leads
2. Apply flux
3. Dip the leads into molten solder
4. Finish with hot water rinse.

Great care is taken to minimize any thermal shock to the package and die during solder joint processing and cleaning of the unit after coating.

The solder coat lead finish is usually available to most of the plastic and ceramic package family formats as well as all military packages. Solder coat lead finish is compatible with many types of assembly processes including wave soldering, infrared, hot air, and vapor phase reflow solder technologies.

3.2.3.4 Tin-Lead Plate

Tin-lead alloy is used extensively for plating leads. The plated elements, when reflowed, form an alloyed composition of approximately 85% tin and 15% lead, or 63% tin and 37% lead. The plating on the packages' copper lead frames, with the thickness of 5 μm minimum, provides full coverage of the copper without exposing any formed intermetallics to air. At the same time, solder plate produces a very solderable finish with a melting point for the 85/15 approximately 220 °C and for the 63/37 approximately 183 °C.

Leads plated with tin-lead alloy can be directly soldered using conventional reflow. Some products may also be socketed.

3.2.3.5 Palladium Plate

A palladium plated lead is composed of a copper base metal, a layer of nickel and a very thin layer of palladium. The key role of the palladium is to protect the underlying nickel plate from oxidation during the assembly process, as well as storage prior to use. Also, since the stitch bond is made directly to the nickel surface, through the palladium, instead of to silver, all silver is eliminated from the package. This eliminates the risk of silver migration causing extraneous electrical contacts.

Since palladium has a more consistent plating thickness, the advantages of fine pitch (0.5 mm or less) packaging becomes more obvious. The user can more accurately control the solder volume in the joint, thus solder bridging control is more easily obtained.

3.2.4 Process Comparisons

The information in figure 3-3 illustrates the process steps that usually occur for leads that are solder plated vs. those

leads that have been solder coated. As can be seen from figure 3-3 there are several more steps in the solder coat process.

SOLDER PLATE	SOLDER COAT
Package Assembly	Package Assembly
Fixturing	Fixturing
Pretreatment	Pretreatment
Rinse	Rinse
Plate	Dry
Rinse	Fluxing
Dry	Preheat
Quality Assurance	Solder Coat
	Cool
	Rinse
	Dry
	Quality Assurance

Figure 3-3 Solder/Coating/Plating Process Comparison

3.2.5 Plastic Packages

The molded plastic package is normally a package made up of a copper alloy or alloy 42 lead frame, silvered-filled polymeric die attached adhesive, the silicon chip, gold bonding wires, and epoxy molding compound. Each of these components has a unique set of physical properties. The varying coefficients of thermal expansion present a challenge to maintain mechanical integrity of the bulk materials and interfaces between them.

Because of the different rates of expansion and contraction, stresses concentrate at the interfaces between materials during the temperature excursions typical of accelerated reliability testing and circuit-board mounting. When these stresses exceed interfacial strength between materials, loss of adhesion can occur. The presence of absorbed moisture in the molding compound exacerbates this phenomenon.

In order to prevent failure of the encapsulant during processing, testing, and end use, many different approaches are taken. From the material perspective, the supplier of the molding compound synthesizes the polymer to exhibit minimum moisture absorption. In addition, coupling agents are used to maximize adhesion between the epoxy matrix and silica filler to limit moisture ingress.

Optimization of other material properties such as flexure strength, module and toughness, ensures that the material can perform under severe moisture and temperature cycling conditions without the occurrence of cracking, which can lead to ingress of corrosion-causing contaminants. The molding compound contains the elastomeric toughening agents that curtail the growth of cracks, should they begin. These low stress materials also provide protection to the fragile chip surface for preventing cracking and shear

deformation of the thin film structures that make up the circuitry.

Careful package and process designs also ensure integrity of the molded package. Package engineers employ design features that provide robustness to the component by creating mechanical locks between the molding compound and chip lead frame. The material flows are designed to maximize adhesion and limit exposure to moisture during the manufacture, shipping and board mounting of the component.

3.2.6 Ceramic Packages

Ceramic packages are normally used when hermetic sealing is required. Hermetic sealing of I/C packages is used to seal the silicon electronic component from the external environment, specifically from water vapor and contamination that can shorten the lifetime of sensitive electronic devices.

3.2.6.1 Metal-filled Ceramic Packages

Two types of hermetic seals are normally used. One uses a hard solder precious metal brazing alloy (laminated ceramic package family) and the other a low melting-temperature glass (pressed ceramic package family).

The metal-sealed packages are of the laminate ceramic type and involve the brazing of a metal lid to gold-plated thick film seal ring on the ceramic. The glass-sealed packages utilize glass to create the seals between the pressed ceramic piece parts. The hermeticity of various sealing materials shows that metals provide the longer life time seal or impermeability, where as epoxies and silicon show the lowest opportunity for those characteristics. Thus, metal seals provide the highest level of hermeticity followed by glasses and ceramics.

The metal-sealed packages utilize a gold-tin eutectic hard solder to create the hermetic seal. The composition of the alloy is 80% gold and 20% tin and has a melting point of 280°C. This solder is chosen for its excellent wetting characteristics to the seal ring and lead materials, and is highly resistant to thermal fatigue. Seals created by the Au-Sn as well as its tin alloy can withstand thousands of thermal cycles without failure.

The gold-tin eutectic seal is made to a seal ring in the surface of aluminum oxide ceramic. The seal ring is composed of a tungsten thick-film that is fired to the ceramic material and plated with a thin nickel diffusion barrier and a gold over-plate. The gold over-plate prevents oxidation and provides a wettable surface for the solder.

The lid material is a gold-plated alloy 42 (a nickel-iron alloy with low thermal expansion) to which is attached an 80% gold and 20% tin alloy (eutectic composition) preform. The seal preform is attached by spot welding. The lid

material is chosen for its stiffness and because the thermal expansion of alloy 42 is close to that of aluminum oxide ceramic.

3.2.6.2 Glass-Sealed Ceramic Packages

In glass-sealed packages, a ceramic lid is sealed to the base ceramic with a vitreous (non-crystallizing) lead based glass having a low melting temperature. The glasses chosen for hermetic sealing are lead-zinc borates that generally seal in the 415/450 °C range.

The glasses used in the industry have compositions in this range, with the final selection based on obtaining the lowest possible processing temperatures. As a result, the most commonly available seal glasses have very similar compositions. The glasses are highly resistant to chemical plating baths and have excellent thermal shock resistance. The variety of the glass that is used for package sealing also has high thermal expansion capability relative to the ceramic. To reduce thermally induced package stresses, it is necessary to reduce the thermal expansion of the glass by adding lower temperature expansion fillers. These fillers are chosen to be compatible with the lead glass and do not react during processing.

Because glasses all have similar composition, they have similar strengths. The glass used most often can be seen to have bending strength equivalent to other commonly used glasses. The fractured toughness is also found to be quite similar. It is expected that mechanical performance of sealed glass will be equivalent to other commonly used glasses.

3.2.7 Die Attach

Die attach is an important part of the component assembly process that ensure the parts performance requirements for the user. There are usually two types of die attach materials: adhesives (organic and in-organic) and hard solders (gold-silicon eutectic).

The choice of die attach materials depends on the specific applications and is compatible with the particular packaging technologies to insure the highest level of performance and reliability. Table 3-1 shows the relationship between the various packages and the die attachment material used and its type.

3.3 Heat Dissipation Techniques

Thermal management of the electronic system encompasses all the thermal processes and technologies that must be utilized to remove and transport heat from individual components to the system thermal sink in a controlled manner.

Thermal management has two primary objectives. The first is to insure that the temperatures of all components are maintained within both their functional and maximum

Table 3-1

Package	Die Attachment	Material Type
Pressed Aluminum Ceramic (Cerdip, Cerquad)	Silver-Filled Glass	Inorganic Adhesive
Laminated Aluminum Ceramic (PGA, CQFP, Side Brazed)	Gold Silicon Eutectic Silver-filled Cyanate Ester Silver-filled Glass	Hard Solder Organic Adhesive
Molded Plastic (Alloyed 42 Lead Frame)	Silver-filled Epoxy	Organic Adhesive
Molded Plastic (Copper Lead Frame)	Silver-filled Epoxy	Organic Adhesive

allowed limits. Functional temperature limits provide the temperature range within which the electrical circuits are expected to meet their specified performance requirements.

Operation outside the range may result in degraded machine performance or logic errors. The maximum allowable temperature limit is the highest temperature to which a component or part of a component may be safely exposed. Operation above the allowable temperature limit may result in actual physical destruction of the component or irreversible changes in its operational characteristics.

The second objective of thermal management is to ensure that distribution of component operating temperatures satisfies reliability objectives. Although failure to meet this objective may not be as readily apparent as failing to remain within maximum temperature limits, in the long run it can be equally costly.

Failure mechanisms encountered in electronic components are kinetic in nature and depend exponentially on device operations temperatures. The exact relationship between failure rate and temperature depends upon the packaging materials and processes and the failure mechanism in operation. This relationship can be illustrated (for changes in device characteristics resulting from chemical or diffusion processes) by using a normalized failure rate equation.

Relative heat flux levels of various devices and natural phenomena are shown in Figure 3-4. As seen from the figure, the heat flux at the die level is only about two orders of magnitude less than that on the surface of the sun. But the sun's surface temperature is 6000 °C, compared to a maximum chip operating temperature of 100°C for typical semiconductor devices. The challenge of thermal design is to continue to maintain die temperatures at acceptable operational temperature levels regardless of the increased power density. Operation of a device outside the specified temperature range can result in degraded machine performance or logic errors. Failure rates increase by a factor of two for every 10 °C increase in operating temperature;

therefore, reliability concerns are a significant factor in thermal design.

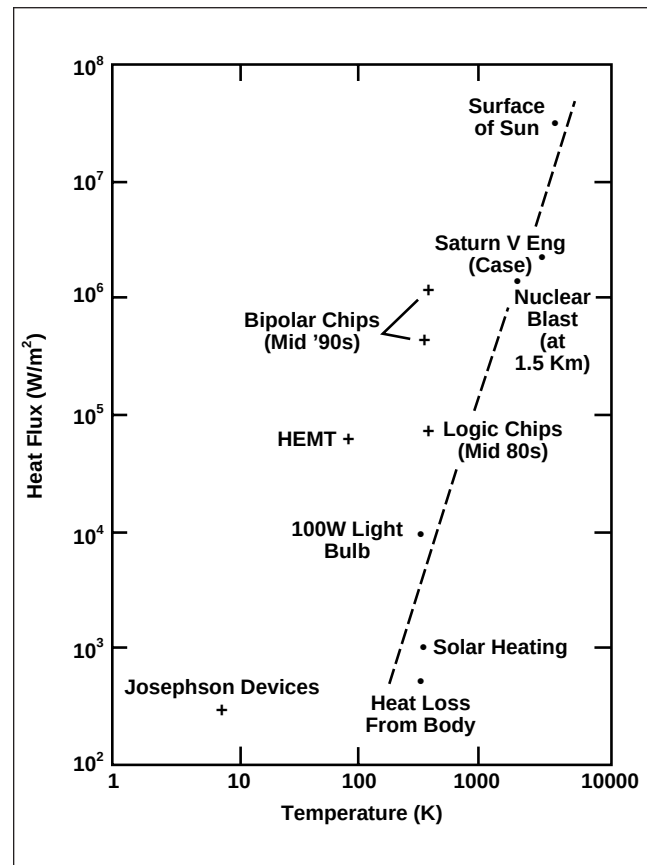


Figure 3-4 Temperature Differences Attainable as a Function of Heat Flux

Heat transfer through a given package can occur in various modes depending on the system environment. In mobile systems, fans are not typical and the heat must be dissipated from the component through heat flow channels that are narrow. In desktop environments, typically a system fan and a power supply fan exist and low air flow levels can be expected to aid more in the cooling process. In servers, additional degrees of freedom are available to provide room and increased airflow to address higher power dissipation.

The cooling technology selection must be made at an early stage of the design. Shown in figure 3-5 is a map that reflects the temperature difference necessary to support dissipation of heat (heat flux is defined as heat per unit exposed surface area of the package) to cooling technology assuming no enhancements have been made to the package (e.g., by addition of heat sink).

The temperature mapping in figure 3-5 can be used as a rough estimate to provide the designer with a starting point so that thermal requirements be accommodated in the design.

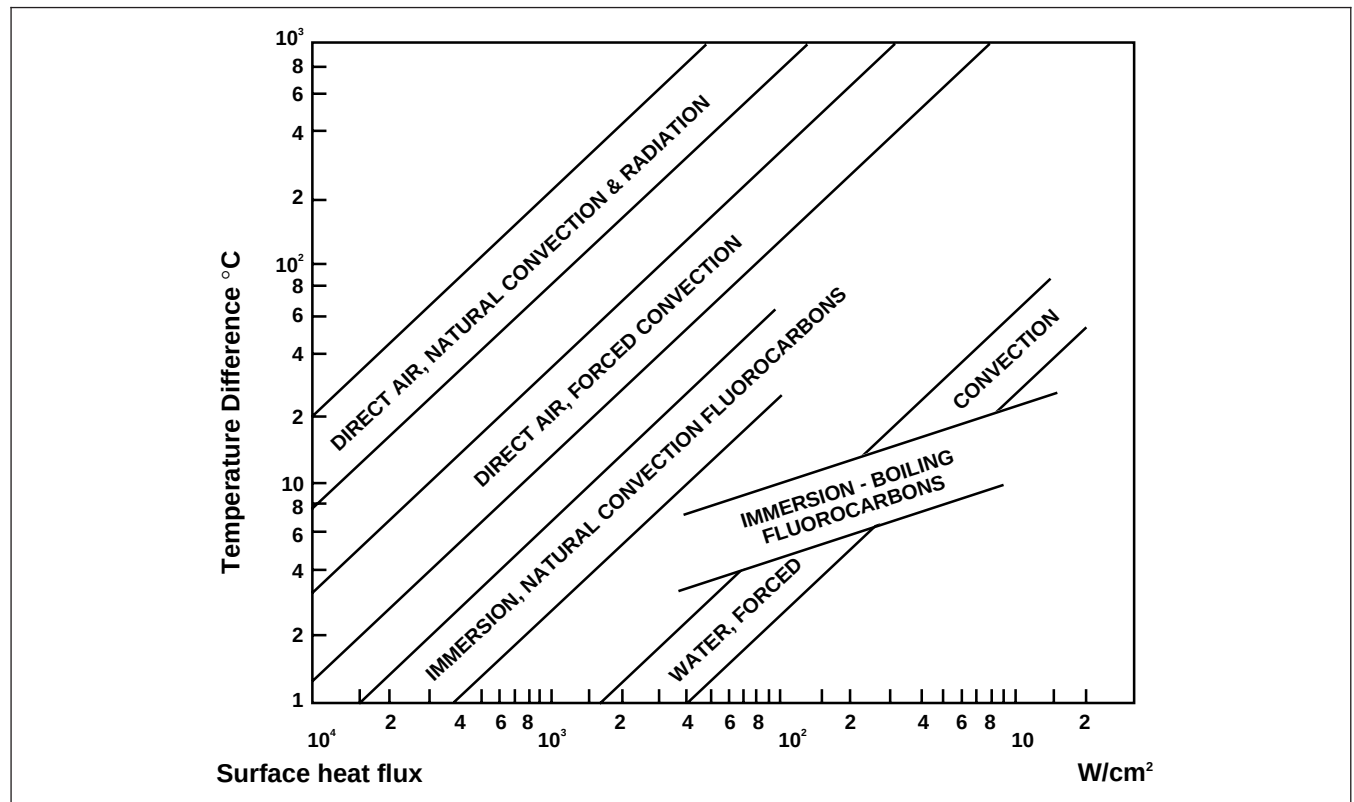


Figure 3-5 Heat Flux vs. Temperature Level

Example: Assume that it is necessary to determine the mode of cooling that would be appropriate for a 25 mm x 25 mm x 1.75 mm package (body only) dissipating 1.2 watts. The case temperature is to be maintained at 85 °C and the air temperature in the vicinity is expected to be 45 °C. The temperature difference available for cooling is $(85 - 45) = 40$ °C. The package of size has an approximate surface area of 8 cm², (including top surface area plus the four sides of the package); the bottom surface does not participate as it is not exposed to any cooling medium.

Package heat flux = $1.2/8 = 0.15$ W/cm².

Then from figure 3-5 using 40 °C and a flux of 0.15 W/cm² it is easy to see that this part can be cooled by air under natural convection environment.

It must be noted that these estimates are based on gross simplifications and refinements are necessary in the later phases of implementation.

Heat transfer from a package assembled onto an interconnecting structure (e.g., printed board) can occur through various modes. These are described in the following paragraphs.

3.3.1 Conduction

Conduction is a process by which heat flows from a region of higher temperature to one of lower temperature within a medium (solid, liquid or gas) or mediums in direct physi-

cal contact. Multilayer printed boards with metal cores are an excellent way to remove the heat from the component. Thermal vias are positioned under the component and provide the thermal path to the heat sinking planes.

The fundamental feature of conduction is the transmission of thermal energy by direct molecular communications without appreciable displacement of the molecules.

In a one dimension form the Fourier law governing conduction can be represented by:

$$q = kA \Delta T/L$$

where: q = Heat flow rate (W)
 k = Material thermal conductivity (W/m°C)
 A = Cross sectional area (m²)
 $\Delta T/L$ = temperature gradient (°C/m)

The temperature difference resulting from the flow of a specified heat rate from a fixed cross section is thus related to the thermal conductivity of the material (k) and the path length (L). From an electrical analogy, if q and ΔT represent current and voltage respectively, L/kA is thermal resistance of the conduction path. While packages are made of a wide variety of materials and shapes, the process of heat dissipation from the junction to the surface(s) of the package is by conduction.

While the manufacturer sets the maximum or junction temperature limits, the component mounted on a board needs

to have a microenvironment that can satisfy the necessary condition for thermal control. Components are typically cooled by air and the heat transfer phenomenon for cooling the case of a package is described by convection.

3.3.2 Convection

Convection is a process of energy transport by the combined action of heat conduction, energy storage and mixing motion. It is a complex mechanism of energy transfer from a package surface to surrounding air. This process takes place in several steps. First, heat will flow by conduction from the package surface to immediate adjacent air molecules. The energy thus transferred will increase the temperature and internal energy of the air molecules. Due to the ability of air molecules to move more freely, the heated air molecules will move to a region of lower temperature of air where they will mix with the colder air and transfer part of their energy to the colder fluid molecules. Note that unlike conduction, the flow in this case is of air as well as energy. The heat energy transferred from the package surface is stored in the fluid and is carried away as a result of mass motion. The effectiveness of heat transfer by convection depends largely upon the mixing motion of the air. The simplified relationship that captures this phenomena is commonly referred to as Newton's law of cooling as given below.

$$q^c = hcA(T_s - T_a)$$

where: q^c = convective heat flow rate from surface to ambient (W).

Δ = surface area (m^2)

T_s = Surface temperature ($^{\circ}C$)

T_a = Ambient temperature ($^{\circ}C$)

h^c = average convective heat transfer coefficient ($W/m^2^{\circ}C$)

The above equation recast into an electrical analogy form results in the convective resistance definition as $1/h^cA$.

The role of convective heat transfer in keeping the package surface at the desired temperature is extremely important as it is the ultimate sink for the heat dissipated from the component. Observe in the definition of the resistance, the effect of the surface area of the package. In order to maximize the efficiency of heat removal from the package surface, the product of the heat transfer coefficient and the surface area has to be maximized. The determination of h^c requires the knowledge of fluid flow and is the focus of thermal research. The typical range of heat transfer coefficients as a function of fluid choice is presented in Table 3-2. Note that although the magnitudes for air are not as high as in liquids, the ease of use combined with simplicity in design promotes the use of air cooling as the primary mechanism in personal computers.

In the absence of a system fan to force air through, air still

participates in the cooling of the packages via the convection currents set up due to density differences that arise in hot and cold air. This process is called natural convection. Under natural convection conditions, orientation of the heated surface with respect to gravity plays a significant role in the cooling. In general vertical surfaces are to be preferred to horizontal orientation. The heat transfer coefficient indicated above encompasses the natural convection regime.

3.3.3 Radiation

Thermal radiation is defined as the radiant energy emitted by a medium by virtue of its temperature, without the aid of any intervening media. The physical mechanism of radiation is not completely understood. Radiant energy is sometimes envisioned to be transported by electromagnetic waves, at other times by photons. Neither viewpoint completely describes the nature of all observed phenomena. The amount of heat transferred by radiation between two bodies at temperatures T_1 and T_2 is governed by the following expression:

$$q = \epsilon \sigma (T_1^4 - T_2^4)$$

where q = amount of heat transferred by radiation (W)

ϵ = emissivity ($0 < \epsilon \leq 1$)

σ = Stefan-Boltzman constant, 5.67×10^{-8} (W/m^2K^4)

A = area (m^2)

F_{12} = Shape factor between surfaces 1 and 2 (A fraction of surface radiation seen by surface 2)

T_1, T_2 = surface temperatures of radiating surfaces

While radiation is an important cooling for space vehicles, natural convection environments can also benefit from radiation. To estimate the magnitude of radiational cooling to the convective cooling described earlier a radiation heat transfer coefficient can be calculated as follows:

$$h_r = \epsilon \sigma F_{12} (T_1^2 + T_2^2) (T_1 + T_2)$$

It is not uncommon to find the radiational contribution to be of the same order as convective cooling especially in natural convection cooled packages. Oversight of this aspect can result in expensive over-design of equipment. Note that the radiational process is nonlinear and the above definition of h_r linearizes the phenomenon and is applicable within moderate temperature ranges.

3.3.4 Thermal Impedance

The complex material tradeoffs for different package families makes it rather difficult for analyzing component details by simple 1D conduction analysis. In order to provide data for a wide variety of packages, the industry has adopted lumping the effects of materials within the package

Table 3-2 Transfer Coefficient as a Function of Fluid Choice

Primary Cooling Mechanism	Typical HTC Range (W/m ² K)	Relative Effectiveness	Achievable Density	Complexity of Implementation
Natural Convection(air)	10	0.1	Low	Very Low
Forced Convection (air)	100	1.0	Medium	Low
Natural Convection (liquid)	100	1.0	Medium	Medium
Forced Convection (liquid)	1000	10.0	High	High
Boiling (liquid)	5000	50.0	High	High

by defining thermal impedance values. Under identical conditions, the package with lower impedance value provides a better thermal solution. The most commonly used ones are defined by the following relations:

$$\begin{aligned}\Theta_{ja} &= (T_j - T_a)/P \\ \Theta_{jc} &= (T_j - T_c)/P \\ \Theta_{ja} &= \Theta_{jc} + \Theta_{ca}\end{aligned}$$

where:

$$\begin{aligned}\Theta_{ja} &= \text{Junction to ambient thermal resistance (}^{\circ}\text{C/W)} \\ \Theta_{jc} &= \text{Junction to case thermal resistance (}^{\circ}\text{C/W)} \\ \Theta_{ca} &= \text{Case to ambient thermal resistance (}^{\circ}\text{C)} \\ T_j &= \text{Maximum die temperature (}^{\circ}\text{C)} \\ T_c &= \text{Case temperature at a predefined location (}^{\circ}\text{C)} \\ P &= \text{Device power dissipation (W)} \\ T_a &= \text{Ambient temperature (}^{\circ}\text{C)}\end{aligned}$$

As can be seen from the above definitions, the various resistances are derived from experimental measurements. For the characterization of packages, temperature-sensitive parameter (TSP) method is most common. This method uses special test structures cut to the same size as the actual device, consisting of resistors and diodes. Resistors are used to simulate the device power dissipation, and the diodes located at different points on the chip surface provide junction temperature data. It is important to recognize that the lumping process of all the materials in a package requires that the location of the measurement of the case temperature be specified.

For single device packages, the manufacturer typically identifies the predominant heat flow path from the packages and chooses a location to identify the heat flow path. For example, in the case of cavity-down PGA packages the center of the top surface yields the highest case temperature. However, a cavity-up package at the same location would result in lower temperature due to the longer path to the device.

Another variable of importance is the definition of ambient temperature. For the data that is measured in air, it is typically defined as the unchanging temperature at a distance away from the package test section. Component data in earlier days have reported using a constant-temperature agitated bath. The applicability of such information to air cooled system environment is poor. In using component

level data, the applicability of test conditions to the end user conditions should be carefully evaluated. The best source of data is one that replicates both the mounting configuration of the user and the airflow environment.

The data pertaining to the junction-to-case thermal resistance provides the end user with lumped effects of the material properties of the package and considerably decreases the need for detailed level models of conduction paths at the board and system level analysis.

3.3.5 Component Level Thermal Characteristics

The component provided by a manufacturer can be utilized in a variety of environments, and it is not possible for the vendor to provide data relating to all application configurations. However, certain information in the form of impedances are provided. These are typically provided both under conditions with still air and air velocities that cover a broad spectrum. As indicated in the description of the convection process, the area of a package has a significant impact on the thermal resistance of a package.

Shown in figure 3-6 are the typical junction-to-ambient resistance for different package families as a function of lead count. Note that packages of smaller size and made of lower conductivity material have higher resistance to heat flow under identical conditions. Observe that for a given package type, the thermal resistance decreases as the package size grows. The package resistance also serves the purpose of assisting the designer in evaluating package alternatives for the same function. Indirectly, given an environment in a system (e.g. fan-less system) one can use the thermal characteristic to determine to the first order whether the power dissipated by the component can be handled without addition of heat sinks or an alternative package style with better performance can be selected.

Package styles are numerous and the heat flow paths from the die are essentially different on each one of them. Use of copper lead frames, spreaders and slugs influence the package characteristics. In the use of data published by the component manufacturer, the effect of board conductance on the measurements provided, must be considered.

This is particularly important for fine pitch parts with copper lead frames. Based on layer count and copper content

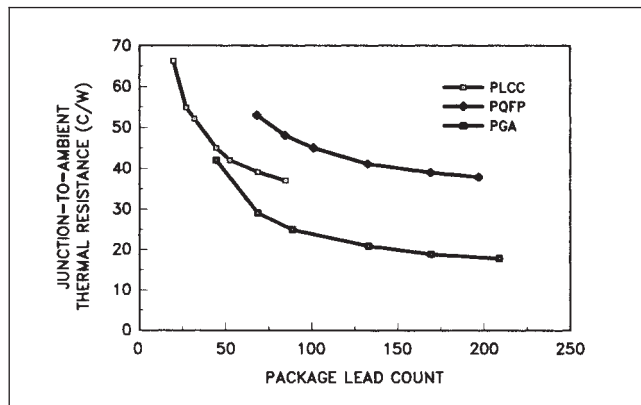


Figure 3-6 Effect of Package on Thermal Resistance of PLCC, PQFP, and PGA Packages

in the board the effective thermal conductivity can be computed for a specific design. Shown in figure 3-7 is the effect of board conductivity on the measured thermal resistance for PQFP package. As the effective board conductivity increases, the spreading resistance through the board reduces and the board participates to an increasing level in the heat removal from the package.

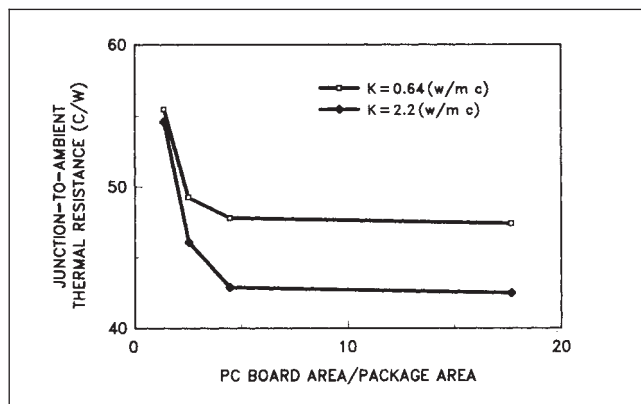


Figure 3-7 Effect of PC Board Material Size on Thermal Resistance of 132-Lead PQFP

Airflow tends to decrease the Θ_{ca} (i.e. the external resistance) and tends to have minimum influence on the internal resistance of the package. Such data is commonly published for a wide variety of packages in the vendor's data book. The data for a 168 lead cavity down package is presented in figure 3-8. In some cases, resistance values with heat sinks attached to the part are also presented. A well designed heat sink in conjunction with interface (attach material) can reduce the external resistance of the package by decreasing the external case-to-ambient resistance. This allows the designer to dissipate additional power from a device while maintaining the device temperature within prescribed limits. However, the penalty is increased volume. While data typically extends to high air flow rates, the acoustic limits established at the system level do not normally permit high air velocities to be attained.

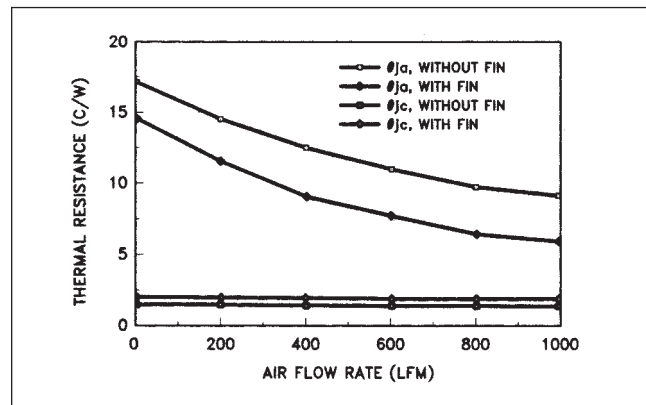


Figure 3-8 Effect of Air Flow Rate on Thermal Resistance of 168-Lead PGA Package

3.3.6 Board Level Thermal Management

In the context of a system, the various components are assembled to establish a board level product. In moving from a component level description to a board level analysis, the environment in which the board is employed has a major influence on the thermal design. To address the need for increased functionality, the separation distance between components is kept to a minimum within manufacturing limits. This is a sharp contrast to the test configuration in which individual packages are characterized.

For natural convection environments the local effects play a major role. Factors such as separation of cards and the inlet vents and orientation result in differing case temperature values for a given board. Recirculation patterns result in complex flow and thermal interactions when combined with nonuniform package geometries, and power dissipation is not amenable to generalized calculations. However, the correlations for plates having uniform spread out loading can serve as a rough guide to calculate temperature and heat transfer capabilities.

It must be noted that these correlations do not include the effects of radiation. It is often instructive to compute radiational contribution of the heat transfer coefficient to ascertain that an important effect is not ignored. Normally the radiational heat transfer between identical boards placed parallel and powered on (close approximation to the system's card environment) is minimal, as the temperature difference between the boards is negligible.

3.4 Handling and Storage

3.4.1 ESD

Electrostatic Discharge (ESD) protection is essential for handling almost all high performance packages. Damage to sensitive devices can result from failure to control the static electricity generated in simple human and machine movements. High voltages, in excess of 5,000 volts, can be generated by the rubbing of common materials: wood, plastics,

fabrics, in normal activities on the manufacturing floor. This electrical charge must be controlled because many components can be damaged by as little as 30 volts.

The threshold voltage where ESD damage can be sustained by a device has been divided into five categories by the Electrical Overstress/Electrostatic Discharge Association, Inc.

- Class 0** 0 to 199 volts
- Class I** 200 to 499 volts
- Class II** 500 to 1999 volts
- Class III** 2000 volts and above
- Class IV** no ESD sensitivity

Most high performance packages require class 0 ESD protection. The device manufacturer defines the ESD constraints on the device, and an ESD specification should be provided with the product data.

A standard symbol for ESD protection requirements, a hand superimposed on a triangle with a yellow/black format, provides universal recognition of this surface mount process requirement. The ESD Class can be printed on the hand near the wrist. This symbol can be used to identify areas and process machinery that must be ESD protected. Use of the symbol on the components is desirable, but marking space constraints often preclude this practice.

Printed board assemblies, containing electrostatic sensitive components (ESD) are marked with the circular symbol containing three inward pointing arrows. The ESD symbol may be marked or screened, using a permanent ink or label, able to withstand assembly processes, or etched in copper on the printed board. (See figure 3-9)

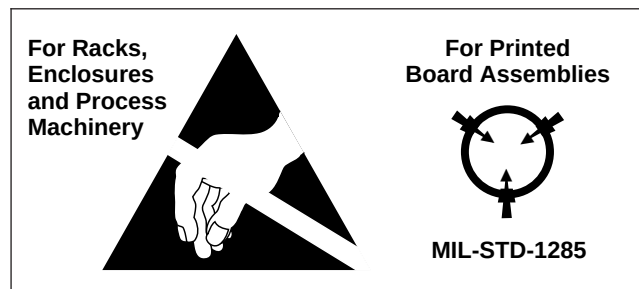


Figure 3-9 Standard ESD Symbols

3.4.1.1 ESD Control

ESD control consists of bleeding off any electrostatic charge through conductive paths to ground in all portions of the process equipment, part containers, and in the human interface. Many areas of the process equipment must be altered in construction or provided with a surface treatment to provide a conductive path for static charges. Air ionizers strategically located in the process area reduce static build-up. The human interface is a significant problem due to the static generating nature of most clothing, shoes, etc.

Control devices include static dissipative jackets or suits, grounding foot straps or foot wear, conductive floor finish, and wrist straps electrically connected to ground. It is preferable to have static dissipative (10^5 to $<10^{12}$ ohms per square) surface resistivity rather than conductive surfaces (0 to $<10^5$ ohms per square). Conductive surfaces may contribute to component damage by providing an excessively rapid discharge of an electrostatic charge. It is preferable to have the component in contact with static dissipative surfaces during handling, storage, and assembly. In addition, maintaining a moderate room humidity (30% to 50% R.H.) promotes static dissipation.

Measurement of ESD parameters is essential for working with sensitive components. Tools required for monitoring ESD include the electrostatic field meter that detects and measures the voltage and field strength associated with static charges on equipment, materials, and people. Additional testing is performed with surface resistivity meters to determine effectiveness of ESD coatings on equipment and facilities, charge plate monitor to evaluate air ionizers, and a personal grounding tester to measure the effectiveness of ESD protective equipment worn by personnel in the area.

All personnel in the area should receive training that describes the nature of ESD damage, the procedures necessary to prevent this damage, and care to be taken in handling sensitive components. One or more persons should be assigned to monitor the ESD control activities, procedures, training, and equipment for the production facility. This person or committee must have the responsibility and authority to enforce ESD controls.

3.4.1.2 Shipping Media

ESD-sensitive components must be shipped and stored in ESD-approved static dissipative containers and packing materials. The package must be opened on a static dissipative surface and ESD-controlled area. Components should be removed from the container with proper regard to ESD control in the work surface, containers, implements, and personnel. (See EIA-583 and EIA-541)

Proper labeling on shipping containers must be an essential part of the contract between the supplier and user. Internal part numbers, if used, must be assigned and clearly labeled at incoming inspection. Transfer of the part identification from the stock location, reel, tube, or tray to the feeder location on the process equipment is a prime source of error. Requiring that a second person check and sign off on all stock room transactions, machine set-ups, and part handling activities has proven effective in controlling these errors.

Moisture-sensitive components must be shipped in sealed moisture-resistant containers with an effective desiccant material included in the package. IPC-SM-786 provides information on handling moisture-sensitive components.