

3.9.1 Bit Wide DRAM

Release 1

3.9.1.1 – 16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES

CAPACITY—16K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
POWER VOLTAGES—VDD=+12 V, VCC=+5 V, VBB=-5 V
PIN ASSIGNMENT—Fig. 3.9.1-1

3.9.1.2 – 16K TO 256K BY 1 DRAM FAMILY IN DIP

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN DIP, 0.3" wide
PIN ASSIGNMENT—Fig. 3.9.1-1

3.9.1.3 – 16K TO 256K BY 1 DRAM IN RCC

CAPACITY—16K, 64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PAD (PIN) RCC, 0.290" by 0.425" (16K & 64K)
—18 PAD (PIN) RCC, 0.290" by 0.490" (256K)
PIN ASSIGNMENT—Fig. 3.9.1-2

3.9.1.4 – 64K & 256K BY 1 DRAM IN ZIP

CAPACITY—64K, 256K WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—16 PIN ZIP
PIN ASSIGNMENT—Fig. 3.9.1-3

3.9.1.5 – 1M AND 4M BY 1 DRAM FAMILY IN DIP

CAPACITY—1M, & 4M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—18 PIN DIP, Width: 0.3" for 1M, 0.35" for 4M,
PIN ASSIGNMENT—Fig. 3.9.1-4

3.9.1.6 – 1M TO 16M BY 1 DRAM FAMILY IN SOJ OR TSOP2

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 1M,
— : 0.3" or 0.35" by .675" for 4M
—26/20 PIN TSOP2: 0.3" by 0.675" and 0.050" PIN PITCH for 4M
—26/20 PIN SOJ OR TSOP-2: 0.3" FOR 16M
—28/24 PIN SOJ OR TSOP-2: 0.4" BY 0.725" for 16M
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC-16.
PIN ASSIGNMENT—Fig. 3.9.1-5

3.9.1.7 – 1M TO 16M BY 1 DRAM FAMILY IN ZIP

CAPACITY—1M, 4M, 16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—20 PIN ZIP, 0.400" WIDE FOR THE 1M & 4M PARTS
PACKAGE—28 PIN ZIP, 0.475" WIDE FOR THE 16M PART
SUPPLY VOLTAGE—The 16M part with an 8K refresh is approved for use with the LVTTL power and interface standard developed by Committee JC-16.
PIN ASSIGNMENT—Fig. 3.9.1-6

3.9.1.8 – 1M TO 16M BY 1 NON-MUX DRAM FAMILY IN SOJ

CAPACITY—1M, 4M, & 16M WORDS OF 1 BIT
LOGIC FEATURES—Non-Multiplexed Address
PACKAGE—28, 32, OR 34 PIN DIP
PIN ASSIGNMENT—Fig. 3.9.1-7

Release 4

3.9.1.9 – 1M BY 1 DRAM IN TSOP1

CAPACITY—1M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—24/20 PIN TSOP1
PIN ASSIGNMENT—Fig. 3.9.1-8

3.9.1.10 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS
LOGIC FEATURES—Configurable as a X1 or a X4 part
—The data access mode can be chosen by logic control
PACKAGE—28 PIN SOJ
PIN ASSIGNMENT—Fig. 3.9.1-9

3.9.1.11 – 64M BY 1 DRAM IN SOJ OR TSOP2

CAPACITY—64M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses
This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.
PACKAGE—34 PIN SOJ, 0.500" Wide
—34 PIN TSOP2, 0.500" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1-10
PACKAGE—32 PIN SOJ, 0.400" Wide
—32 PIN TSOP2, 0.400" WIDE, 0.050" PP
PIN ASSIGNMENT—Fig. 3.9.1-12

3.9.1.12 – 2 X 16M BY 1 DRAM IN TSOP2

CAPACITY—32M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Addresses and Two arrays of 16M x1 with common data pins and separate $\overline{RE}$ & $\overline{CE}$ inputs.
PACKAGE—28/24 PIN TSOP2, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.1-11

3.9.1.13 – 16M BY 1 DRAM IN USON

CAPACITY—16M WORDS OF 1 BIT
LOGIC FEATURES—Multiplexed Address
PACKAGE—28 PIN USON, Width: 7.0 mm, 0.8 mm Pin Pitch
PIN ASSIGNMENT—Fig. 3.9.1-13

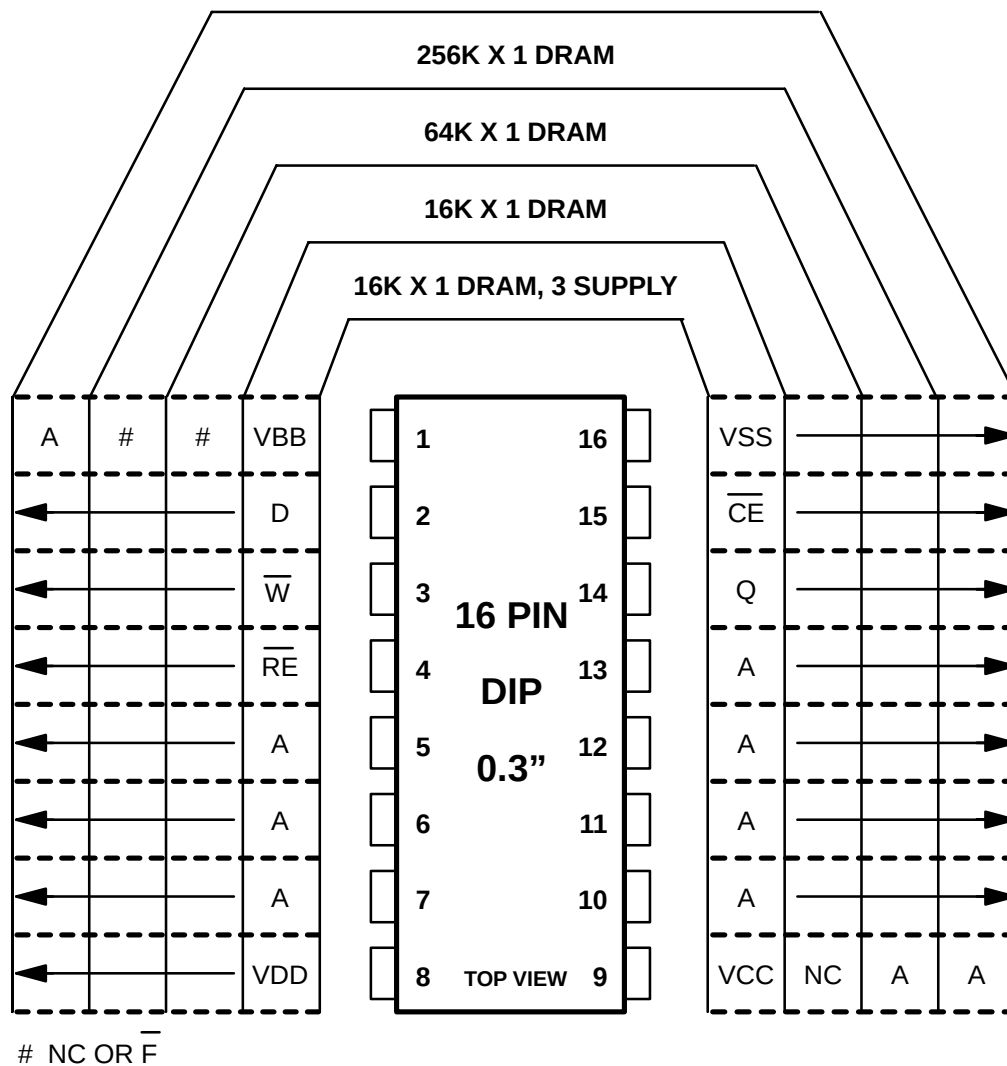


FIGURE 3.9.1-1
16K BY 1 DRAM IN DIP WITH 3 SUPPLY VOLTAGES
16K TO 256K BY 1 DRAM FAMILY IN DIP

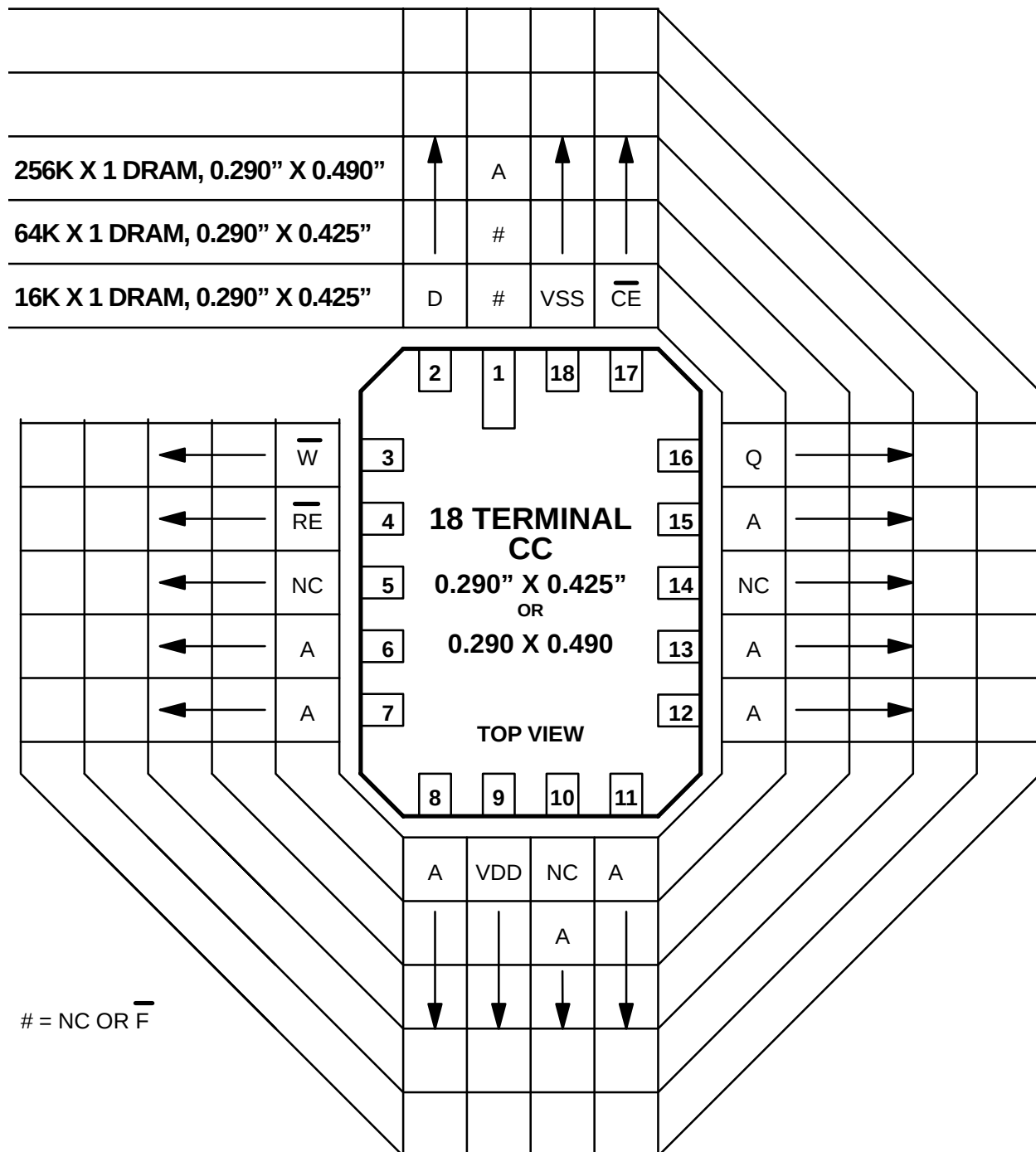


FIGURE 3.9.1-2
16K TO 256K BY 1 DRAM IN RCC