

### 3.9.2 Nibble Wide DRAM

Release NIL

**3.9.2.1 – 16K & 64K BY 4 DRAM IN DIP**

CAPACITY—16K, 64K WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—18 PIN DIP, 0.3" WIDE

PIN ASSIGNMENT—Fig. 3.9.2-1

**3.9.2.2 – 16K BY 4 DRAM IN DIP**

CAPACITY—16K WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address, Separate DATA I/O

PACKAGE—20 PIN DIP, 0.3" WIDE

PIN ASSIGNMENT—Fig. 3.9.2-1

NOTE: At the time that this document was published, this standard was in the process of being rescinded by the Committee.

**3.9.2.3 – 64K BY 4 DRAM IN RCC**

CAPACITY—64K WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address with Common DATA I/O

PACKAGE—22 PAD (PIN) RCC, 0.290" X 0.490"

PIN ASSIGNMENT—Fig. 3.9.2-2

**3.9.2.4 – 256K & 1M BY 4 DRAM FAMILY IN DIP**

CAPACITY—256K, 1M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—20 PIN DIP, Width: 0.3" for 256K & 1M,

PIN ASSIGNMENT—Fig. 3.9.2-3

**3.9.2.5 – 256K TO 4M BY 4 DRAM FAMILY IN SOJ & TSOP2**

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—26/20 PIN SOJ: 0.3" by 0.675" for 256K

—26/20 PIN SOJ or TSOP2: 0.3" or 0.35" by 0.675" for 1M

—26/24 PIN SOJ OR TSOP-2: 0.3" for 4M

—28/24 PIN SOJ: 0.4" by 0.725 for 4M

PIN ASSIGNMENT—Fig. 3.9.2-4

**3.9.2.6 – 64K TO 4M BY 4 DRAM IN ZIP**

CAPACITY—64K, 256K, 1M, 4M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—20 PIN ZIP, 0.400" WIDE FOR 64K, 256K, & 1M PARTS

—24 PIN ZIP, 0.475" WIDE FOR 4M PART

PIN ASSIGNMENT—Fig. 3.9.2-5

**3.9.2.7 – 256K & 1M BY 4 DRAM WITH 4 CE IN SOJ & TSOP2**

CAPACITY—256K, 1M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address with 4 CE clocks controlling the 4 data bits

PACKAGE—26/24 PIN SOJ, Width: 0.3"

—26/24 PIN TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"

PIN ASSIGNMENT—Fig. 3.9.2-6

**3.9.2.8 – 256K BY 4 DRAM IN TSOP1**

CAPACITY—256K WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—24/20 PIN TSOP1, 14.4 mm x 6.0 mm, 0.5 mm LEAD PITCH

PIN ASSIGNMENT—Fig. 3.9.2-7

### 3.9.2.9 – 16M BY 1/4M BY 4 CONFIGURABLE DRAM IN SOJ

CAPACITY—16M WORDS OF 1 BIT or 4M WORDS OF 4 BITS

LOGIC FEATURES—Configurable as a X1 or a X4 part

—The data access mode can be chosen by logic control

PACKAGE—28 PIN SOJ

PIN ASSIGNMENT—Fig. 3.9.2-8

### 3.9.2.10 – 256K TO 4M BY 4 NON-MUX DRAM FAMILY IN SOJ

CAPACITY—256K, 1M, 4M WORDS OF 4 BITS

LOGIC FEATURES—Non-Multiplexed Address

PACKAGE—28, 32, OR 34 PIN SOJ, WIDTH Not yet defined

PIN ASSIGNMENT—Fig. 3.9.2-9

### 3.9.2.11 – 4M BY 4 DRAM WITH 1 $\overline{CE}$ AND 4 $\overline{CE}$ IN TSOP2

CAPACITY—4M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

—There are two versions of this part, one with 1  $\overline{CE}$  and one with 4  $\overline{CE}$  controlling each of the data bits

PACKAGE—28/24 PIN TSOP2, 0.4" WIDE FOR THE 1  $\overline{CE}$  PART

— 28 PIN TSOP2, 0.4" WIDE FOR THE 4  $\overline{CE}$  PART

PIN ASSIGNMENT—Fig. 3.9.2-10

### 3.9.2.12 – 16M BY 4 DRAM IN SOJ & TSOP2

CAPACITY—16M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

This part is available in two package sizes as defined below. The pin rotations of the two are essentially the same with the exception of two NC pins.

PACKAGE—34 PIN SOJ, WIDTH: 0.5"

—34PIN TSOP2, WIDTH: 0.5", PIN PITCH: 0.050"

PIN ASSIGNMENT—Fig. 3.9.2-11

PACKAGE—32 PIN SOJ, 0.400" Wide

—32 PIN TSOP2, 0.400" WIDE, 0.050" PP

PIN ASSIGNMENT—Fig. 3.9.1-12

### 3.9.2.13 – 1M, 2M, & 4M BY 2 DRAM IN SOJ & TSOP2

CAPACITY—1M, 2M, & 4M WORDS OF 2 BITS

LOGIC FEATURES—Multiplexed Address and a separate  $\overline{CE}$  control for each data bit.

PACKAGE—26/20, 26/24, & 28/24 PIN SOJ or TSOP2, WIDTH: 0.3", PIN PITCH: 0.050"

PIN ASSIGNMENT—Fig. 3.9.2-12

### 3.9.2.14 – 16M BY 4 DRAM WITH 4 $\overline{CE}$ IN SOJ OR TSOP2

CAPACITY—16M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

—The part, has 4  $\overline{CE}$ , one controlling each of the data bits.

PACKAGE— 34 PIN TSOP2, 12.7 mm WIDE, PP = 1.27 mm

— 34 PIN SOJ, 12.7 mm WIDE, PP = 1.27 mm

PIN ASSIGNMENT—Fig. 3.9.2-14

PACKAGE—32 PIN SOJ, 10.16 mm Wide

—32 PIN TSOP2, 10.16 mm Wide, 1.27 mm PP

PIN ASSIGNMENT—Fig. 3.9.2-14

### 3.9.2.15 – 64M X 4 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 64M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT—Fig. 3.9.2-15

**NOTE:** This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

**3.9.2.16 – 4M BY 4 DRAM IN USON**

CAPACITY—4M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—28 PAD USON, 7 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.2-16

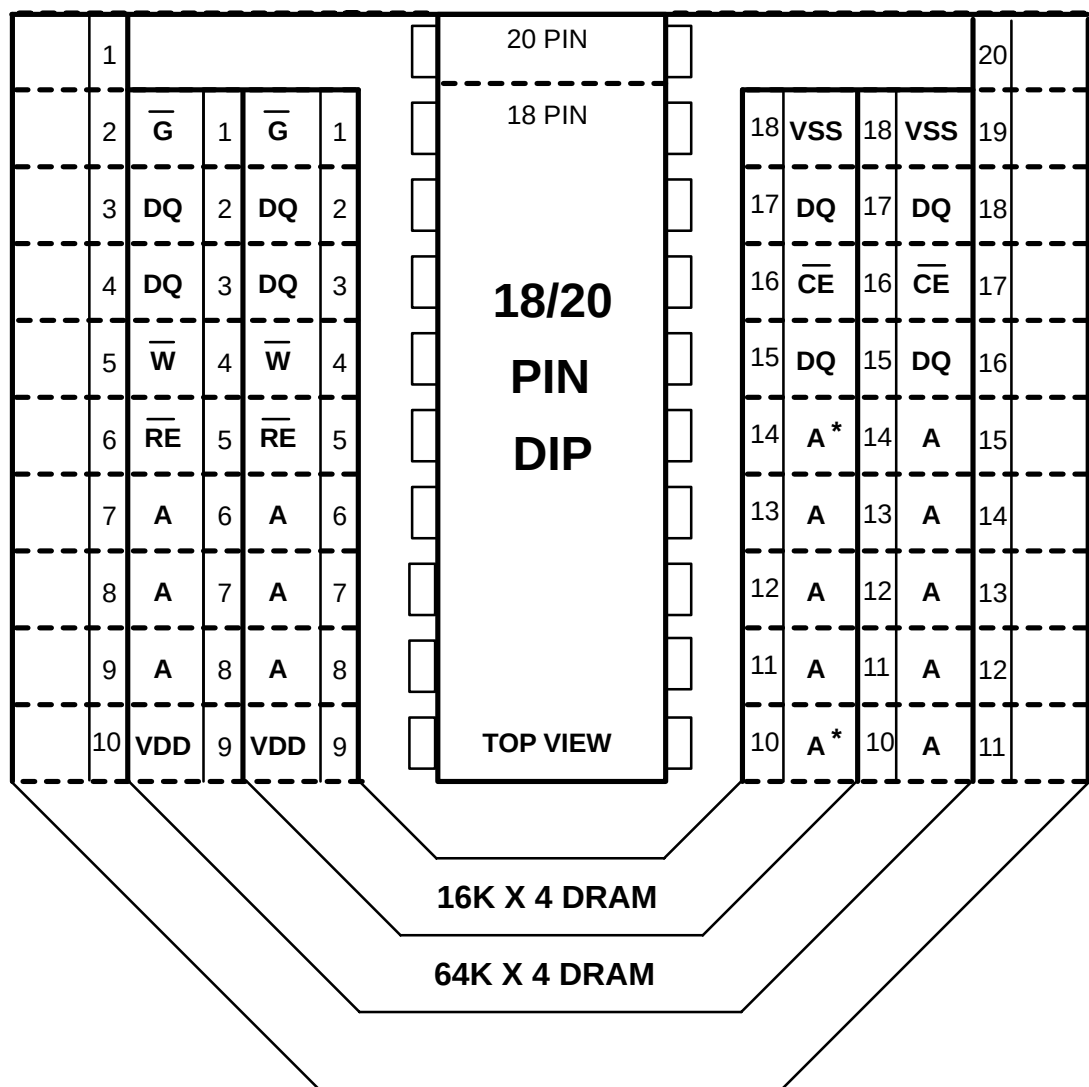
**3.9.2.17 – 16M BY 4 DRAM IN USON**

CAPACITY—16M WORDS OF 4 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—36 PAD USON, 10 mm WIDE, 0.8 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.2-17



\* COLUMN ADDRESS NOT SUPPLIED ON PINS 10 & 14 TO 16K PART

FIGURE 3.9.2-1  
16K & 64K BY 4 DRAM IN DIP

Release 1

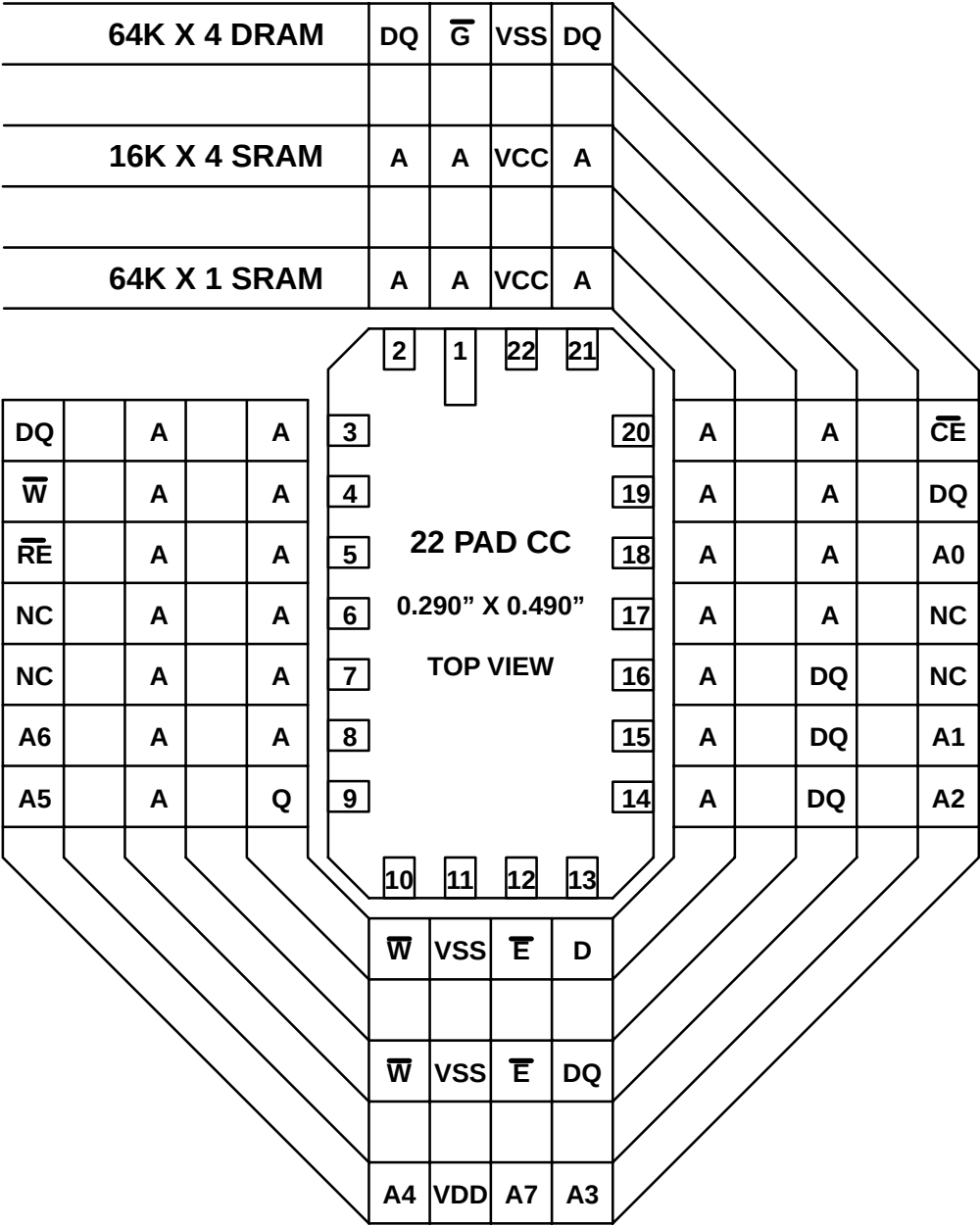


FIGURE 3.9.2-2  
64K BY 4 DRAM IN RCC

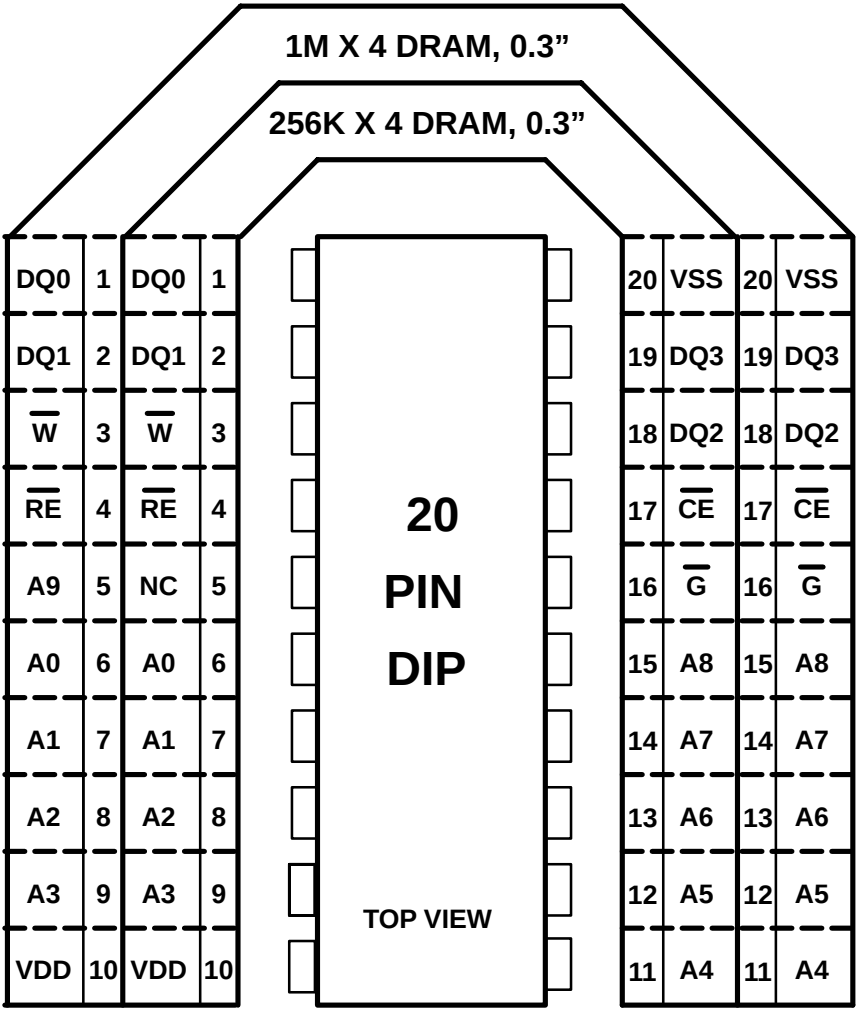


FIGURE 3.9.2-3  
256K & 1M BY 4 DRAM FAMILY IN DIP