

3.9.4 Word Wide DRAM

Release 1

3.9.4.1 – 64K BY 16 DRAM WITH 2 $\overline{W}$ IN SOJ & TSOP2

CAPACITY—64K WORDS OF 16 BITS,
LOGIC FEATURES—MULTIPLEXED ADDRESS
PACKAGE—40 PIN SOJ, 0.400" WIDE
—44/40 PIN TSOP2, 0.400" WIDE, 0.8mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–1 (SOJ)
—Fig. 3.9.4–6 (TSOP2)

3.9.4.2 – 256K & 1M BY 16 & 18 WITH 2 $\overline{CE}$ OR 2 $\overline{W}$ DRAM IN SOJ & TSOP2

CAPACITY—256K, 1M WORDS OF 16 & 18 BITS,
The standard for the 2 $\overline{W}$ versions of the 1M part has been rescinded and removed from Figs. 3.9.4–4 & 3.9.4–5 in Release 5.
LOGIC FEATURES—MULTIPLEXED ADDRESS
—There are two versions of these parts, one with 2 $\overline{W}$ and the other with 2 $\overline{CE}$.
—The two clocks control the LOWER BYTE and UPPER BYTE data bits.
—The 1M part allows the option of the manufacturer to utilize either 1K or 4K refresh cycles
PACKAGE—256K in 40 PIN SOJ, 0.400" WIDE
—256K in 44/40 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
—1M IN 42 PIN SOJ, 0.400" WIDE
—1M in 50/44 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–2 (256K SOJ)
—Fig. 3.9.4–3 (256K TSOP2)
—Fig. 3.9.4–4 (1M SOJ)
—Fig. 3.9.4–5 (1M TSOP2)

3.9.4.3 – 256K BY 16 DRAM WITH EXTENDED FUNCTIONS IN DIP AND SOJ

CAPACITY—256K WORDS OF 16 BITS
LOGIC FEATURES—This part contains multiple logic functions that are similar to those used in MPDRAMS and that are keyed for VIDEO memory applications. All devices meeting this standard must contain all functions which must be implemented as defined in the TRUTH TABLE.
PACKAGE—40 PIN DIP, 0.400" WIDE, 0.100" PIN PITCH
—40 PIN SOJ, 0.400" WIDE, 0.050" PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–7A
FUNCTION TRUTH TABLE—Fig. 3.9.4–7B

3.9.4.4 – 2M BY 16 & 4M BY 16 & 18 DRAM IN TSOP2

CAPACITY—2M & 4M WORDS OF 16 or 4M WORDS OF 18 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts utilizes 4K or 8K refresh cycles
PACKAGE—50 PIN TSOP2, 0.400" WIDE, 0.8 mm PIN PITCH, X16 parts only
PACKAGE—54 PIN TSOP2, 0.500" WIDE, 0.8 mm PIN PITCH
PIN ASSIGNMENT—Fig. 3.9.4–8

3.9.4.5 – 128K & 256K BY 16 BURST DRAM WITH 2 CAS IN SOJ, TSOP2, OR ZIP

CAPACITY—128K OR 256K WORDS OF 16 BITS
LOGIC FEATURES—MULTIPLEXED ADDRESS
—These parts have BURST data out capability
PACKAGE—40 PIN SOJ, 10.16 mm WIDE, 1.27 mm PIN PITCH
PACKAGE—44/40 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PIN PITCH
PACKAGE—40 PIN ZIP, 1.27 mm PIN PITCH (256K only)
PIN ASSIGNMENT—SOJ, Fig. 3.9.4–9
PIN ASSIGNMENT—TSOP2, Fig. 3.9.4–10
PIN ASSIGNMENT—ZIP, Fig. 3.9.4–11, (256K ONLY)

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3.9.4.6 – 16M X 16 DRAM IN TSOP2 PIN ROTATION

CAPACITY— 16M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT—Fig. 3.9.4–12

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time.

3.9.4.7 – 128K, 256K, & 512K X 32 DRAM WITH 4 $\overline{CE}$ IN SSOP

CAPACITY—128K, 256K, OR 512K WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address

—The part, has 4 $\overline{CE}$, one controlling each group of 8 data bits.

PACKAGE— 64 PIN SSOP, 0.525" WIDE, PP = 0.8 mm

PIN ASSIGNMENT—Fig. 3.9.4–13

3.9.4.8 – 512K & 2M BY 32 & 36 DRAM WITH 4 $\overline{CE}$ IN SOJ & TSOP2

CAPACITY—512K, 2M WORDS OF 32 & 36 BITS,

LOGIC FEATURES—MULTIPLEXED ADDRESS

—The part, has 4 $\overline{CE}$, one controlling each group of 8 or 9 data bits.

—The standard allows the option of the manufacturer to utilize either 1K or 4K refresh cycles

PACKAGE—70 PIN TSOP2, 10.16 mm WIDE, 0.8 mm PP

—70 PIN TSOP2, 10.16 mm WIDE, 0.65 mm PP, 512K only.

—70 PIN SOJ, 10.16 mm WIDE, 0.8 mm PP

PIN ASSIGNMENT—Fig. 3.9.4–14

3.9.4.9 – 8M X 32 DRAM IN TSOP2 PIN ROTATION (OBSOLETE, DO NOT USE)

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—TSOP2, PIN COUNT AND DIMENSIONS NOT DEFINED

PIN ASSIGNMENT—Fig. 3.9.4–15

NOTE: This standard defines a pin rotation only. The package details, dimension and pin count, are not defined at this time. (THIS STANDARD WAS DECLARED OBSOLETE IN 1998)

3.9.4.10 – 2M X 32 DRAM IN TSOP2

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

PACKAGE—86 PIN TSOP2, 10.16 mm WIDE, 0.5 mm PP

PIN ASSIGNMENT—Fig. 3.9.4–16

3.9.4.11 – 2M X 32 DRAM WITH EDO IN QFP

CAPACITY— 8M WORDS OF 32 BITS

LOGIC FEATURES—Multiplexed Address, Common DATA I/O

—The Data Out conforms to the EDO feature defined in Par. 3.9.5.7.

PACKAGE—100 PIN QFP OR TQFP, 10 mm BU 14 mm, 0.65 mm PP

PIN ASSIGNMENT—Fig. 3.9.4–17

3.9.4.12 – 1M BY 16 DRAM IN USON

CAPACITY—1M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—46 PAD USON, 7 mm WIDE, 0.5 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.4–18

3.9.4.13 – 4M BY 16 DRAM IN USON

CAPACITY—4M WORDS OF 16 BITS

LOGIC FEATURES—Multiplexed Address

PACKAGE—58 PAD USON, 10 mm WIDE, 0.5 mm Pad Pitch

PIN ASSIGNMENT—Fig. 3.9.4–19

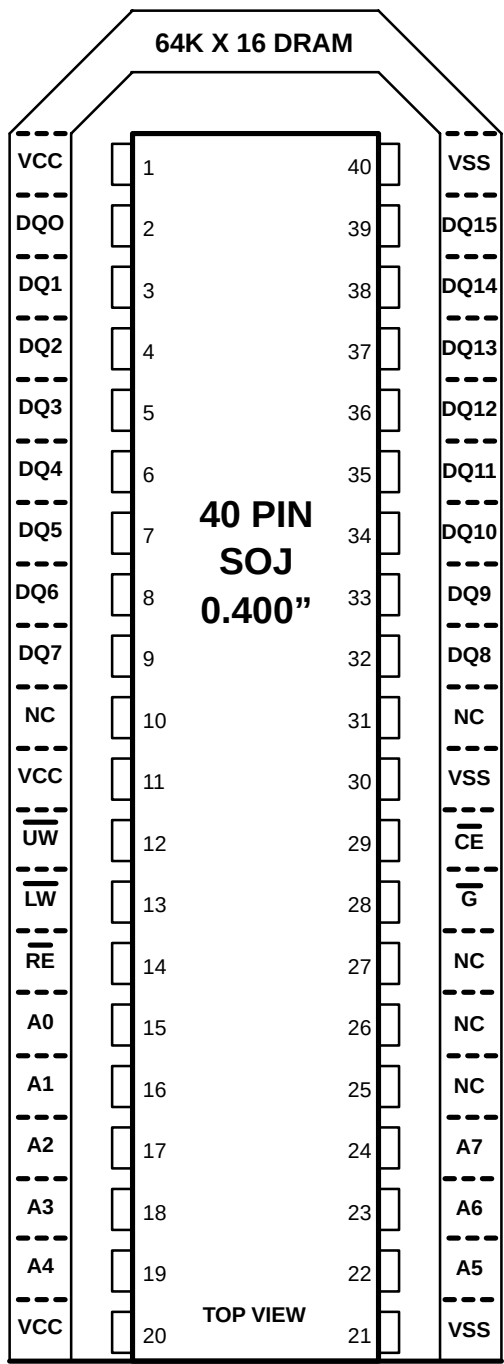


FIGURE 3.9.4-1
64K BY 16 DRAM IN SOJ

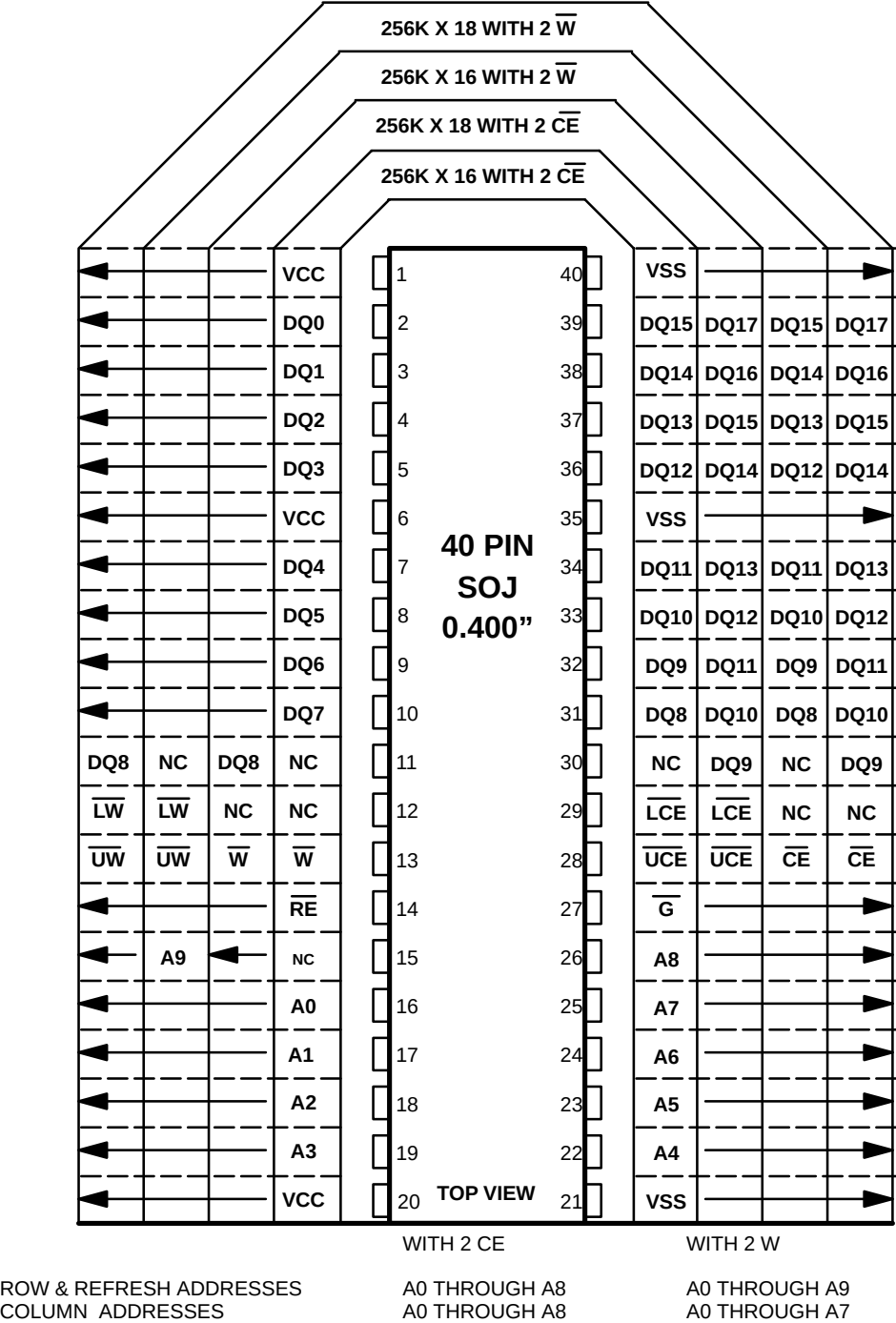
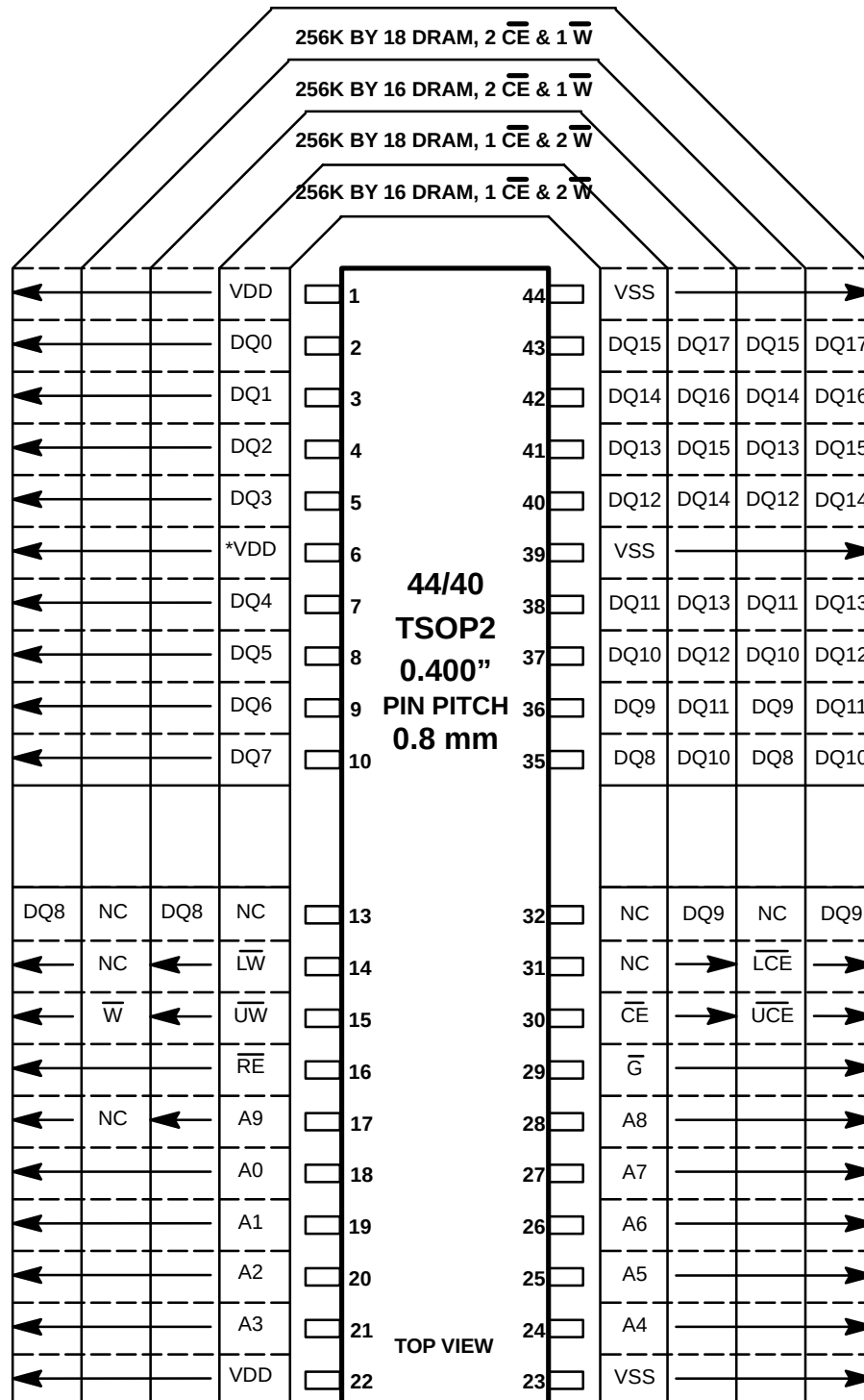


FIGURE 3.9.4-2
256K BY 16 & 18 DRAM WITH 2 $\overline{W}$ OR 2 $\overline{CE}$ IN SOJ



CONFIGURATION
REFRESH COUNT
REFRESH ADDRESS
ROW ADDRESS
COLUMN ADDRESS

1 $\overline{CE}$, 2 $\overline{W}$
1024 Cycles
A0 TO A9
A0 TO A9
A0 TO A7

2 $\overline{CE}$, 1 $\overline{W}$
512 Cycles
A0 TO A8
A0 TO A8
A0 TO A8

The JEDEC Std. No 30 designator for the TSOP2 package is PDSO-G

* NOTE: In the first release of this standard, Pin 6 was a VSS connection. This was in error and this release changes Pin 6 to VDD.

FIGURE 3.9.4-3

256K BY 16 & 18 DRAM WITH 2 $\overline{W}$ OR 2 $\overline{CE}$ IN TSOP2

Release 4

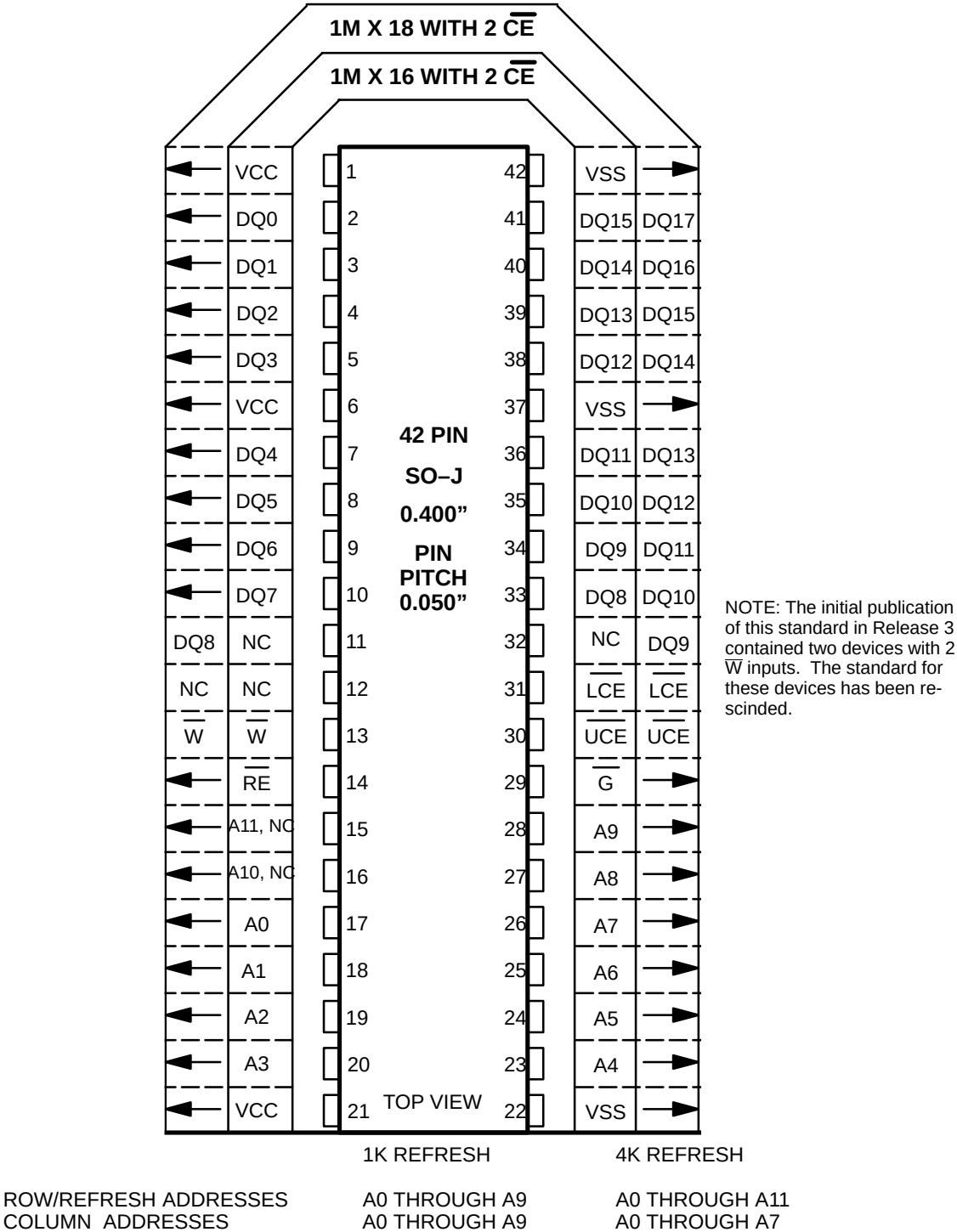


FIGURE 3.9.4-4
1M BY 16 & 18 DRAM WITH 2 $\overline{CE}$ IN SOJ