

3.9.5 DRAM Optional Features

Release 1

3.9.5.1 - OPTIONAL OPERATIONAL MODES AND CYCLES FOR DRAM

The definitions for serial data access, bit write, and refresh control included in Release 1 of this standard have been replaced by the more general definitions of Optional Operational Modes and Cycles beginning on page 3.9.5-11

3.9.5.2 - 1M DRAM BUILT IN TEST FUNCTION

An approved option for 1M DRAM (1M X 1 or 256K X 4) is the inclusion of a built in manufacturer defined "Test Mode". This mode is enabled using a dedicated pin which is optional NC or TF. When the optional mode is implemented, the manufacturer should include notes on his data sheet as follows:

- (A) Normal operation requires the "TF" pin be connected to a VSS or logic low level or left unconnected.
- (B) When the "TF" pin is connected to the manufacturer defined positive voltage, the internal test mode will be actuated. Contact the manufacturer for specific operational details of the Test Mode.

3.9.5.3 - ON-CHIP REFRESH CONTROL FOR X8 DRAM

This standard describes an optional feature that is applicable to the non-address multiplexed byte wide dynamic RAMs described in this publication. The standard establishes the clock timing sequence needed to invoke an on-chip refresh feature.

3.9.5.4 - $\overline{G}$ BEFORE $\overline{E}$ REFRESH

If G is low when E falls, a refresh cycle is executed. During this type of refresh cycle, an internal counter/register provides the refresh address and the external address is ignored

3.9.5.5 - DRAM SPECIAL TEST AND OPERATIONAL MODES

This standard defines a scheme for controlling a series of special operational modes for address multiplexed DRAM. The standard defines the logic interface required to enter, control and exit from the special modes. In addition, it defines a basic test mode plus a series of other special test and operational modes. The details of this standard are given on pages 3.9.5-7 through 3.9.5-10.

3.9.5.6 - NON-MULTIPLEXED DRAM OPERATION

This standard defines multiple aspects of the address and clock relationships for DRAMs that have a non-multiplexed address architecture. It also defines the relationships between the address bits of multiplexed and non-multiplexed devices. The details of the standard are given on page 3.9.5-13

3.9.5.7 - DRAM EXTENDED DATA OUT

This standard defines the output characteristics of Extended Data Out (EDO) feature for DRAMs. Any part incorporating "EDO" must satisfy all of the following criteria to conform to the Standard. The details of the EDO standard are given on P 3.9.5-14

3.9.5.8 - 256M DRAM TEST MODE DATA AND ADDRESS COMPRESSION

This standard defines the algorithms for data and address compression when 256M DRAMs are operated in the built in special test mode. The detaild of the Compression standard are given on P 3.9.5-15

3.9.5.9 - PIPELINED NIBBLE MODE DEFINITION

This standard defines the output characteristics of the Pipelined Nibble Mode feature for DRAMs. Any part incorporating Pipelined Nibble Mode must satisfy all of the following criteria to conform to the Standard. The details of the standard are given on P 3.9.5-16

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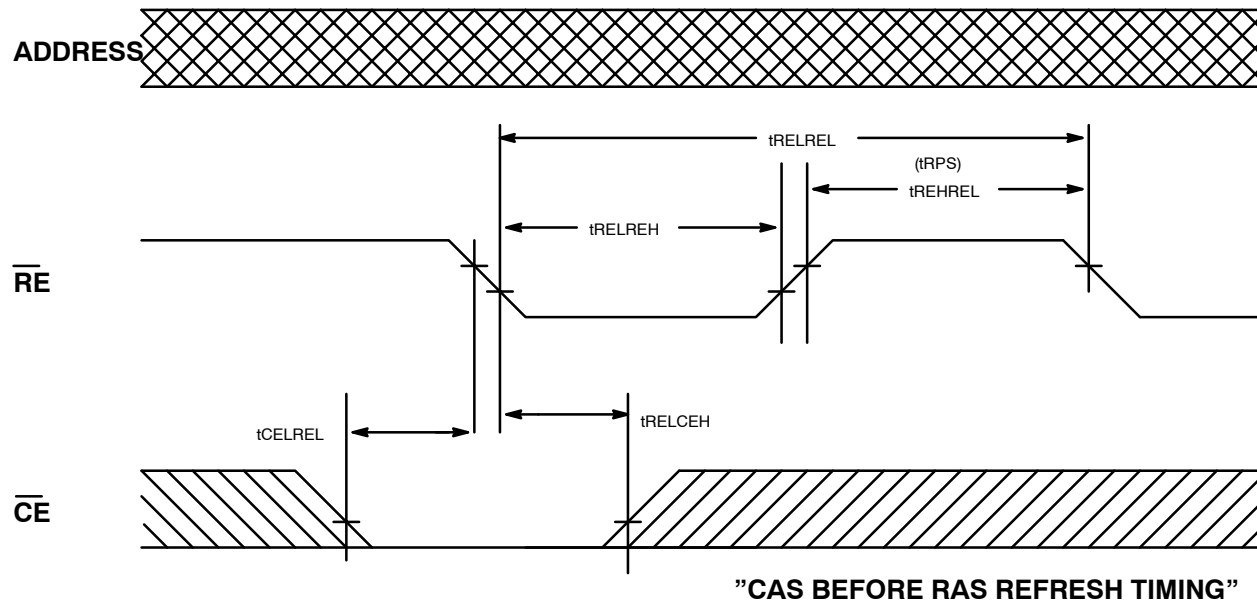
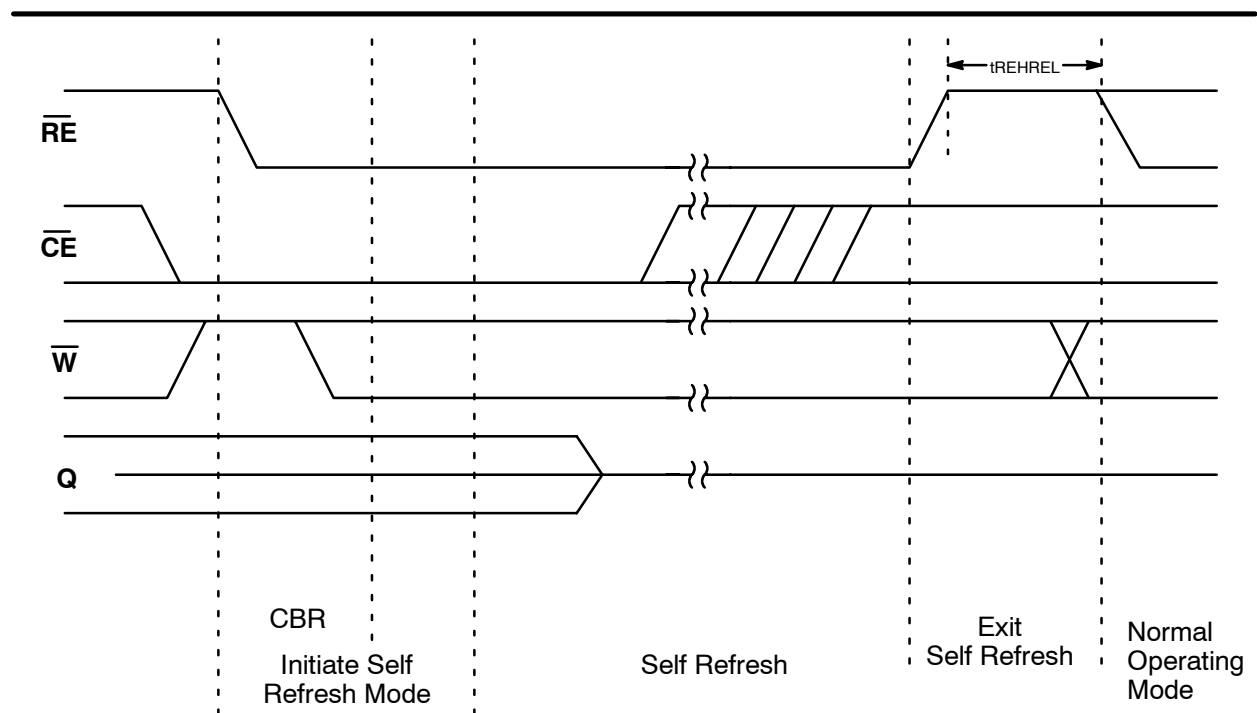


FIGURE 3.9.5-1A
DRAM ON CHIP REFRESH TIMING



Data Out may be either Tristate or Active depending on the state of $\overline{CE}$ when the cycle is entered.

FIGURE 3.9.5-1 B
DRAM SELF REFRESH MODE TIMING