

3.5.1 EEPROM, Byte Wide

Release 1

3.5.1.1 - .5K TO 2K BY 8 EEPROM FAMILY IN DIP

CAPACITY--.5K, 1K, 2K WORDS OF 8 BITS
PACKAGE--24 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.5.1-1

3.5.1.2 - 2K & 4K BY 8 EEPROM IN RCC

CAPACITY--2K, 4K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.5.1-2
These devices are CC equivalents of 24 pin DIP devices

3.5.1.3 - 1K TO 32K BY 8 EEPROM FAMILY IN DIP

CAPACITY--1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE--28 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.5.1-3

3.5.1.4 - .5K TO 32K BY 8 EEPROM FAMILY IN RCC

CAPACITY--.5K, 1K, 2K, 4K, 8K, 16K, 32K WORDS OF 8 BITS
PACKAGE--32 PAD (PIN) RCC, 0.450" BY 0.550"
PIN ASSIGNMENT--Fig. 3.5.1-4

3.5.1.5 - 32K TO 256K BY 8 EEPROM FAMILY IN SOJ,

CAPACITY--32K, 128K, 256K WORDS OF 8 BITS,
PACKAGE--28 OR 32 PIN SOJ, 0.4" WIDE OR NOT DEFINED
PIN ASSIGNMENT--Fig. 3.5.1-5

3.5.1.6 - 32K TO 512K BY 8 EEPROM FAMILY IN DIP,

CAPACITY--32K, 64K, 128K, 256K, 512K WORDS OF 8 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.5.1-6

3.5.1.7 - 32K TO 256K BY 8 EEPROM FAMILY IN RCC,

CAPACITY--32K, 64K, 128K, 256K WORDS OF 8 BITS,
PACKAGE--32 PIN RCC, 0.450" X 0.550"
PIN ASSIGNMENT--Fig. 3.5.1-7

3.5.1.8 - 32K TO 256K BY 9 EEPROM FAMILY IN DIP,

CAPACITY--32K, 64K, 128K, 256K WORDS OF 9 BITS,
PACKAGE--32 PIN DIP, 0.6" WIDE
PIN ASSIGNMENT--Fig. 3.5.1-8

3.5.1.9 - 128K TO 1M BY 8 EEPROM FAMILY IN SCC,

CAPACITY--128K, 256K, 512K, & 1M WORDS OF 8 BITS,
PACKAGE--44 PIN SCC, 0.650" x 0.650"
PIN ASSIGNMENT--Fig. 3.5.1-9

3.5.1.10 - 32K TO 256K BY 8 EEPROM FAMILY IN TSOP1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
 PACKAGE--32 LEAD TSOP-1, 8 mm X 18.4 mm
 PIN ASSIGNMENT--Fig. 3.5.1-10

3.5.1.11 - EXTENDED FEATURE SET FOR 256K BIT EEPROM

This standard specifies features beyond the existing pinout standards that need to be standardized for 32K X 8 EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.1..

3.5.1.11.1 - REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 32K Byte EEPROMs and must be implemented to be in compliance with this standard:

- Operate with a primary power supply of 5.0 V nominal
- Operate in conformance with the standard truth table
- Have read and write timing cycles which are consistent with the standard timing diagrams
- Contain Data & Address Latches for Write cycles
- Operate with self timed write cycles
- Operate with input levels between 0 and 5 Volts.

3.5.1.11.2 - OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:

- Page Write Mode with standard write cycle timings
- Minimum page size of 16 Byte in page write mode
- DATA\ Polling
- Software Data Protect Option
- Hardware Mass Erase (All 1's)
- Software Mass Erase (All 1's)

3.5.1.12 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices (commonly known as FLASH EEPROM). This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.2-4

3.5.1.13 - 512K BY 8 DUAL-SUPPLY EEPROM IN RCC

CAPACITY--512K WORDS OF 8 BITS,
 PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
 PIN ASSIGNMENT--Fig. 3.5.1-12

3.5.1.14 - 128K TO 512K BY 8 SINGLE-SUPPLY EEPROM FAMILY IN DIP, RCC, & TSOP-1

CAPACITY--32K, 64K, 128K, & 256K WORDS OF 8 BITS,
 THESE DEVICES ARE APPROVED IN THREE PACKAGES:
 DIP PACKAGE--32 LEAD DIP, 15.24 mm (0.6") WIDE WITH 2.54 mm (0.1") PP
 PIN ASSIGNMENT--Fig. 3.5.1-13
 RCC PACKAGE--32 LEAD RCC, 11.43 mm X 13.97 mm (0.450" X 0.550")
 PIN ASSIGNMENT--Fig. 3.5.1-14
 TSOP-1 PACKAGE--32 LEAD TSOP-1, 8 mm X 20 mm WITH 0.5 mm PP
 PIN ASSIGNMENT--Fig. 3.5.1-15

3.5.1.15 - 256K, 512K, & 1M BY 8 DUAL-SUPPLY EEPROM IN TSOP-1

CAPACITY--256K, 512K, 1M WORDS OF 8 BITS,
PACKAGE--40 LEAD TSOP-1, 10 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT--256K, 512K, Fig. 3.5.1-18
PIN ASSIGNMENT--1M, Fig. 3.5.1-16

The 256K & 512K devices have a different pin assignment pattern from the 1M device, therefore are not backward compatible with the 1M device.

3.5.1.16 - 1M TO 8M BY 8 SINGLE-SUPPLY EEPROM FAMILY IN TSOP-1

CAPACITY--1M, 2M, 4M, & 8M WORDS OF 8 BITS,
PACKAGE--48 LEAD TSOP1, 12 mm X 20 mm WITH 0.5 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-17

3.5.1.17 - 8K BY 256B OR 264B SERIAL ACCESS EEPROM IN TSOP-2

CAPACITY--8K WORDS OF 256 OR 264 BYTES, SERIALY ACCESSED
PACKAGE--44/40 LEAD TSOP2, 10.16 mm WIDE WITH 0.8 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-19 A
CONTROL & LOGIC TABLES--Figs. 3.5.1-19 B & C

3.5.1.18 - 1M & 2M BY 8 SINGLE OR DUAL SUPPLY EEPROM FAMILY IN PSOP

CAPACITY--1M & 2M WORDS OF 8 BITS,
PACKAGE--44 LEAD PSOP 16 mm wide WITH 1.27 mm PP
PIN ASSIGNMENT--Fig. 3.5.1-20

**3.5.1.19 - 4Mb TO 32Mb DENSITY BY 8 Dual Supply Flash EEPROM in 8 X 5 GRID
Micro BGA Package**

CAPACITY--512K, 1024K, 2048K, & 4096K WORDS OF 8 BITS
PACKAGE--8 X 5 GRID MICRO BGA PACKAGE, 0.75 mm BUMP PITCH
PIN ASSIGNMENTS--Fig. 3.5.1-21

3.5.1.20 - 2K BIT SERIAL, SINGLE SUPPLY EEPROM IN 8 PIN SOG

CAPACITY--2K BITS, ACCESSABLE SERIALY, 1 BIT AT A TIME
PACKAGE--8 PIN SOG
PIN ASSIGNMENT--Fig. 3.5.1-22

This device is intended for use on memory modules to store the SPD information so that it may be interrogated by the host computer to determine the electrical and logic characteristics of the module.

3.5.1.21 - 2-WIRE EEPROM IN SMALL FOOTPRINT PACKAGE

PIN ASSIGNMENT--Fig. 3.5.1-23

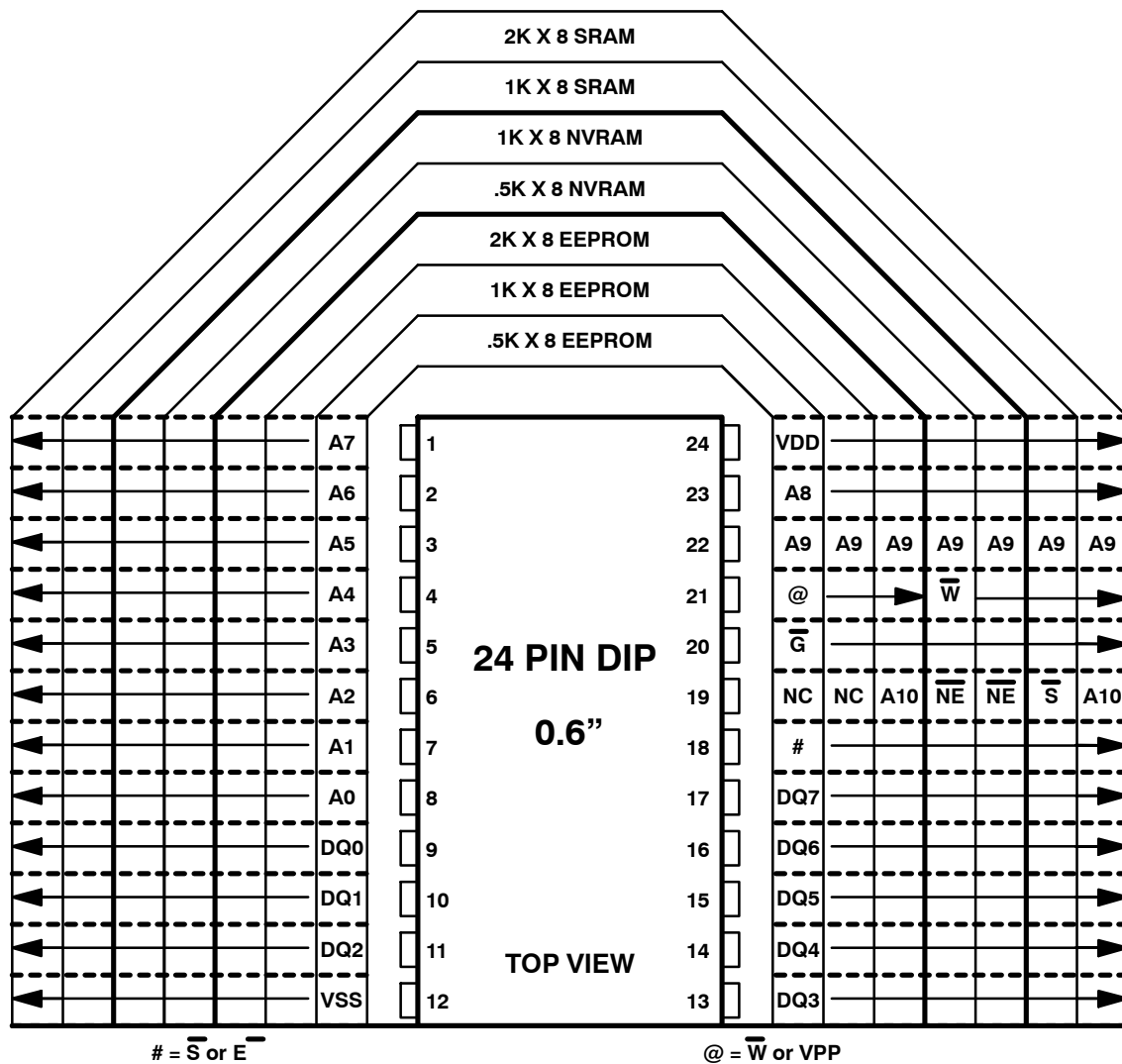


FIGURE 3.5.1-1
.5K TO 2K BY 8 EEPROM IN DIP

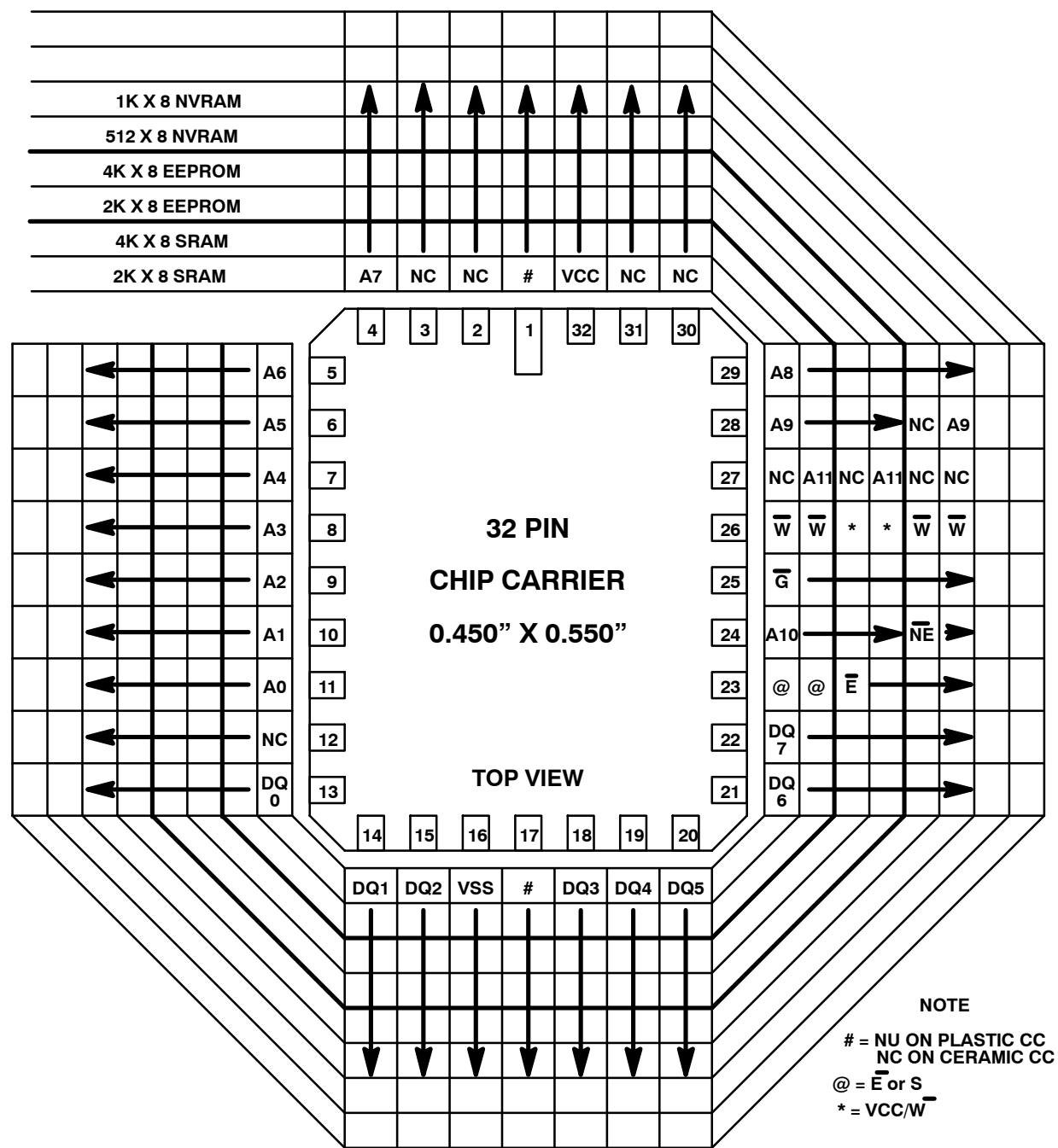


FIGURE 3.5.1-2
2K & 4K BY 8 EEPROM IN RCC

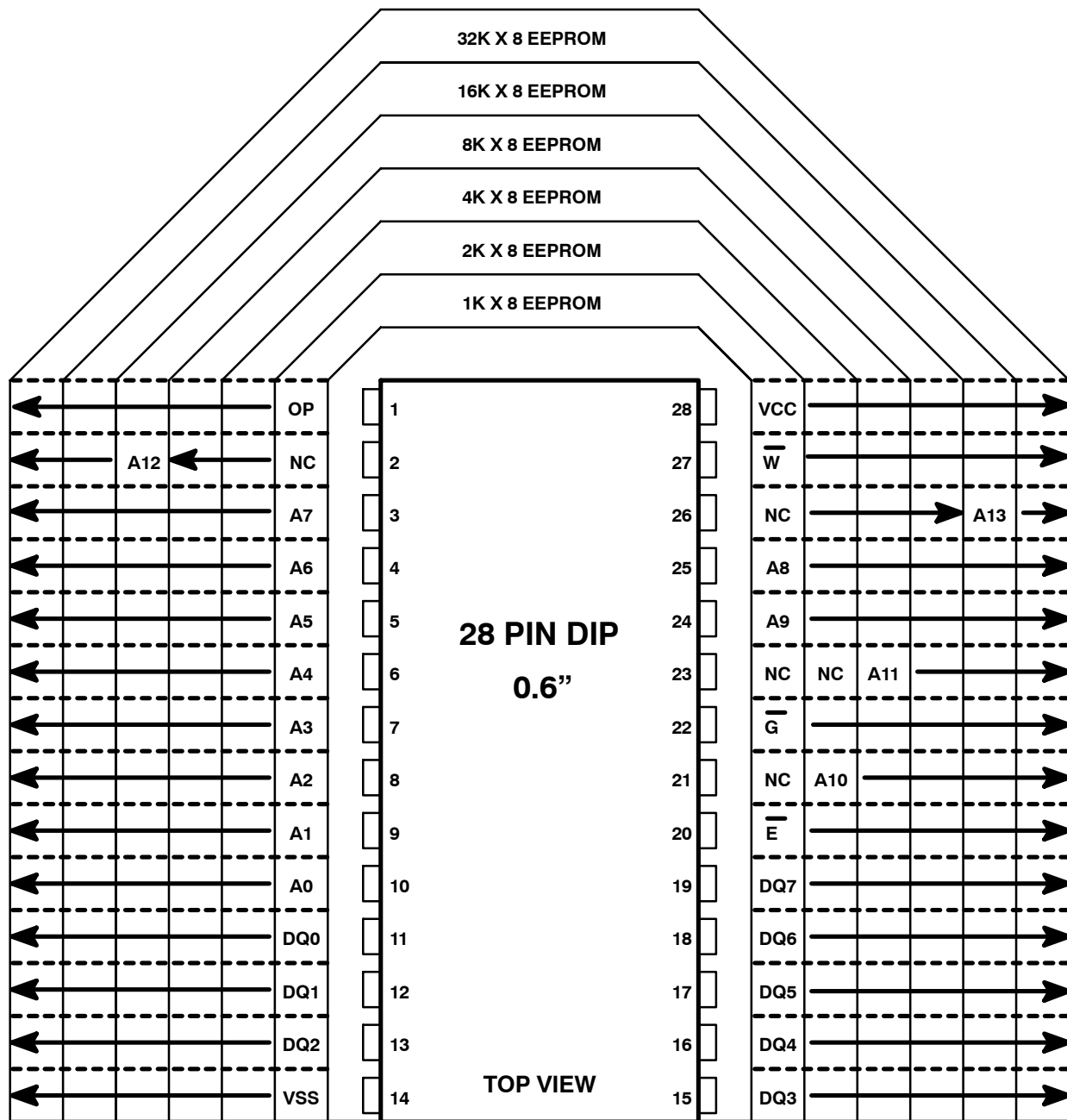


FIGURE 3.5.1-3
1K TO 32K BY 8 EEPROM FAMILY IN DIP

Release 1

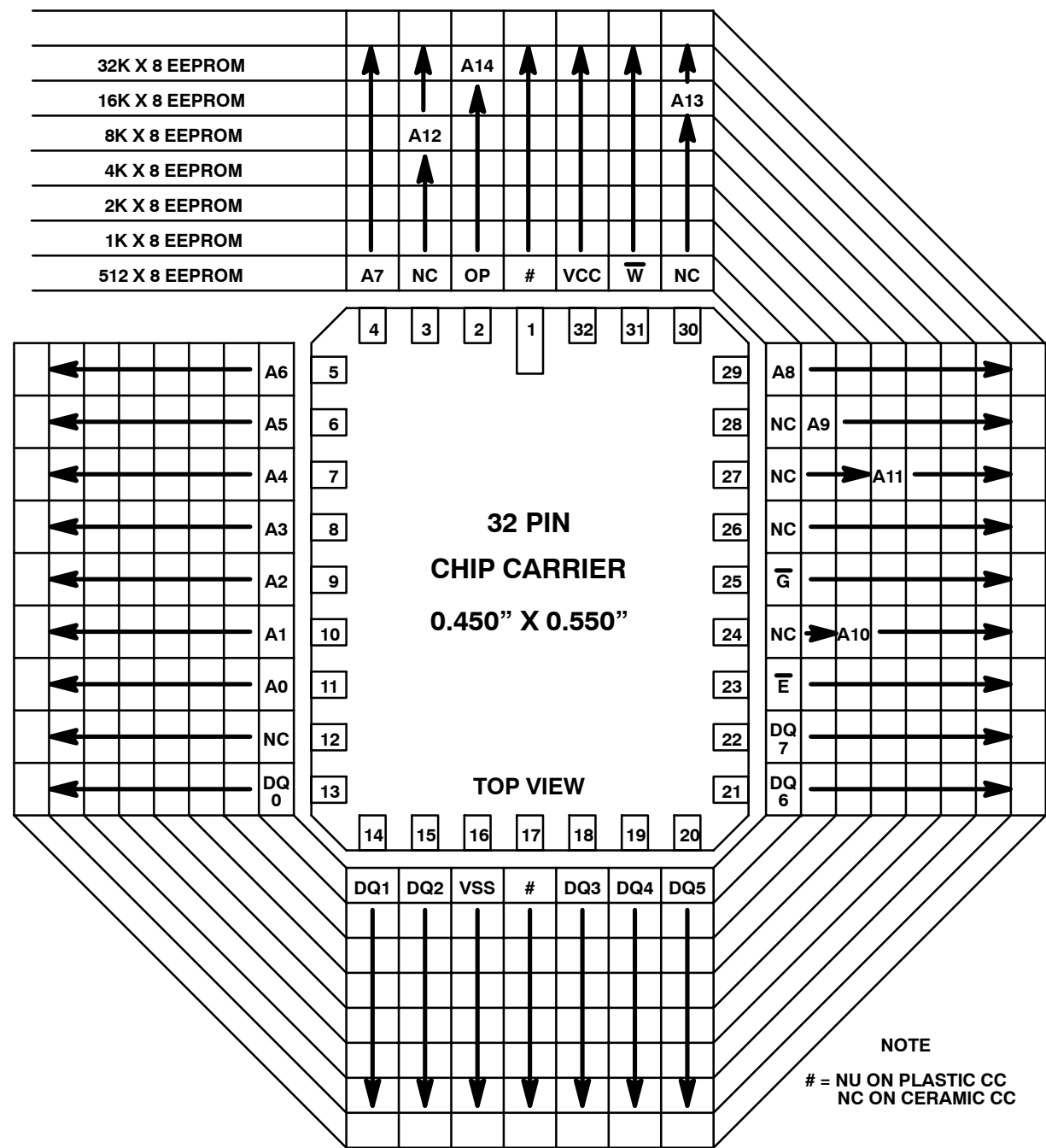


**FIGURE 3.5.1-4
.5K TO 32K BY 8 EEPROM FAMILY IN RCC**

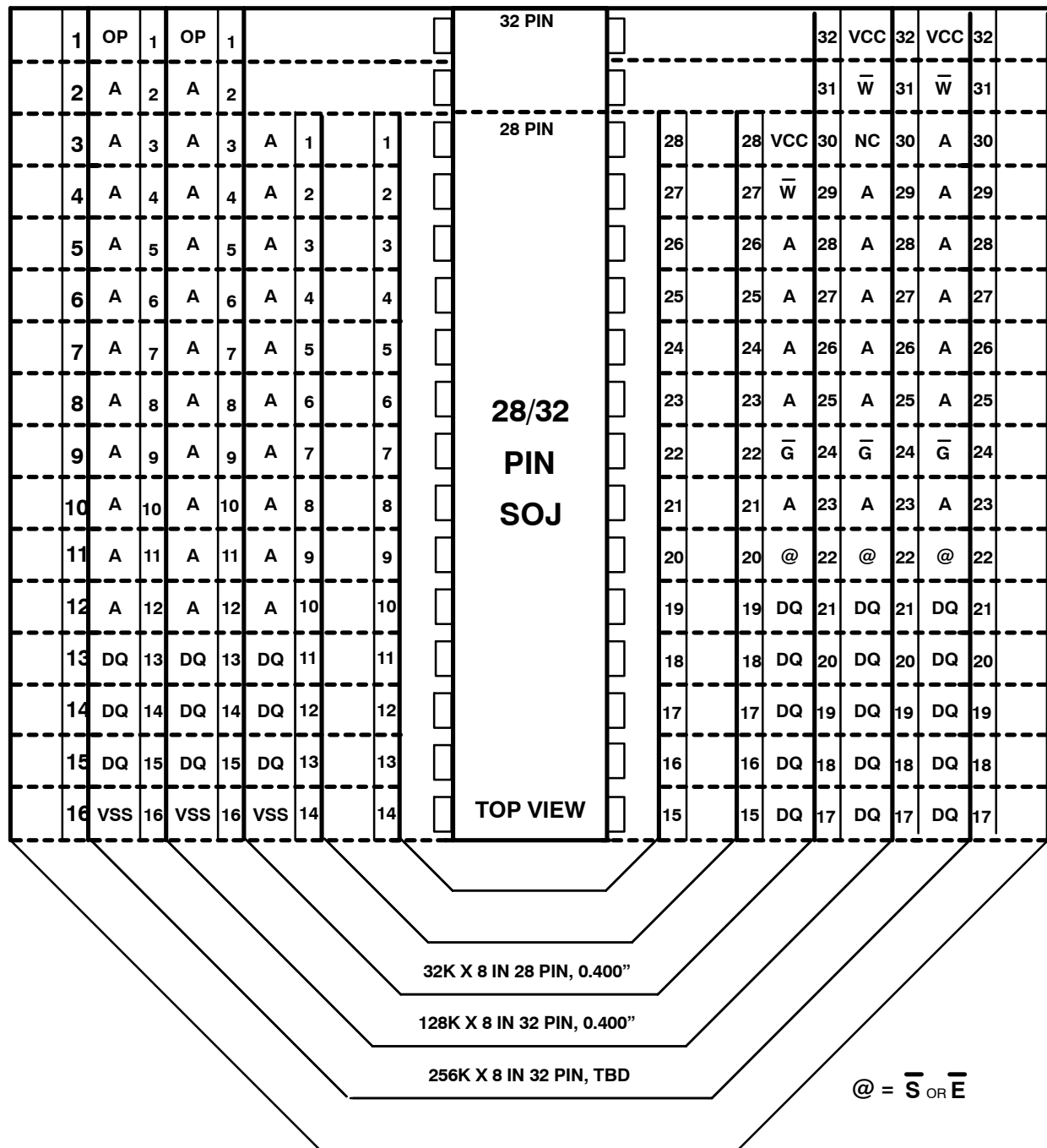


FIGURE 3.5.1-5
32K TO 256K BY 8 EEPROM FAMILY IN SOJ

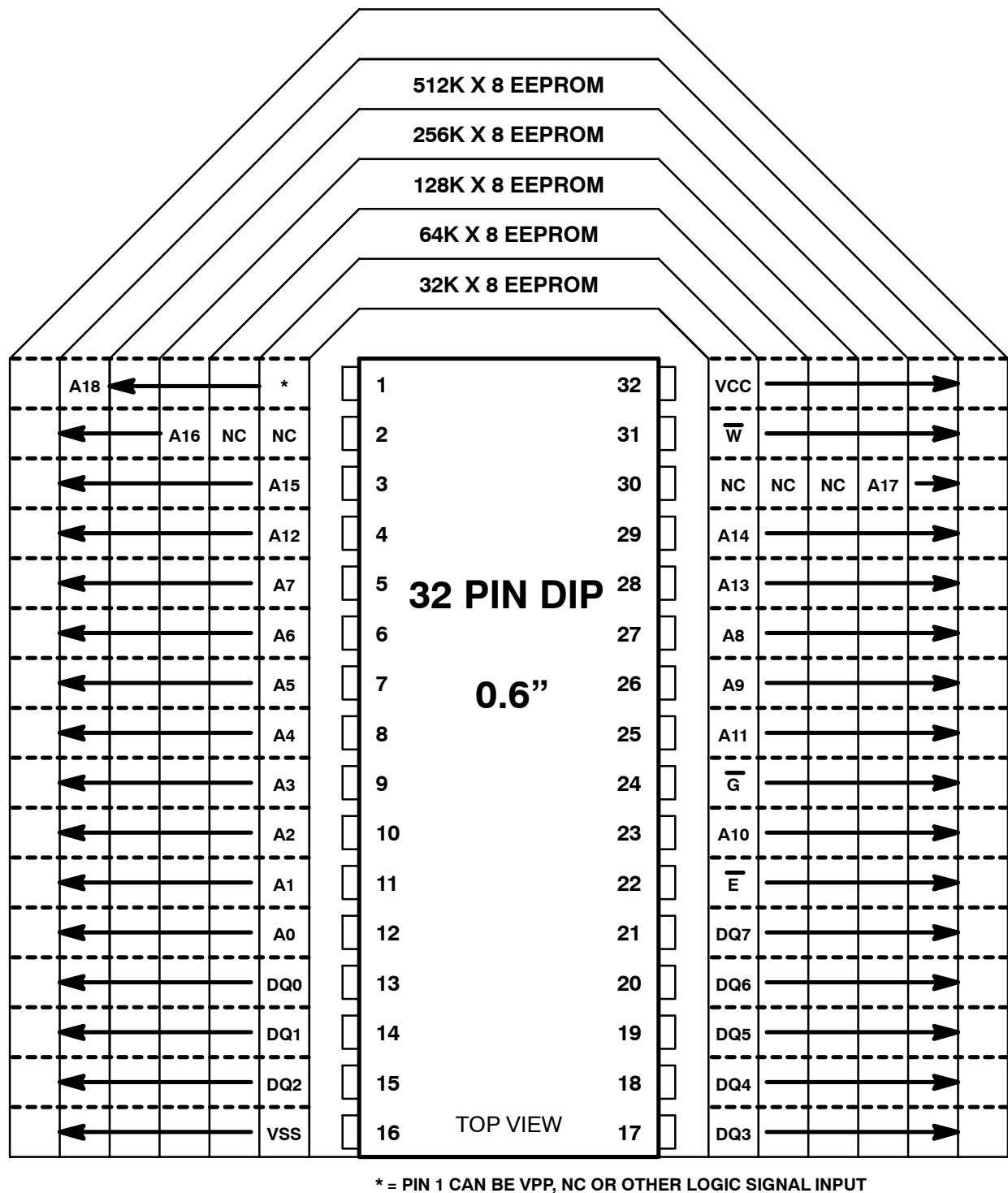


FIGURE 3.5.1-6
32K TO 512K BY 8 EEPROM FAMILY IN DIP

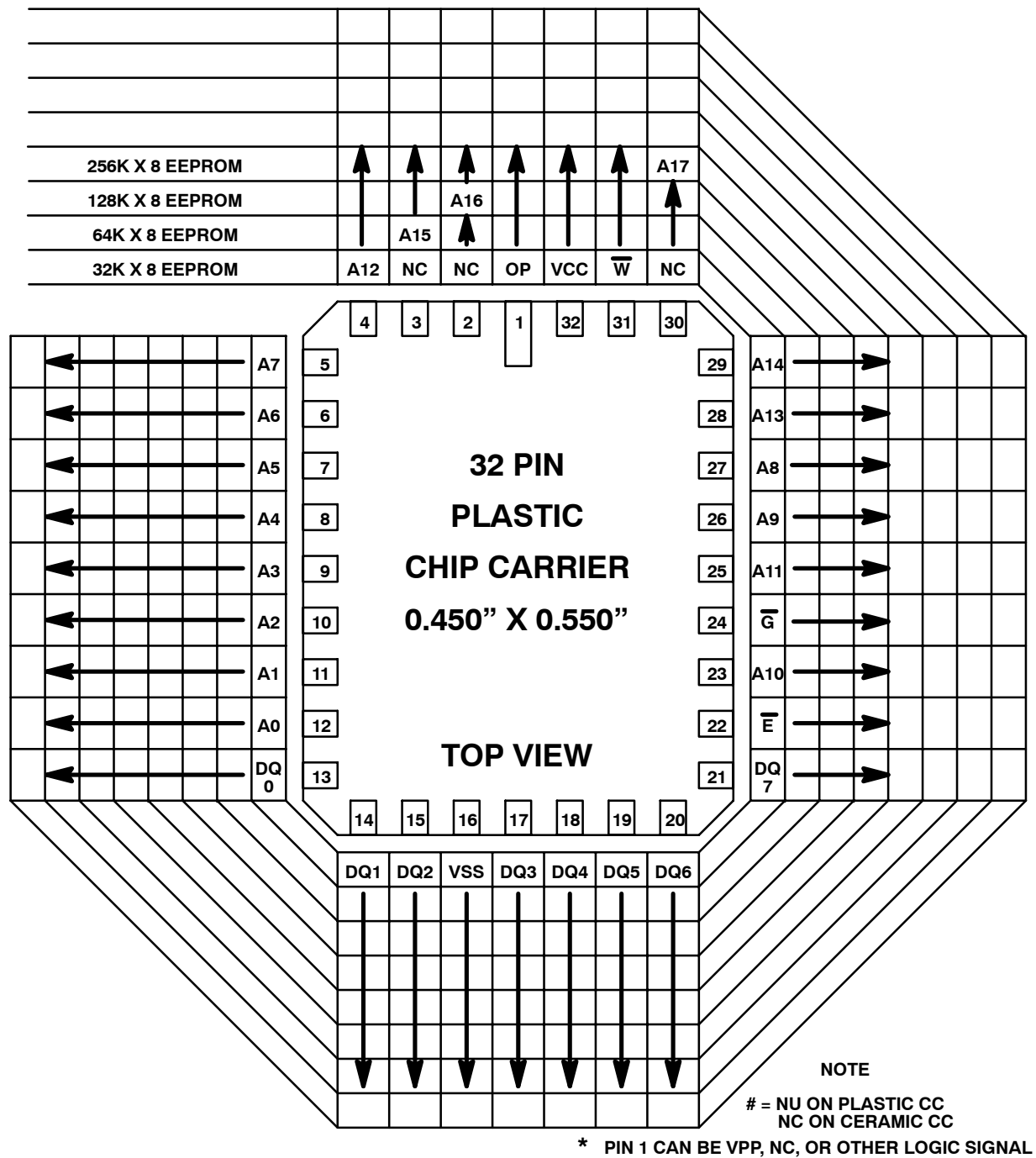
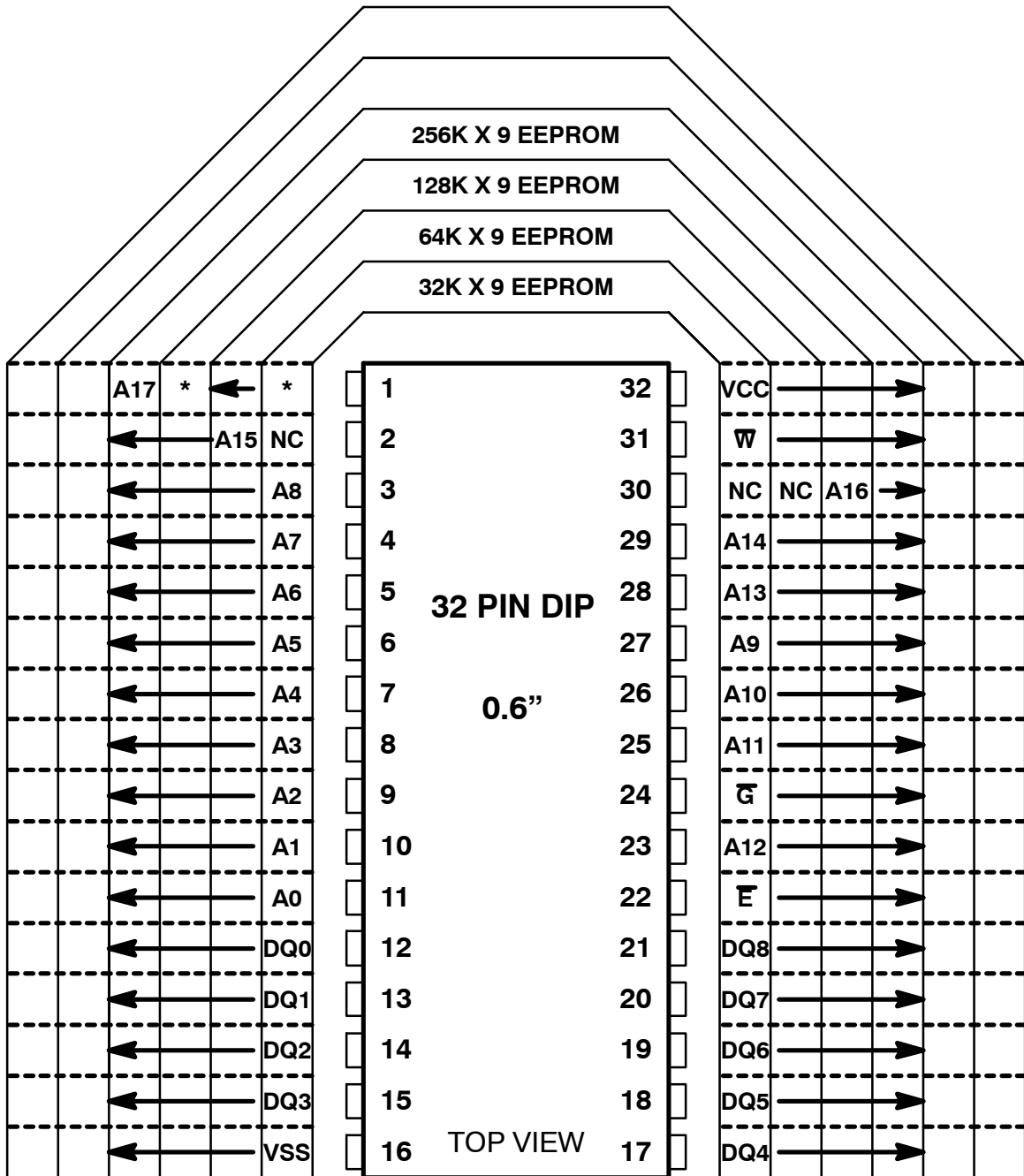


FIGURE 3.5.1-7
32K TO 256K BY 8 EEPROM FAMILY IN RCC



*** = PIN 1 CAN BE VPP, RY, NC, OR OTHER TTL INPUT**

FIGURE 3.5.1-8
32K TO 256K BY 9 EEPROM FAMILY IN DIP