

### 3.5.3 EEPROM EXTENDED FEATURES

There are a number of extended feature standards for EEPROMS that depend on the capacity and number of power supplies used in the design. The various standards and their location are listed as follows:

- 32K X 8 BIT EEPROM EXTENDED FEATURE STANDARDS. PP 3.5.1-15 to 22
- DUAL POWER SUPPLY EEPROM COMMAND SET. Fig. 3.5.3.2, P 3.5.3-13
- EXTENDED FEATURE SET FOR EEPROM (256Kb and larger) . Sec. 3.5.3.1 following
- SINGLE POWER SUPPLY EEPROM COMMAND CODES. SEC. 3.5.3.3
- EEPROM TOGGLE BIT FEATURE (larger than 256 Kb) . Sec. 3.5.3.4

### 3.5.3.1 - EXTENDED FEATURE SET FOR EEPROM (256Kb and larger)

This standard specifies features beyond the existing pinout standards that need to be standardized for EEPROMs to achieve operational compatibility. A summary of the required and optional features is listed below. The full standard follows the pinout drawings at the end of Sec. 3.5.3.2

#### 3.5.3.1.1 - REQUIRED STANDARD FEATURES

The following features are the minimum set necessary to achieve functional compatibility for 256Kb and larger EEPROMs and must be implemented to be in compliance with this standard:

- Operate with a primary power supply of 5.0 V and lower nominal
- Operate in conformance with the defines standard command set
- Operate in conformance with the standard truth table
- Have read and write timing cycles which are consistent with the standard timing diagrams
- Contain Data & Address Latches for Write cycles
- Operate with self timed write cycles
- Operate with input levels between 0 and 5 Volts.
- DATA\ Polling

#### 3.5.3.1.2 - OPTIONAL FEATURES

The following features are optional and are not required for the part to conform to this standard. If any of these features are implemented, they must operate as defined in order to maintain compatibility and to be in compliance with this standard:

- Page Write Mode with standard write cycle timings
- Minimum page size of 16 Byte in page write mode
- Software Data Protect Option
- Hardware Mass Erase (All 1's)
- Software Mass Erase (All 1's)

### 3.5.3.2 - OPTIONAL COMMAND SET FOR DUAL-SUPPLY EEPROM

This Standard provides an optional command set for DUAL-SUPPLY EEPROM devices. This set includes the existing algorithmic commands and adds a series of automatic codes. A component may respond to either or both of the operating modes. The COMMAND SET TRUTH TABLE is shown in Figure 3.5.1-11

### 3.5.3.3 - SINGLE POWER SUPPLY EEPROM COMMAND CODES

These tables define the three cycle and 6 cycle comand codes for SINGLE SUPPLY EEPROMs with capacities greater than 256 Kb.

### 3.5.3.4 - EEPROM TOGGLE BIT FEATURE

This standard is applicable to devices with a capacity greater than 256 Kb, with both single and dual power supplies. The Toggle Bit feature is used to determine if a Write Cycle (either Erase, Program, or both) is in progress in the EEPROM or if the part is available for reading or another write cycle.

### 3.5.3.5 - SYNCHRONOUS DRAM INTERFACE EEPROM (FLASH) IN 86-PIN TSOP-2 AND 90-BALL FBGA

This section provides the Mode Register Architecture (Figure A1-11) and Truth Tables 1 and 2.

### 3.5.3.6 - EEPROM with two SPD Software Write Protect Methods

This section describes two methods to software write protect the EEPROM.

## EEPROM EXTENDED FEATURE STANDARD (256Kb and greater)

The mandatory features, which are the minimum set necessary to achieve functional compability for 256Kb and larger EEPROMs, must be implemented to be in compliance with this standard. Any, all, or none of the optional features may be implemented at the manufacturers discretion. However, if an optional feature defined In this standard is implemented, it must operate as specltied in this standard to be in compliance with the standard.

Other features not described in the standard may be incorporated and the device still be in compliance as long as they are compatible wth the required and optional features in this standard.

### **BYTEWIDE EEPROM REQUIRED STANDARD FEATURES (256Kb and larger)**

1. VDD SUPPLY IS 5 V OR LESS NOMINAL
2. STANDARD LOGIC TRUTH TABLE (FIG. A1-1)
3. STANDARD COMMAND SET (Fig. A1-2)
4. STANDARD READ CYCLE TIMING (FIG. A1-3)
5. STANDARD BYTE WRITE CYCLE FEATURES
  - TIMING (FIG. A1-4)
  - DATA AND ADDRESS LATCHES
  - SELF-TIMED WRITE CYCLES
  - ALL INPUT LEVELS IN RANGE BETWEEN 0 V AND 5 V.
6. DATA POLLING (FIG. A1-5)
  - MUST MEET NORMAL READ CYCLE AND WRITE CYCLE TIMING

### **OPTIONAL FEATURES**

1. PAGE WRITE MODE (FIG. A1-6)
  - STANDARD PAGE WRITE CYCLE TIMING
  - 16 BYTE MINIMUM PAGE SIZE (A0 - A3)
2. SOFTWARE DATA PROTECT OPTION (FIGS. A1-7 & A1-8)
3. HARDWARE MASS ERASE (ALL 1'S) (FIG. A1-9)
4. SOFTWARE MASS ERASE (ALL 1'S) (FIG. A1-10)

| EEPROM TRUTH TABLE |                |                |                           |        |         |
|--------------------|----------------|----------------|---------------------------|--------|---------|
| $\overline{E}$     | $\overline{G}$ | $\overline{W}$ | MODE                      | DQ     | POWER   |
| L                  | L              | H              | READ                      | Q      | ACTIVE  |
| L                  | H              | L              | WRITE                     | D      | ACTIVE  |
| H                  | X              | X              | STANDBY AND WRITE INHIBIT | HIGH Z | STANDBY |
| L                  | L              | L              | WRITE INHIBIT             | HIGH Z | ACTIVE  |
| L                  | H              | H              | WRITE INHIBIT             | HIGH Z | ACTIVE  |

~NOTE:  $\overline{G}$  functions as both an output control and a write Inhibit control in this EEPROM Standard.

**FIGURE A1-1**

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## SINGLE-SUPPLY EEPROM COMMAND SET

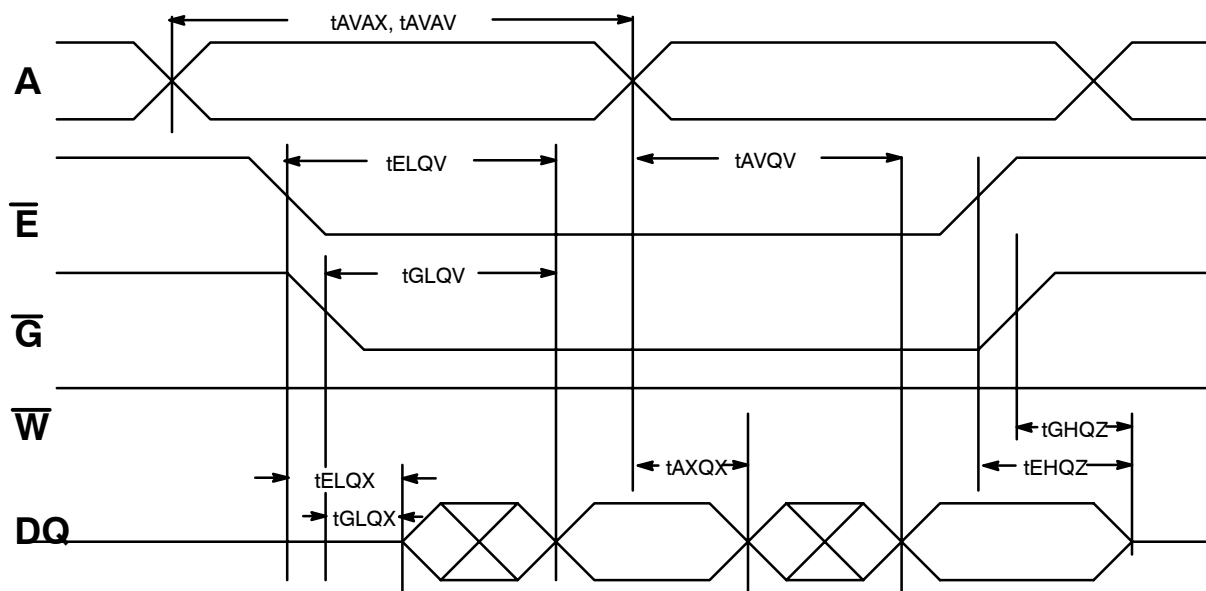
**Bus Command Table**

| Command Sequence     | Bus Write Cycles Req'd | First Bus Write Cycle                                                         |      | Second Bus Write Cycle |      | Third Bus Write Cycle |      | Fourth Bus Read/Write Cycle |      | Fifth Bus Write Cycle |      | Sixth Bus Write Cycle |      |
|----------------------|------------------------|-------------------------------------------------------------------------------|------|------------------------|------|-----------------------|------|-----------------------------|------|-----------------------|------|-----------------------|------|
|                      |                        | Addr                                                                          | Data | Addr                   | Data | Addr                  | Data | Addr                        | Data | Addr                  | Data | Addr                  | Data |
| Read/Reset           | 1                      | XXH                                                                           | F0H  |                        |      |                       |      |                             |      |                       |      |                       |      |
| Read/Reset           | 4                      | 555H                                                                          | AAH  | 2AAAH                  | 55H  | 555H                  | F0H  | RA                          | RD   |                       |      |                       |      |
| Autoselect           | 4                      | 555H                                                                          | AAH  | 2AAAH                  | 55H  | 555H                  | 90H  |                             |      |                       |      |                       |      |
| Byte Program         | 4                      | 555H                                                                          | AAH  | 2AAAH                  | 55H  | 555H                  | A0H  | PA                          | Data |                       |      |                       |      |
| Chip Erase           | 6                      | 555H                                                                          | AAH  | 2AAAH                  | 55H  | 555H                  | 80H  | 555H                        | AAH  | 2AAAH                 | 55H  | 555H                  | 10H  |
| Sector Erase         | 6                      | 555H                                                                          | AAH  | 2AAAH                  | 55H  | 555H                  | 80H  | 555H                        | AAH  | 2AAAH                 | 55H  | SA                    | 30H  |
| Sector Erase Suspend |                        | Erase can be suspended during sector erase with Addr (don't care), Data (B0H) |      |                        |      |                       |      |                             |      |                       |      |                       |      |
| Sector Erase Resume  |                        | Erase can be resumed after suspend with Addr (don't care), Data (30H)         |      |                        |      |                       |      |                             |      |                       |      |                       |      |

Note: A0 is always LSB regardless of data width.

**FIGURE A1-2**

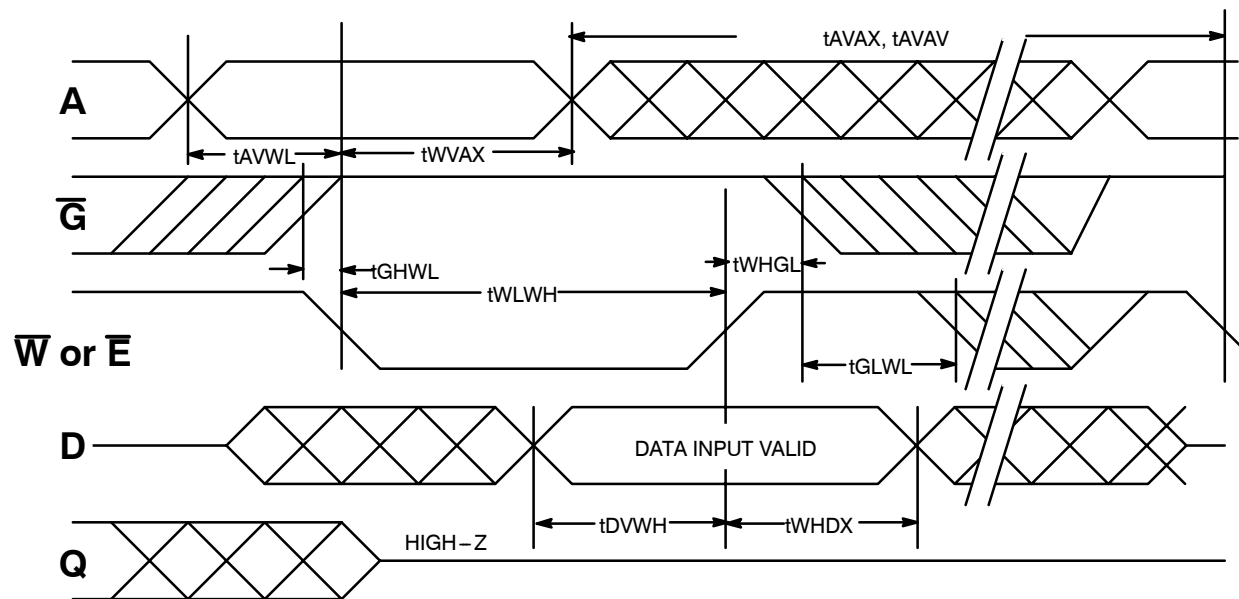
## SINGLE SUPPLY EEPROM READ CYCLE TIMING



| SYMBOL               | DESCRIPTION                                                    |
|----------------------|----------------------------------------------------------------|
| $t_{AVAX}, t_{AVAV}$ | ADDRESS VALID TO ADDRESS CHANGE (READ CYCLE TIME)              |
| $t_{ELQV}$           | $\overline{E}$ LOW TO OUTPUT VALID (CHIP ENABLE ACCESS TIME)   |
| $t_{AVQV}$           | ADDRESS VALID TO OUTPUT VALID (ADDRESS ACCESS TIME) $t_{GLQV}$ |
| $t_{ELQX}$           | $\overline{E}$ LOW TO ACTIVE OUTPUT                            |
| $t_{GLQX}$           | $\overline{G}$ LOW TO ACTIVE OUTPUT                            |
| $t_{EHQZ}$           | $\overline{E}$ HIGH TO HIGH-Z OUTPUT                           |
| $t_{GHQZ}$           | $\overline{G}$ HIGH TO HIGH-Z OUTPUT                           |
| $t_{AXQX}$           | ADDRESS INVALID TO DATA OUT INVALID                            |

FIGURE A1-3

SINGLE SUPPLY EEPROM READ CYCLE TIMING



| SYMBOL (NOTE 1) | DESCRIPTION                                                                                                |
|-----------------|------------------------------------------------------------------------------------------------------------|
| tWLWL, tLEL     | $\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW CYCLE TIME (WRITE CYCLE TIME) |
| tAVWL, tAVEL    | ADDRESS VALID TO $\overline{W}$ OR $\overline{E}$ LOW TIME (ADDRESS SETUP TIME)                            |
| tWLAX, tELAX    | $\overline{W}$ OR $\overline{E}$ LOW TO ADDRESS INVALID (ADDRESS HOLD TIME)                                |
| tGHWL, tGHEL    | $\overline{G}$ HIGH TO $\overline{W}$ OR $\overline{E}$ LOW TIME                                           |
| tWHGL, tEHGL    | $\overline{G}$ HIGH HOLD TIME FROM $\overline{W}$ OR $\overline{E}$ HIGH                                   |
| tWLWH, tLEH     | $\overline{W}$ OR $\overline{E}$ LOW TO $\overline{W}$ OR $\overline{E}$ HIGH (WRITE PULSE DURATION)       |
| tGLWL, tGLEL    | $\overline{G}$ LOW TO $\overline{W}$ OR $\overline{E}$ LOW ( $\overline{G}$ LOW WRITE INHIBIT SETUP TIME)  |
| tDVWH, tDVEH    | DATA INPUT VALID TO $\overline{W}$ OR $\overline{E}$ HIGH (DATA SET-UP TIME)                               |
| tVHDX, tEHDX    | $\overline{W}$ OR $\overline{E}$ HIGH TO DATA INPUT INVALID (DATA HOLD TIME)                               |

FIGURE A1-4