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**Terminology and Methods of Measurement for
Bistable Semiconductor Microcircuits**

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TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS

A Guide to the Use of EIA Format MED-32-3A, "Registration Data
for Semiconductor Integrated Bistable Logic Circuits"

This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for Semiconductor Integrated Bistable Logic Circuits. The purpose of this bulletin is to provide guidance at each section of the format. This guidance is given as an explanation as to the intent of the particular section referenced and direction in using the particular section.

1.0 General

This format is intended for the registration of semiconductor integrated bistable logic circuits including monolithic, multichip, film and hybrid bistable circuits.

A semiconductor integrated logic circuit is a single package circuit in which:

- a. No external elements are required to perform the registered function;
- b. The contained elements are inseparably associated;
- c. The contained elements are tested and used as logic circuits.

1.0 General (continued)

A bistable logic circuit is defined as one having an output which can be at either of two levels (an output which is stable in two states). Its output is indefinitely stable after removal of the input signal which caused it to go to that level. This differentiates it from a logic gating circuit whose output has two possible levels but which requires the retention of the input signals to retain the output level. This also differentiates the bistable circuit from the monostable and astable circuits.

The state of a bistable refers to a particular and specified pin (Para. 2.1 of format). This pin can, under normal operation, be at one of two levels. The voltage (or current) at that pin is normally and discretely at a high or low level. In positive logic the "HIGH (H)" voltage (or current) level is the more positive than the "LOW (L)" voltage (or current) level. If the pin specified in Para. 2.1 is at the "HIGH" level, then the bistable is in the "HIGH" state.

In the format when reference is made to the state of the bistable the pin specified in Para. 2.1 of the format is considered. In bistables having an output which must be gated so that the state of the bistable can be determined, where reference is made to the state of the bistable, it is assumed that the circuit is gated so that the state of the bistable will be reflected at the output.

This format is written to include all logical forms of bistable circuits. It is also intended to be used for registration of all circuit configurations used to achieve the variety of logical forms of bistable circuits.

1.0 General (continued)

Therefore, some parameters are not applicable to some forms of bistable circuits. (For example; clock and synchronous parameters are not applicable to bistables having only asynchronous inputs.) In cases where a parameter is not applicable to a particular circuit being registered it should be so stated on the registration and sound technical justification supplied with the request for registration. Where a circuit to be registered has terminals which are not specifically covered by this format, those terminals must still be specified using this format as a guide.

1.1 Type of device

The type of semiconductor material used should be registered.

1.2 Type of logic function and polarity

The format is intended to cover registration of single and multiple bistable logic circuits in a single package. Where multiple circuits are included in one package they should be specified separately if the bistables have different logic, function or circuit. If all bistable circuits in the package are of the same type it should be so noted in sections 2.0 and 5.0 which parameters apply to each device and which parameters apply to the total package.

1.3 Inputs

For the purpose of registration, bistable circuits are considered to have three types of inputs into which signals may be introduced. Further expansion of the following section is recommended if there is a variety of any one type of input.

1.3.1 Clock

That terminal(s) whose condition or change of condition is intended to control the acceptance or rejection of signals applied to the synchronous terminal(s) and/or the output state of the

1.3.1 Clock (continued)

bistable.

1.3.2 Synchronous

That input(s) whose data is accepted and affects the output state of the bistable by the condition or change of conditions on the clock terminal(s). Once the data has effected the output state of the bistable subsequent changes cannot be made until the clock terminal(s) goes through the registered sequence.

1.3.3 Asynchronous

That input(s) which is intended to affect the output state of the bistable device independent of the condition or change of condition on the clock terminal(s). Asynchronous inputs may require that the clock terminal(s) be at a prescribed level but once this level is obtained the asynchronous inputs can change the bistable output state without further regard to the clock.

1.3.4 Additional Inputs

If the bistable has inputs which fit none of the categories of 1.3.1, 1.3.2, 1.3.3, such as, gating functions; then they should be noted here and their function described.

4 Output(s)

Every terminal from the bistable logic circuit which is used to drive or provide signals to other logic elements or devices shall be classified as an output. The intent of this section is to define how these outputs may be used logically. The registration shall call out those outputs which can be connected with similar outputs to do logic. If the state of the bistable logic circuit can be changed by applying signals to the outputs this should also be called out.

1.4 Output (s) (continued)

This indicates the degree of isolation between the output and the bistable portion of the bistable logic circuit.

2.0 LOGIC - GENERAL

The logic of switching circuits deals with variables which can take on only one of two states. The states which can exist on a terminal or a signal line shall be referred to as the LOW state and the HIGH state. A circuit can be characterized either with positive logic or negative logic; actually both can be applied to any device. But, if a circuit is intended to be used predominantly with one or the other logic conventions then it should be registered in that fashion. It should be noted that the logic could (not must) be restated for the opposite logic convention.

If all signal line terminals in a logic diagram of a device have the same pair of physical states and if the more positive potential (current) is consistently selected as the HIGH level, the logic description of the device is said to have positive logic.

If the less positive potential (current) is consistently selected as the HIGH LEVEL, the device is said to have negative logic. Positive logic is assumed for this format. If negative logic is required by application, it must be so stated.

2.1 Logic Diagram - General

Logic diagrams are graphical symbols which describe devices or systems which contain only two-state variables.

The purpose of providing a logic diagram in this format is to assist the user in understanding the operation of the device without needing to refer to or completely understand the electrical equivalent circuitry involved in implementing the device. Note that the bistable device as a black box is the subject of registration by this format rather than



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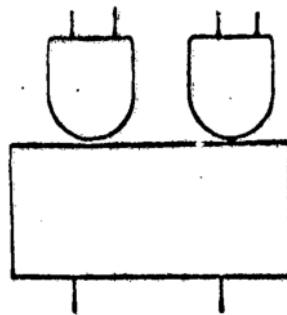
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2.1 Logic Diagram - General (continued)

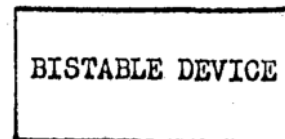
the circuitry used to implement the device. A logic diagram should provide the user with as much information regarding device use as is possible.

Logical Sub-Functions

In many bistable devices some logical sub-function is performed on the synchronous (or other) inputs. Standard graphical symbols for these sub-functions as outlined in ^{USASI} Y32.14 should be used (the rectangular block used herein to represent a bistable device is in accordance with this document). Consider a bistable device in which a two input AND function is performed at the synchronous inputs. Such a case can best be diagrammed as shown below.



Inputs applied here



Outputs shown here

Component Symbols

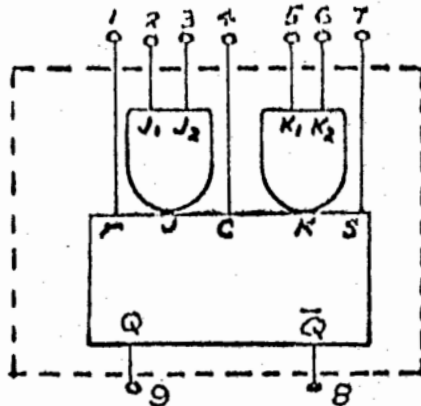
Use of component symbols (transistors, capacitors, etc.) to clarify the diagram is admissible only when the operation cannot be described by standard logic symbols alone.

Pin Numbering of Terminals

In order to make the logic diagrams fully representative of the device, pin numbers should be given for all logic inputs and outputs. Supply voltage pin and ground pin numbers as well as numbers of unused (no connection) pins for completeness,

2.1 Logic Diagram - General (continued)

as shown below.



10 - V_{cc1}

11 - V_{cc2}

12 - GND

13 - No Connection

14 - No Connection

Note that letter symbols representing logic functions have been added within the device. Since agreement has not been reached regarding standardization of these symbols, use of them is not required. If symbols are used, they should be among those "commonly used" if possible. A helpful reference in the determining of symbols is "Logical Design of Digital Computers" by M. Phister. In general, use of different print to distinguish between synchronous and asynchronous inputs would be helpful if possible. Upper and lower case have been used herein to distinguish synchronous and asynchronous inputs respectively.

2 Truth Table(s) - General

The truth table is a chart which tabulates all the combinations of possible states of the logic variables of the device. Standard form is to place the combination of input states on the left of a double line and the resulting output states on the right of a double line.

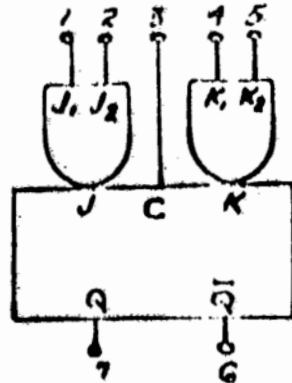
The purpose of the truth table is to provide the user with logic input-output information at a glance.

2.2 Truth Table(a) - General (continued)

Pin Designations

All pertinent logic terminals should be identified with respect to pin number. It is also useful if the terminal LOGIC SYMBOL is used.

Consider a J-K flip flop for which the logic diagram is



- 8. Reset (r) (Asynchronous)
- 9. Open
- 10. V_{CC}
- 11. GND
- 12. Set (s) (Asynchronous)

The truth table heading should be:

Logical Inputs					Logical Outputs		Conditions on other pins for which the truth table is valid	
Pin Number	1	2	4	5	6	7	Pin No.	Condition
Letter Symbol	J1	J2	K1	K2	$\bar{Q}$	Q		
							8	"H" - level
							9	N. C.
							10	6.0 Volts
							11	GND
							12	"H" - level
							3(n)*	"L" - level

*See Sections 2.2.1 and 2.2.2

n refers to pre-activating condition of the clock.

Note that Pin 3 (clock) is not considered to be a logical input but rather an activating input.

2.2 Truth Table(s) - General (continued)

Since the bistable device has complementary outputs (although only one may be available), it is not necessary to show the state of both on the truth table. Hence the column headed pin 6, for example, could be omitted without loss of clarity.

2.2.1 &

2.2.2 Distinction between Synchronous and Asynchronous Tables

A basic difference between the synchronous and asynchronous modes of operation is that the asynchronous inputs cause as well as determine the state of a device, whereas the synchronous inputs determine the state of the output only after a clock signal has been applied. Hence the time delay between asynchronous input variations and output variations is determined by the speed of the circuit and is, for all intents and purposes, insignificant. In the case of the synchronous mode all one can say is that there is, of necessity, some time differential between the arrival of synchronous input information, the establishment of the activating condition of the clock, and the time at which the output takes on the state determined by the synchronous input. Since clarity is of utmost concern in establishing the truth table, it is recommended that this time differential be expressed as part of the functional symbol.

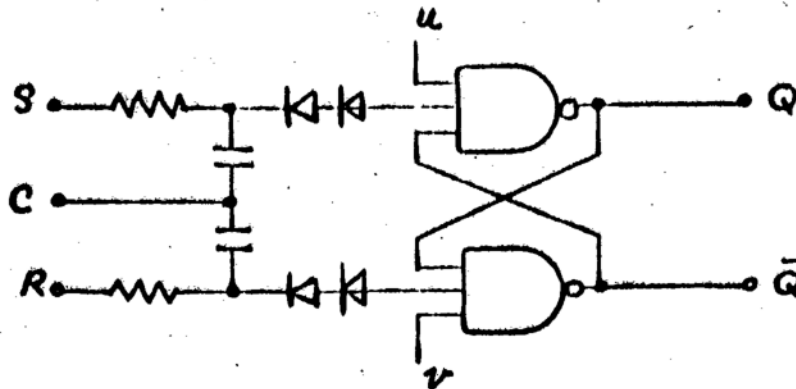
By choosing n to connote the state of a signal line at time n before the occurrence of an activating (or clock) signal and choose $n+1$ to connote the state of a signal line after the activating signal has affected the device, a distinction between the synchronous and asynchronous truth tables can be readily attained.



2.2.1 &

2.2.2 Distinction between Synchronous and Asynchronous Tables (continued)

Consider a synchronous R-S flip-flop (Phister) with asynchronous preset and clear inputs which will be referred to as u and v respectively. Assume the circuitry used in implementing this device is that shown below.



Examination of the operation of such a device serves to highlight some important considerations in developing a complete truth table.

Synchronous Mode

The device is activated by the negative going transition of the clock. If a HIGH level exists on S and R, the clock transition has no effect. If a LOW level exists on either S or R, the negative transition of the clock steals base current from one of the gates and that gate must go to the HIGH level releasing the input to the other gate which allows it to go to the LOW level. Note that u and v must be in the LOW level for this to occur.

If both R and S are in the LOW level when the clock negative transition occurs, an equivalent LOW level is applied dynamically to both NAND gate inputs forcing both outputs to the HIGH level but when the current stops flowing through the capacitors, the LOW levels are released and the HIGH levels (cross-coupled from the output)

- 11 -

2.2.1 &

2.2.2

Distinction between Synchronous and Asynchronous Tables (continued)

at the inputs try to force the outputs to LOW. For rather obvious reasons, the output levels of two cross-coupled NAND gates cannot exist in the LOW level simultaneously; a race occurs and it cannot be predicted which output will reach the LOW level first and the state of the output is indeterminate. The truth table which describes the effect is given below:

SYNCHRONOUS MODE

R_n	S_n	Q_{n+1}
L	L	Indeterminate
H	L	H
L	H	L
H	H	Q_n (Does not change)

In most cases it is assumed that the last level on the synchronous inputs just before the activating edge of the clock is the one that will be recognized. However, in some bistable designs some level prior to that existing at the clock edge may be recognized. In the circuit shown on Page 10, if the clock goes high and the S or R terminal momentarily goes to "L" the capacitor will charge and may not discharge before the clock edge even though the input goes back to "H" and the clock will recognize the "L". The truth table should note this by a footnote which says "will store a momentary 'L' (or 'H') level."

Asynchronous Mode

For the asynchronous Mode of operation, the truth table describing the operation is given below:

u_n	v_n	Q_n	$\bar{Q}_n$
L	L	H	H
H	L	L	H
H	H	Q_n	$\bar{Q}_n$ (Does not change)

2.2.1 &

2.2.2 Distinction between Synchronous and Asynchronous Tables (continued)

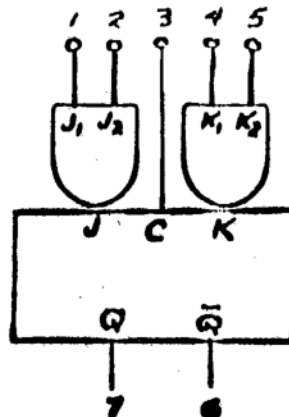
A subtlety which exists, however, is that the sequential combination of $u_n = L, v_n = L$ to $u_n = H, v_n = H$ leads to an indeterminate state much in the same way that an indeterminate state resulted from the applications of $S_n = H, R_n = H$ in the synchronous mode. This can be demonstrated in truth table form the following way:

Inputs				Output
$t = t_0$		$t = t_{0+1}$		$t = t_{0+1}$
u	v	u	v	Q
L	L	H	H	Indeterminate

Such a condition should be specified in truth table form or as a footnote to the truth table because it is the purpose of the truth tables to show all possible logic combinations even (and perhaps essentially) those which reflect limitations of the device.

Sub-Function Truth Tables

If the device can be broken down into a basic logical cell or groups of cells, much confusion in interpretation of the tables can be avoided. Consider again the example given in paragraph 2.2.1



2.2.1 &

2.2.2 Distinction between Synchronous and Asynchronous Tables (continued)

Sub-Truth Tables such as these:

1	2	-	4	5	-	-	-	7
J ₁	J ₂	J	K ₁	K ₂	K	J _n	K _n	Q _{n+1}
L	L	L	L	L	L	L	L	Q _n
L	H	L	L	H	L	L	H	L
H	L	L	H	L	L	H	L	H
H	H	H	H	H	H	H	H	Q _n

Replace the More Cumbersome

1	2	4	5	7
J ₁	J ₂	K ₁	K ₂	Q _{n+1}
L	L	L	L	Q _n
L	L	L	H	Q _n
L	L	H	L	Q _n
L	L	H	H	L
L	H	L	L	Q _n
L	H	L	H	Q _n
L	H	H	L	Q _n
L	H	H	H	L
H	L	L	L	Q _n
H	L	L	H	Q _n
H	L	H	L	Q _n
H	L	H	H	L
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	Q _n

2.3 Logic Equations - General

Logic equations must be interpreted by the Boolean Algebra. The number of levels a logic variable may take on is two. These are commonly referred to as ZERO (0) and ONE (1), and have been standardized as LOW (L) and HIGH (H). A function is said to be HIGH if the equation which characterizes it equals HIGH. Rules for manipulating the equations are given in many texts and so will not be related here. The purpose of the logic equation is to aid the user in establishing those interrelationships between inputs and outputs which determine a

2.3 Logic Equations - General (continued)

specified level of the output.

Boolean Algebra

does not recognize time as a variable; hence, in the algebra the aforementioned symbols Q_n and Q_{n+1} may be treated as different functions even though the function refers to the same terminal or signal line.

2.3.1 The Logic Equation and the Truth Table

The logic equation supports the truth table in asserting the conditions required to obtain a HIGH (H) at the output either at time $(n+1)$ in the case of synchronous operation, or at time n in the case of asynchronous operation. Separate logic equations should describe the "don't care" conditions such as illogical entries or entries which lead to indeterminate outputs. In order to fully support the truth table, therefore, equations which define input restrictions should also be provided.

SYNCHRONOUS MODE

Consider the synchronous mode of operation of the bistable device discussed in Section 2.2.1/2.2.2. The truth table is:

S_n	R_n	Q_{n+1}
L	L	Q_n
L	H	L
H	L	H
H	H	(Indeterminate)

The logic equation which specifies when $Q_{n+1} = 1$ is

$$Q_{n+1} = \bar{S}_n \cdot \bar{R}_n \cdot Q_n + S_n$$

which reduces to

$$Q_{n+1} = \bar{R}_n \cdot Q_n + S_n$$

(Simplest Form)

If we plug in the values $R_n = H$, $S_n = H$ into this equation, it would appear that Q_{n+1} becomes HIGH for this condition. The equation which is required to fully support the truth table



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2.3.1 The Logic equation and the truth table (continued)

is given as INPUT RESTRICTION: $S_n = R_n = L$

Note that logic equations in their simplest form are most useful to the logic designer. Details of the device are available to him from the logic diagram and the truth table.

ASYNCHRONOUS MODE

Consider now the asynchronous mode of operation for which the truth tables are:

u_n	v_n	Q_n	$\bar{Q}_n$	$t=t_0$			$t=t_{0+1}$		
L	L	H	H (indeterminate)	u	v		u	v	Q
H	L	L	H	L	L		H	H	Indeterminant
L	H	H	L	(Sequential-combinational)					
H	H	Q_n	$\bar{Q}_n$ (no change)						

(combinational)

Note that outputs are directly dependent on inputs whereas table on the right is dependent on the sequence of input signals.

Logic equations supporting these truth tables are:

$$Q_n = \bar{u}_n + u_n v_n Q_n$$

$$\bar{Q}_n = \bar{v}_n + u_n v_n \bar{Q}_n$$

The input restriction may be expressed in an equation as follows:

$$\left((\bar{u}_n \cdot \bar{v}_n) \right)_{t=t_0} \cdot \left((u_n \cdot v_n) \right)_{t=t_{0+1}} = L$$

Recognizing that the first line of the truth table shows both outputs to be in the same level at the same time, the rather common practice of naming these two outputs with the same letter symbol, except for the complement bar on the one, must be used with caution.

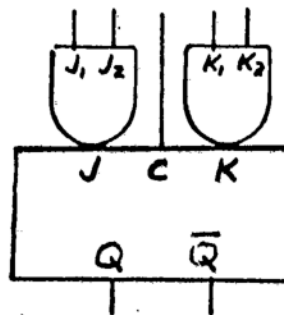
2.3.2 Functional Designations

Use of pin numbers in logic equations could conceivably cause difficulty, for example, $6_{n+1} = \bar{3}_n 6_n + 2_n$, $2_n 3_n = L$ is less meaningful to the logical designer than $Q_{n+1} = \bar{R}_n Q_n + S_n$, $S_n R_n = L$. Hence it is recommended that logic equations be given in terms of commonly used symbology for logic functions, if possible.

2.3.3 Multiple Inputs to Flip-Flops

Consider the case where there are two input AND gates driving the J-K inputs to a flip-flop.

i.e.,



$$\text{Either } Q_{n+1} = \bar{Q}_n J_n + Q_n \bar{K}_n, \quad J = J_1 J_2, \quad K = K_1 K_2$$

$$\text{Or } Q_{n+1} = \bar{Q}_n J_{1n} J_{2n} + Q_n \overline{K_{1n} K_{2n}}$$

are acceptable

Of course this should be done in a similar fashion to the way the truth tables are structured.

2.3.4 Distinguishing Between Modes of Operation

Since synchronous and asynchronous refer to two different modes of operation, separate logic equations should be used. A hypothetical example is given below:

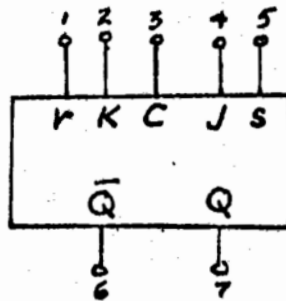
Synchronous

$$Q_{n+1} = \bar{Q}_n J_n + Q_n \bar{K}_n$$

Asynchronous

$$Q_n = s_n + \bar{r}_n Q_n$$

$$s_n r_n = L$$



3.0 Mechanical Data (No Comments)

4.0 Maximum Limits

A maximum limit is a limiting value of voltage, current and/or temperature which is to be exceeded only at the risk of permanently altering the characteristics of the bistable. A combination of maximum limits cannot normally be attained simultaneously.

4.1 Temperature

4.1.1 Storage Temperature Range defines the range of environment in which a bistable may be stored with no electrical connections to the device.

4.1.2 Temperature Range under Bias defines the temperature range in which the bistable may be operated when it is in a normal operating mode. One should be cognizant of the fact that if operating temperature range is specified, electrical characteristics must be registered at the temperature extremes.

4.2 Terminal Voltage and/or Current defines the maximum voltage and/or current that may be safely applied to each terminal of the bistable over the specified temperature range. Each of these maximum values are defined independently of all others. For example, if a maximum output supply voltage is specified to be 8 volts and a maximum output current is specified to be 30 mA, the 8 volt and 30 mA conditions cannot be applied simultaneously.

5.0 Electrical Characteristics

In this portion of the format the parameters and the characteristics of the registered circuit are defined under specified conditions. Each parameter is verified by limits shown for each test. The conditions are clearly defined for each test. It should be noted that there is no inference or requirement that the tests be performed by the registrant or other manufacturers of the registered device. The format merely says that one would expect the electrical characteristics of the device to be equal to or better than the individual parameter limits shown under the conditions shown.

The electrical characteristics are divided into four broad sections.

5.1 Operating conditions for normal use

5.2 Static characteristics

5.3 Dynamic characteristics

5.4 Power characteristics

Current and Voltage Convention for registering bistable circuits

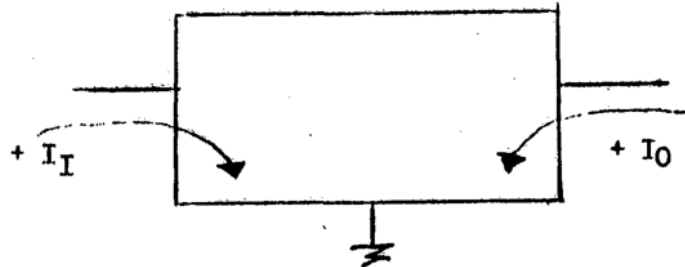
A. Currents

Direction and Sign

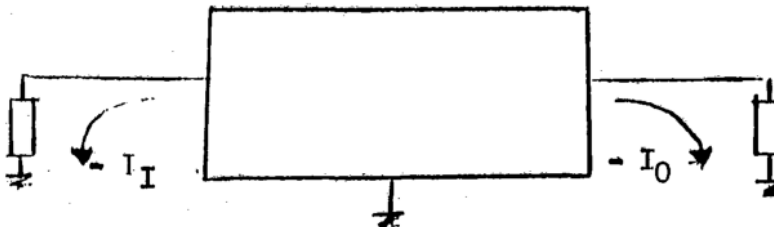
Current is called positive when current flows into a terminal.

This is true regardless of whether it is an input or an output.

The following diagram shows positive current



The following diagram shows negative current



Magnitude - For purposes of registration the magnitude only is considered when comparing a current. Therefore, a maximum current which is negative is its greatest magnitude. (-10mA is larger than -1mA). Where a parameter limit is a maximum negative current, any magnitude, without regard to sign, less than the limit is permissible.

B. Voltage

Direction and Sign

A voltage is always measured in relation to a reference point.

This is generally ground or a common pin. The positive terminal is that one into which electrons flow when the two terminals are

B. Voltage (continued)

connected together. A voltage can then be positive or negative in relation to the specified terminal or reference.

Magnitude

Just as in current, sign is not considered when ranking magnitude. -10V is larger than -1 volt

5.1 Operating Conditions

This section describes the power supply voltages and temperature for which operation is claimed. In addition it describes the test technique used to verify proper operation.

5.1.1 Nominal Supply Voltages

While a circuit may operate over a range of power supply voltages, it is generally true that optimum operation occurs at a specific voltage. Show here the nominal supply voltages to be applied and denote the pin to which it is applied. It is intended that the voltages be referenced to a common ground pin; if this is not true, it should be clarified here. The registrant may add other definitions such as percent or magnitude variation permissible.

5.1.2 Operating Temperature

This will define the restrictions on the devices capability to operate within the temperature spectrum.

5.1.2.1 This describes the definition of the 25°C condition as to whether it is ambient or case. Either condition may be used to define the electrical characteristics.

5.1.2.2 If operation is claimed or permitted over a temperature range then static characteristics must be defined for that temperature range.

5.1.2.3 To permit flexibility in testing techniques and still provide good definition of the registered device a choice of stabilized D.C. or pulsed D.C. testing is permitted. Whichever is used must be defined to permit interchangeability.

D.C. Stabilized tests are made after all transients induced by operating conditions have ended. Electrical and Thermal stability have been reached.

Pulsed, the electrical conditions for testing the parameter have been applied long enough to reach electrical stability but the thermal condition may not have stabilized. In fact, the converse is often considered true, that is, the thermal conditions are considered to be the same as they were before any electrical conditions were introduced. This concept is generally applied for automatic, high speed testing. It is obvious that for repeatability and interchangeability the time and duty cycle of the applied voltages are very important and must be defined here. Even though the measurement technique is defined as pulsed the parameters measured are still considered to be the static characteristics.

5.2 Static Characteristics

This section defines parameters which are measured at the time the



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5.2 Static Characteristics (continued)

bistable device is in a stable electrical logical state. This stable state will be the result of a static input and output applied electrical conditions. To achieve the required state may have taken a sequence of electrical conditions (pulses) or it may have been achieved by statically forcing the condition through input or output terminals. Regardless of the technique used, time is not considered a variable; the parameter measurement is unaffected by time (except as described in 5.1.2.3).

The introductory paragraph in the format for this section provides expansion of its intent.

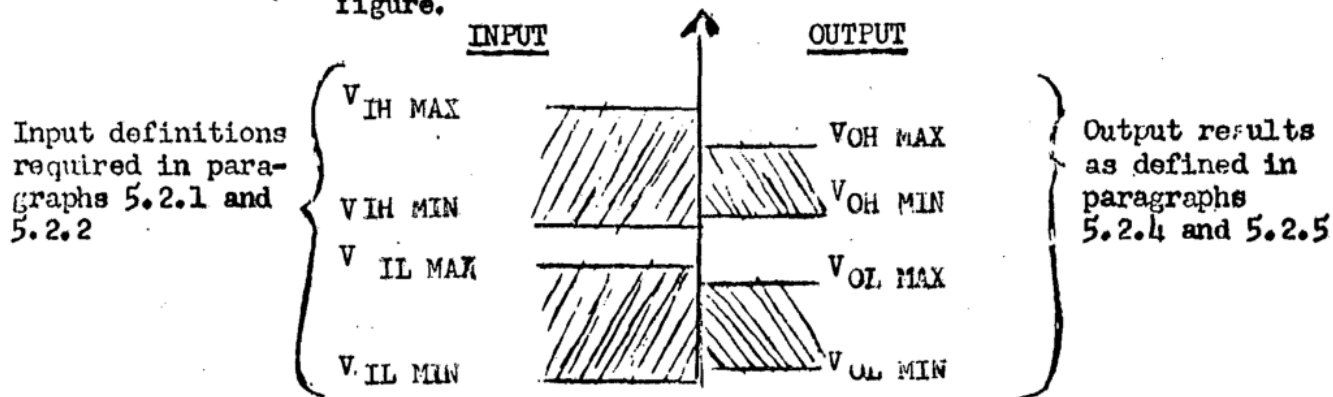
5.2.1 & 5.2.2 These sections are input logic voltage level definitions.

This is the starting point of the registration of all electrical parameters. They are, by nature, definitions of the maximum and minimum LOW (L) and HIGH (H) voltage levels which will be accepted and recognized by the registered device. These do not appear as parameters in the format. The validity of the definitions is proven by using them as conditions and verifying that they do result in proper logical operation according to the truth tables of paragraph 2.2. They are used in the static and Dynamic characteristic sections.

Care should be taken not to confuse the definitions in these paragraphs [5.2.1 ($V_{IL\ MAX}$ and $V_{IL\ MIN}$) and 5.2.2 ($V_{IH\ MAX}$ and $V_{IH\ MIN}$)] with the output parameters of paragraphs 5.2.4 (V_{OL}) and 5.2.5 (V_{OH}). The definitions in 5.2.1 and 5.2.2 when applied as described in 5.2.4 (and subsequently in paragraphs 5.3.2, 5.3.3 and 5.3.4 of the

5.2.1 & 5.2.2 (continued) dynamic characteristics) will result in the specified output levels. It can be said that the definitions of 5.2.1 and 5.2.2 are the range of input conditions and will result in the range of output levels shown in 5.2.4 and 5.2.5.

Generally the output levels of a bistable are intended to be compatible with its input requirements. The bistable is intended to drive other bistables like itself or other logic elements in the same family having the same input requirements. Therefore, a relationship generally exists as depicted in the following figure.



It is possible that different types of inputs (paragraph 1.3) may have different ranges of permissible Logical input voltages. The asynchronous may be different than the synchronous, etc. Where this is true the definitions must be shown by pin #.

5.2.3 Reference Voltage

If the registered bistable device requires a reference voltage, it will be defined here. The registrant has the option of defining a reference voltage (and its tolerance) for all tests at each temperature or specifying the reference voltage at each parameter

5.2.3 Reference Voltage (continued)

If the latter choice is made then the tolerance for these reference voltages should be shown in 5.2.3 (b).

5.2.4 V_{OL}

This characteristic is intended to define the maximum (5.2.4.1) and minimum (5.2.4.2) LOW level of the bistable output(s) under worst case conditions of input levels and output loading.

In 5.2.4.1, $V_{OL\ MAX}$ is defined for two conditions. First, in 5.2.4.1.1, V_{OL} maximum is determined under normal internal stable conditions. All inputs (asynchronous and synchronous) are at worst case levels for this stable state, but are not intended to force the state. In 5.2.4.1.2, the output state is forced and held by asynchronous inputs which are then at their worst case levels. Para. 5.2.4.1.1 applies to any type of bistable circuit and must be specified whereas 5.2.4.1.2 may or may not be applicable depending on the particular type of circuit. Figure 5.2.4.1 shows two examples of applying 5.2.4.1.1 and 5.2.4.1.2 to basic RTL and DTL bistable circuits.

The V_{OL} minimum is defined in 5.2.4.2 and (as is the case for logic gates) this characteristic is primarily intended for ECL type circuits although it is equally applicable to other types. However, in cases such as DTL it is recommended to specify this characteristic as zero volts rather than determine the actual minimum. In any case, all inputs must be at that worst case level which will make the output level in question a minimum, either holding or not holding the bistable in this state, whichever is worse. For a specific ECL circuit example, see Figure 5.2.4.2.

5.2.5 V_{OH}

This characteristic is intended to define the maximum (5.2.5.2) and minimum (5.2.5.1) HIGH level of the bistable output(s) under worst case conditions of input levels and output loading.

For (5.2.5.1) V_{OH} minimum is again defined for two conditions in a similar manner as in 5.2.4.1. The first (5.2.5.1.1) is normal internal stable condition. The other (5.2.5.1.2) is the state forced and held by asynchronous inputs. Para. 5.2.5.1.1 applies to any type of bistable circuit and must be specified. But 5.2.5.1.2 may or may not be applicable depending on the particular circuit. An example of application to a basic TTL circuit is given in Figure 5.2.5.1

Para. 5.2.5.2 is the V_{OH} maximum and here also is primarily intended for ECL type circuits. For this case all asynchronous inputs must be at their worst case levels to make the output "H" level in question a maximum, either holding or not holding the bistable in this state, whichever is worse. * See Figure 5.2.4.2 for application to a basic ECL circuit.

5.2.6 I_O

The purpose of this characteristic is to define the output current capability of the bistable when it is in the state in which, under normal conditions, it is not required to supply current. The intent is to define the type of circuit output, emitter follower, resistor pull-up, etc.

In 5.2.6.1 I_O is defined at $V_O \leq V_{IH \text{ MAX}}$ with the bistable in that state which would normally product a "L" output, or



5.2.6 I_O (continued)

asynchronous inputs at $V_{IL\ MIN}$ or $V_{IH\ MAX}$ to force the output to the "L" level. All other inputs and outputs are to be at their worst case values. In the case of ECL type bistable circuits, this characteristic would determine the minimum and/or maximum value of the output emitter follower resistor R_L shown in Fig. 5.2.4.2. This characteristic would not be applicable to RTL, DTL, or TTL type circuits.

For 5.2.6.2 I_O is defined at $V_O \leq V_{IL\ MAX}$ with the bistable in that state which would normally produce a "H" output, or asynchronous inputs at $V_{IL\ MIN}$ or $V_{IH\ MAX}$ to force the output to the "H" level. This is applicable to RTL and DTL type circuits would distinguish the type of circuit output, e.g., resistor pull up, emitter follower pull-in, etc. This characteristic would not be applicable for the ECL bistable, because this is covered in 5.2.5.1 where the $I_{OH\ MAX}$ is used. For other types of circuits this is referred to as short circuit current.

5.2.7 I_I

This characteristic defines all (asynchronous and synchronous and clock) input currents for both HIGH and LOW levels. A maximum must be specified and a minimum may be specified for each input.

Para. 5.2.7.1 defines I_{IL} for $V_I \leq V_{IL\ MAX}$ with worst case levels on all other inputs and worst case output loading. In some cases it may be necessary to force output levels with asynchronous inputs to obtain the worst case. Several examples of application to specific types of circuits are given in Figure 5.2.7.