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**METHODS OF MEASUREMENT FOR SEMICONDUCTOR**

**LOGIC GATING MICROCIRCUITS**

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METHODS OF MEASUREMENT FOR SEMICONDUCTOR  
LOGIC GATING MICROCIRCUITS

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## FOREWORD

The test methods and other material included herewith are recommended for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. These methods of measurement are equally applicable to monolithic, multichip, film or hybrid device construction, whether of silicon, germanium, or other semiconductor material, whether incorporating bipolar or MOS or both types of transistor technology.

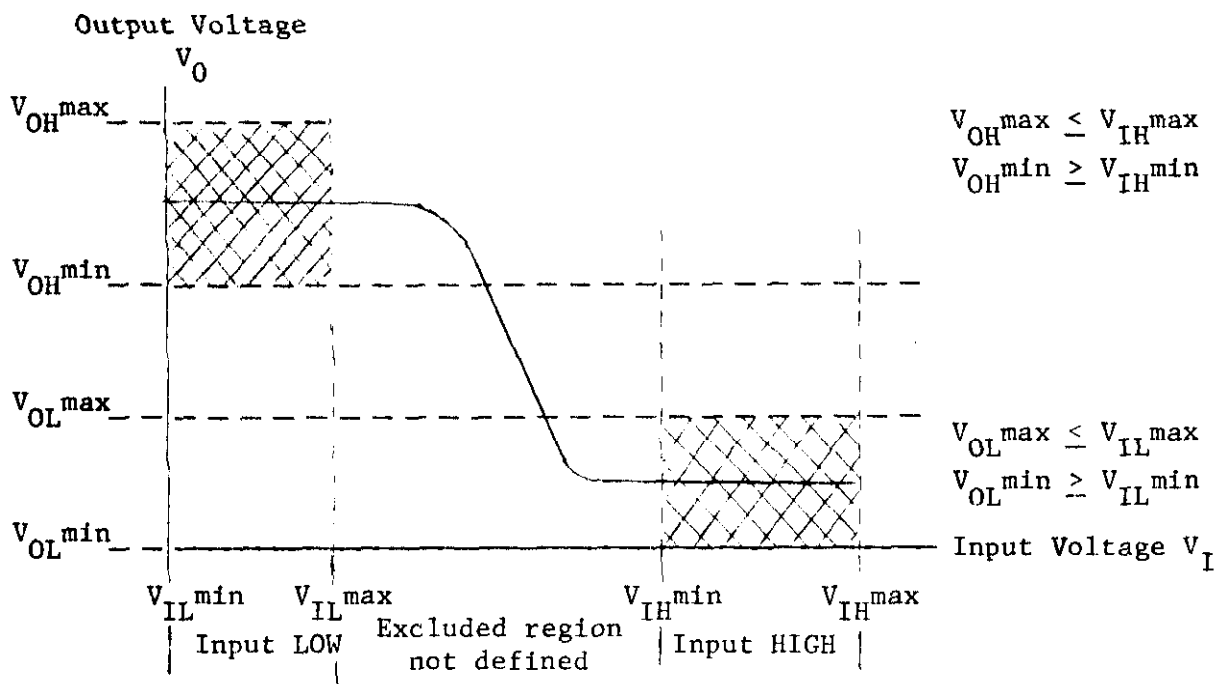
The purpose of this bulletin is twofold. It is to describe recommended tests and test methods, as noted above. It is also intended to assist and instruct those who complete and use the EIA Registration Data format for semiconductor logic gating microcircuits, MED-32-1C.

This document has been prepared by the MED-32 Committee on Active Digital Circuits and has been approved for publication by the EIA Microelectronics Engineering Panel.

## GENERAL BACKGROUND

For the circuit configurations of semiconductor logic gating microcircuits which use binary states to represent the digital information, a logical relationship exists between input and output. The logical conditions can be identified by the electrical parameters measured on the input and output to describe the binary states. Voltages or currents may be used to describe the states, but voltage is used most commonly.

The diagram of Figure 1 shows the state of the output of a gating circuit as a function of the input, using voltages to represent the states. There are certain limits that can be applied to each of the states to identify the acceptable operating regions for a particular design. Thus, on Figure 1, which is for an inverting logic gate, the output voltage must be within the cross-hatched areas for the defined voltages that appear at the input.  $V_{IHmin}$ ,  $V_{IILmax}$ ,  $V_{IHmax}$ , and  $V_{IILmin}$  are the boundaries of these regions. Since the logic gating circuits must couple to each other, the same values apply to input and output. The cross-hatched regions represent the regions of DC stability for the input and output voltages under worst case conditions for any logic gating circuit in a digital system made up of such gates.



OUTPUT VS INPUT VOLTAGE FOR AN INVERTING LOGIC GATING MICROCIRCUIT

Figure 1

$V_{IILmax}$  is the maximum allowed input LOW level in a logic system;  $V_{IHmin}$  is the minimum allowed input HIGH level in a logic system. For any  $V_I$  value less than  $V_{IILmax}$  or greater than  $V_{IHmin}$ , but less than  $V_{IHmax}$  the output voltage must be in the cross-hatched area.  $V_{IHmax}$  is chosen to be at least as large as the maximum HIGH state output can be. It will generally be the supply voltage unless the output has an active rather than a resistive pull-up.  $V_{IILmin}$  is chosen to be at least as small as a minimum LOW state output can be. It generally is zero and is shown so in Figure 1 and used so in the following test condition.

## MINIMUM DC CHARACTERISTICS FOR INTERCHANGEABILITY

In setting the registration format for semiconductor logic gating microcircuits, it was found that a universal set of "black-box" specifications could not be settled on without getting very cumbersome. Therefore, the format has been divided according to the type of circuit configuration of the logic gating circuit. A certain minimum amount of information is required to assure interchangeability. The format contains what is considered the minimum information necessary to describe a logic gate.

The inverting logic function is assumed in most of the format and in the commentary and curves which follow. Transposition of the worst-case conditions for non-inverting logic should be made as appropriate.

### DEFINITIONS

HIGH and LOW Levels The HIGH (H) level is that level which is the most positive of the two logic levels whereas the LOW (L) level is that level which is the most negative of the two logic levels.

Positive and Negative Logic Positive logic identifies the logic ONE with the HIGH level and logic ZERO with the LOW level. Negative logic identifies the logic ONE with the LOW level and the logic ZERO with the HIGH level.

Positive Current Conventional current flow into a microcircuit terminal is defined as positive.

Maximum Limit The highest-magnitude limit of a range of some quantity. For logic levels only, the most positive (least negative) limit.

Minimum Limit The lowest-magnitude limit of a range of some quantity. For logic levels only, the least positive (most negative) limit.

Logic Gating In the titles of this bulletin and the registration data format, the term "logic gating" is used. This is meant to cover all combinatorial logic functions and to exclude sequential logic functions. The latter, because they have memory, are covered by the bistable bulletin and registration data or some extension of it. Thus all interconnections of logic gates inside the registered microcircuit are within the applicability of this bulletin on logic gating microcircuits, provided that no inverting gates are cross-coupled (the output of gate A drives an inverting input of gate B and the output of gate B drives an inverting input of gate A) or the equivalent or obtain logic memory in any other manner.

For additional definitions, see also EIA format MED-32-1C, "Registration Data, Semiconductor Logic Gating Microcircuit," Appendix I.

Microelectronics Engineering Bulletin 1A, "Recommended Microelectronic Terms and Definitions."

## COMMENTARY ON THE REGISTRATION DATA FORMAT

Numbering herein is identical to that used in the MED-32-1C format for semiconductor logic gating microcircuits.

### 1.0 GENERAL DESCRIPTIONS

- 1.1 Type of Device specifies semiconductor material.
- 1.2 Type of Logic Function and Polarity describes the number of separate gates within the device and the logic function provided (NANA, AND, NOR, OR, COMBINATIONAL, etc.) and specifies whether positive or negative logic is meant.
- 1.3 Number of Inputs identifies all inputs to the device. This includes the number of inputs to each section of the device as well as expanding nodes for increasing fan-in or performing other logic functions externally.
- 1.4 Number and Type of Outputs describe the number and electrical type (open collector, emitter follower, etc.) of external outputs from each gate. It should be stated if logic can or should not be performed by connecting outputs together.

### 2.0 LOGIC DESCRIPTION The device must be completely described with a logic diagram, logic equations, and a truth table relating inputs to outputs.

- 2.1 The Logic Diagram represents the circuit function symbolically. Each terminal (inputs and outputs) must be identified with letters for reference to the logic equation and truth table. The preferred logic symbols are those defined in "Graphic Symbols for Logic Diagrams," IEEE Publication No. 91/ANS Y32.14.
- 2.2 The Logic Equation relates each output to the inputs. This equation must be consistent with the type and polarity of logic function described in Section 1.2 and the terminal identification in Section 2.1.
- 2.3 The Truth Table shows the relations between the HIGH (H) or LOW (L) logic levels of the inputs and outputs. The "HIGH/LOW" designation should be used in the truth table to avoid any confusion between positive or negative logic notation. Generally every column corresponds to the level of an input or output and every line corresponds to a combination of the input level and the resulting output level or levels. Whenever the level of an input has no influence it should be indicated by the symbol "X."

### 3.0 MECHANICAL DATA No commentary beyond notes incorporated in the registration data format is necessary.

### 4.0 MAXIMUM RATINGS A maximum rating is a limiting value of voltage, current or temperature which is to be exceeded only at the risk of permanently altering the characteristics of the microcircuit. A combination of maximum ratings cannot normally be permitted simultaneously.

#### 4.1 Temperature

4.1.1 Storage Temperature Range defines the range of environment in which a microcircuit may be stored with no electrical connections to the device.

4.1.2 Temperature Range under Bias defines the temperature range in which the microcircuit may be operated without risk of permanent change. The intent of this paragraph is to state the allowable maximum temperature in a system under some fault condition of cooling with supply voltages still applied. No guarantee of correct logic operation is intended. Both the temperature range and the bias conditions must be specified. Bias should represent that set of expected extreme continuous operating conditions of supply voltages, input drive, and output loading which result in worst-case power consumption. If the operating frequency has any significant effect on power consumption, a normal operating frequency shall be specified.

4.2 Terminal Voltage and/or Current Terminal Voltage and/or Current defines the maximum voltage and/or current that may be safely applied to each terminal of the microcircuit without risk of permanently altering any of its characteristics. Note that these ratings must be guaranteed over a specified temperature range and that this temperature range must include the temperature extremes specified for electrical characteristics under paragraph 5.1.2.2 but not necessarily those specified under paragraph 4.1.2. Each of these maximum values is defined independently of all others. For example, if a maximum power supply voltage is specified at 10 V and a maximum output current is specified to be 50 mA, the 10 V and 50 mA conditions cannot necessarily be applied simultaneously. In addition, if the maximum values specified apply only for certain conditions on other terminals, then these relevant conditions must also be specified. When maximum ratings are specified for both voltage and current at the same terminal, these maximum values are not defined independent of one another. For instance, if a maximum output voltage is specified at 8 V and a maximum current is specified to be 30mA for the same output, neither rating may be exceeded in attempting to apply the other.

#### 5.0 ELECTRICAL CHARACTERISTICS

5.1 Operating Conditions The notes in the registration data format are sufficient for use and understanding. No additional commentary is needed.

#### 5.2 Static Characteristics

A. For registration of static characteristics, three alternate sequences of tests are provided. These sequences relate to the three main circuit types in use:

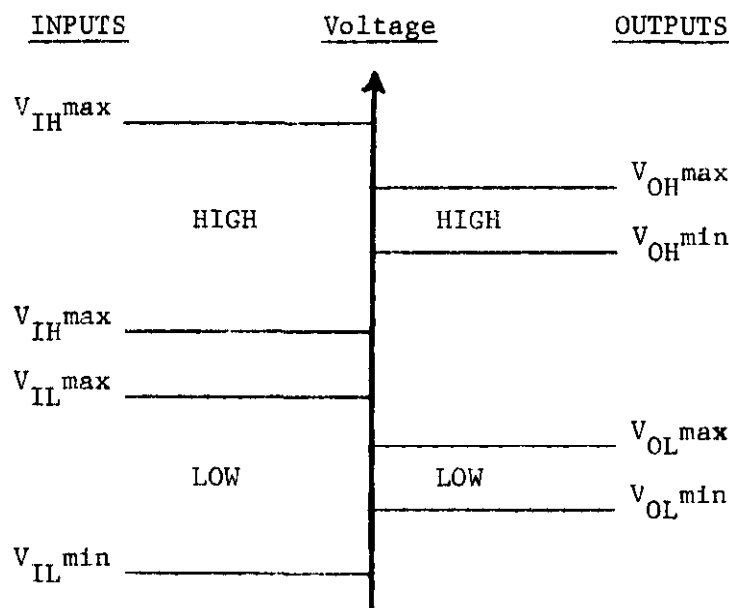
5.2.1 DCTL, RTL and RCTL

5.2.2 DTL and TTL

5.2.3 ECL

One of these sequences, where applicable to the type of circuit configuration used, should be chosen. For multiple duplicate gates, these tests apply for each gate. For more complex combinations of gates, these tests should serve as guiding rules in specifying the circuits. Conditions on all terminals must be specified for each test.

- B. The first two items in each sequence (5.2.X.1 and 5.2.X.2) are not tests. They are definitions of input logic voltage levels. This is the starting point for the registration of all electrical parameters. They are, by nature, definitions of the maximum and minimum LOW (L) and HIGH (H) voltage levels which will be accepted and recognized by the registered device. These do not appear as parameters in the format. The validity of the definitions is proven by using them as conditions and verifying that they do result in proper logical operation according to the truth tables of paragraph 2.2. They are used for both Static and Dynamic characteristics. Generally, the output levels of a logic gate are intended to be compatible with its input requirements. The logic gate output is intended to drive other logic gates like itself or other logic elements in the same family having compatible input requirements. Therefore, a relationship generally exists as depicted in Figure 2.
- C. In the descriptions and comments which follow, for each of the three sequences of tests, the same paragraph numbering is used as that given in the registration data format. Description of many of the tests is clarified by reference to Figures showing certain electrical characteristics. The test points are located by "X's" and are keyed to the text by circled numbers. The numbers are the least significant (right-most) part of the decimal number of the respective test.



Relationship between Input and Output HIGH and LOW Levels

FIGURE 2

5.2.1 Static Characteristics of DCTL-RTL Type Digital Circuitry This section will serve to illustrate the application of the logic gating format to an RTL type gate. This can best be illustrated with the aid of a transfer characteristic curve which is labeled with both the EIA standard terminology and the corresponding terminology most commonly employed in current RTL literature; see Figure 3.

With the aid of this curve the terms can be interpreted as follows:

5.2.1.1 A:  $V_{IL}^{min}$  - The minimum voltage that can be applied at the input of an RTL gate. In principle this may be zero volts. In practice, this would normally be output of a heavily saturated gate.

B:  $V_{IL}^{max}$  - The maximum low level voltage that can be applied to the input of an RTL gate and maintain that gate in the logical high state ( $V_{OH} \geq V_{OHmin}$ ). This is commonly referred to as  $V_{OFF}$  in RTL literature.

5.2.1.2 A:  $V_{IH}^{min}$  - The minimum high level voltage that can be applied to an RTL gate to guarantee that the gate output will maintain the logical low condition ( $V_{OL} \leq V_{OLmax}$ ). This is commonly referred to a  $V_{ON}$  in RTL literature. The purpose of this measurement is to establish the guaranteed value of  $I_{available}$  for fanout purposes. This current is normally specified at the  $V_{IH}$  required to drive the next gate load. In RTL circuitry, this measurement is more meaningful at that value of  $V_{IH}$  that guarantees "hard" saturation ( $V_{IN}$  in RTL literature).  $V_{IHmax}$  is only achieved at a fanout of one which defeats the purpose of the measurement.

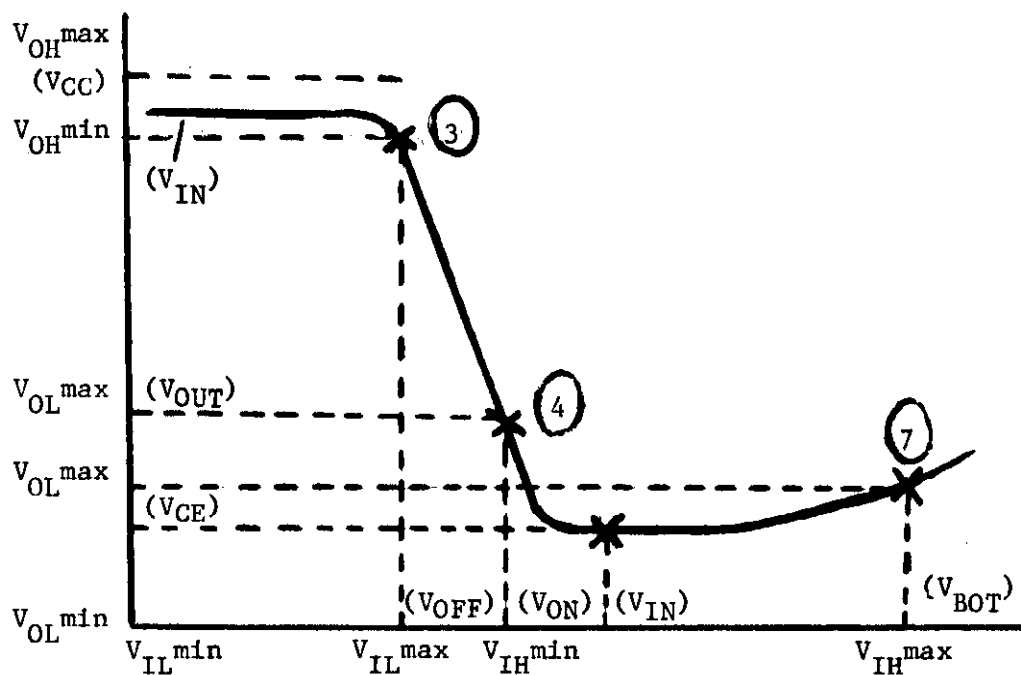
B:  $V_{IH}^{max}$  - The maximum high level voltage that will be applied to an RTL gate under normal operation. Commonly referred to as  $V_{BOT}$  in current RTL literature.

5.2.1.3  $V_{OH}^{min}$  - The minimum value of output voltage realizable with a known current, under conditions of maximum reverse bias current in the output gate transistor. In RTL literature, this is usually expressed in terms of the voltage for which a guaranteed  $I_0$  ( $I_{available}$ ) is obtainable.

5.2.1.4  $V_{OL}^{max}$  - The maximum value of output voltage realizable with the gate in the logical low condition, sinking a specified load current  $I_0$ , with a minimum high level drive  $V_{IHmin}$  ( $V_{ON}$ ) applied. Commonly referred to as  $V_{OUT}$  in RTL literature.  $I_0$  represents the  $I_{CER}$  reverse bias current of the driven gates.

5.2.1.5  $I_{IH}^{max}$  - The maximum input current which will flow when all other inputs are simultaneously biased high with at least the minimum high threshold voltage. This current is referred to as  $I_{IN}$  in the literature. At the other inputs, most RTL specifications use a voltage greater than  $V_{IHmin}$ ; normally  $V_{BOT}$ .

- 5.2.1.6  $I_{OH}^{max}$  - The maximum current that will flow with the worst-case input "off" voltage applied and an output voltage greater than  $V_{OHmin}$  at the gate output. The closest equivalent in most RTL literature is an  $I_L$  test which measures the current into the  $V_{CC}$  lead. The  $I_{OH}$  measurement is performed on some gate expander elements in the literature.
- 5.2.1.7 A:  $V_{OL}^{max}$  - The purpose of this test is to define the condition of "hard" saturation. The idea is to establish the the output voltage level under maximum input drive conditions to aid in determining the relative system noise margin available in the design.
- B:  $V_{OL}^{max}$  - The purpose is generally to ensure that the output voltage remains below  $V_{OL}^{max}$  even with all inputs simultaneously high at maximum  $V_{IH}$ . If appreciable emitter resistance were present, the test might be a worst case.
- 5.2.1.8  $I_{OH}^{max}$  - No comment, similar to test 5.2.1.3.
- 5.2.1.9  $I_{IH}^{max}$  - This measurement is equivalent to 5.2.1.5 except that it permits measuring directly the input current at a voltage greater than the input threshold voltage. Normally, in RTL this current is measured at  $V_{IN}$  and is referred to as  $I_{IN}$ . See the discussion on  $I_{IN}$  under paragraph 5.2.1.5.
- 5.2.1.10  $I_0^{max}$  - The test is designed to measure the total current drain from the  $V_{CC}$  supply with the input and outputs normally grounded. In RTL it is a direct measure of the output resistor.
- 5.2.1.11  $V_0^{max}$  - This measurement is intended exclusively for use with the gate extender type elements. Normally, the  $I_0$  current is matched to what would be expected if an internal output resistor were attached.



VOLTAGE TRANSFER CHARACTERISTIC FOR DCTL, RTL, AND RCTL (5.2.1)

Figure 3

### 5.2.2 Static Characteristics for DTL and TTL Type Logic Gating Circuitry

This section will serve to illustrate the application of the logic gating format to the registration of circuits such as DTL and TTL. Understanding of the definitions (5.2.2.1 and 5.2.2.2) and tests (5.2.2.3 ff) may be facilitated by reference to the electrical characteristic curves given in Figures 4, 5, 6, and 7. The test points are shown in these figures by "X's" and are keyed to the tests by circled numbers. These numbers are the least significant part of the decimal number of the respective tests.

5.2.2.1 A:  $V_{ILmin}$  - The minimum LOW level voltage applied to the gate input.

B:  $V_{ILmax}$  - The maximum LOW level voltage that can be applied at the gate input and still maintain the gate output at a logic HIGH level.

5.2.2.2 A:  $V_{IHmin}$  - The minimum HIGH level voltage that can be applied at the gate input and still maintain the gate output at a logic LOW level.

B:  $V_{IHmax}$  - The maximum HIGH level voltage applied to the gate input.

5.2.2.3  $V_{OLmax}$  - The maximum LOW level output voltage sinking a specified load current  $I_0$  while  $V_I = V_{IHmin}$  is applied to all inputs simultaneously.

5.2.2.4  $I_{ILmax}$  - The maximum LOW level input current flowing into the gate when  $V_I \leq V_{ILmax}$  is applied to each input sequentially, other inputs  $V_I = V_{IHmax}$ .

5.2.2.5 A:  $I_{IHmax}$  - The maximum current with  $V_I \geq V_{IHmin}$  applied sequentially to each input with other inputs at  $V_{ILmin}$  and measured at  $I_0 = 0$ .

B:  $I_{IHmax}$  - The maximum current with  $V_I \geq V_{IHmin}$  applied sequentially to each input with other inputs open or to  $V_{IHmin}$  and measured at  $I_0 = 0$ .

5.2.2.6 HIGH Level Output with  $V_I = V_{ILmax}$  applied to each input sequentially, other inputs to  $V_I \geq V_{IHmin}$ .

A:  $I_{OHmax}$  - This is a measure of the output high current into the output terminal, for outputs having no current source (pull-up).

B:  $V_{OHmin}$  - This is a measure of the minimum HIGH level output voltage when the output is sourcing a specified current.

5.2.2.7  $I_{Omax}$  and/or  $I_{Omin}$  - The output current available from the device. This represents the short circuit current flowing while the inputs have  $V_I = V_{ILmin}$  applied to them simultaneously.

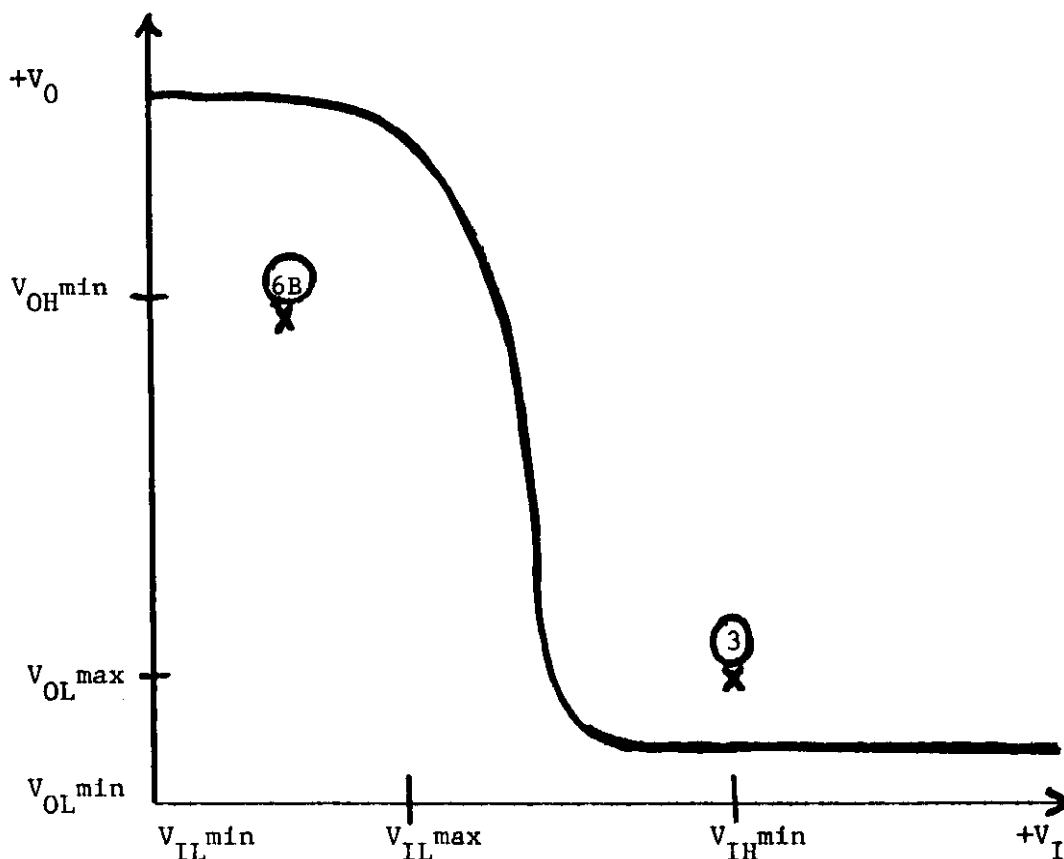
5.2.2.8  $I_{INL}^{max}$  - This is a measure of the maximum input current on the expander input node of an expandable DTL gate. This current is measured with the expander node held to a logic LOW level.

5.2.2.9 HIGH Level Output with  $V_{INL}$  applied to the expander node input, with other inputs open or to  $V_I \geq V_{IH}^{min}$ .

A:  $I_{OH}^{max}$  - This is a measure of the output HIGH current into the output terminal, for outputs having no current source (pull-up).

B:  $V_{OH}^{min}$  - This is a measure of the minimum HIGH level output voltage when the output is sourcing a specified current with the expander node held to a logic LOW level.

5.5.5.10  $I_R^{max}$  and/or  $I_R^{min}$  - This is a test to calculate the resistance of the output resistors when they are not internally connected to the output transistors. This current is measured with a voltage  $V_R \leq V_{IL}^{max}$  applied to the resistor terminals.



VOLTAGE TRANSFER CHARACTERISTIC FOR DTL AND TTL (5.2.2)

Figure 4