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FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

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FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

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Foreword

The document provides methodologies for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g., analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g., Cu/Low K interconnects or ultra-thin gate oxide.

Any qualification requirements beyond the minimum set are to be developed for the specific performance expected of the technology. The minimum set of measurements and the requirements for the qualification based on those measurements are to be determined between the foundry and its customers on an individual basis. The process technology owner (foundry) will be required to document the details of specific testing unique to the process being qualified.

The guideline documents attempts to reflect common best practices in the semiconductor industry and updated in accordance to advancement in the semiconductor industry and JEDEC bylaws of periodic reviews.

Introduction

This publication, entitled 'Foundry Process Qualification Guidelines', is co-sponsored by JEDEC and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification methodologies. The JEDEC sponsoring committee is JC-14 through its JC-14.2 subcommittee on wafer level reliability.

This document encompasses and references a number of other standards and procedures, some of which are in a state of constant revision and update. While a case might be made for producing a lean, concise guideline that does not spell out specific procedures or requirements, the proposition of spelling out the essence of a comprehensive set of methodologies in one place has a practical value that outweighs the case for simplicity. (comment : the requirements are only spelled out in a number of cases. Best to be consistent and let the existing JEDEC specs speak for themselves)

Acronyms

The following acronyms have been used in this document.

BTS:	bias temperature stress	MM:	machine model
CDM:	charged device model	NBTI:	negative bias temperature instability
EFR:	early failure rate	P2ID:	plasma-process induced damage
EM:	electromigration	PCM:	process control monitor
ESD:	electrostatic discharge	QBD:	Charge to breakdown
FA:	failure analysis	SM:	stress migration/voiding
FIT:	Failures in time	TC:	temperature cycling
GOI:	gate oxide integrity	TDDDB:	time-dependent dielectric breakdown
HAST:	highly-accelerated stress test	THB:	temperature-humidity bias
HBM:	human body model	TQV:	technology qualification vehicle
HCI:	hot carrier integrity	TVS:	triangular voltage sweep
HTOL:	high temperature operating life	VRDB:	voltage ramp dielectric breakdown
IMD:	inter/intra-metal dielectric	WLR:	wafer level reliability

FOUNDRIY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites)

(From JEDEC Board Ballot JCB-14-04, formulated under the co-sponsorship of the JC-14.2 Subcommittee on Wafer Level Reliability, and the Fabless Semiconductor Association's Committee on Standard Foundry Process Qualification (SFPQ))

1 Scope

This document describes test and data methods for the qualification of semiconductor technologies. It does not give pass or fail values or recommend specific test equipment, test structures or test algorithms. Wherever possible, it references applicable JEDEC, such as JESD47, or other widely accepted standards for requirements documentation.

There are two levels of qualification described. Level 1 is a pure process qualification intended to find reliability weaknesses. It primarily addresses technology wearout mechanisms through package or wafer level reliability tests on specially designed test structures.

Level 2 demonstrates the reliability of the process that corresponds to the reliability demands from projected or known applications. Level 2 testing can be implemented via the testing of a relevant functional technology qualification vehicle (TQV), including life test. The level 2 tests are described in clause 12. Other Reporting requirements (e.g., PCM data) are also included.

2 Quality system

It is the responsibility of the foundry to have the appropriate quality system in place with special emphasis on issues relating to equipment capability, maintenance and calibration, continuous improvement and process control. In particular, a functioning SPC methodology should be demonstrated for all key processes (see EIA/JEDEC EIA-557A). As a minimum the foundry will have ISO9001 certification. The ISO9001 audit results by a third party and subsequent corrective actions on deficiencies shall be made available to the customer upon request. For those supplying to automotive applications, the foundry may also have to demonstrate requirements from TS 16949 standard to meet the needs of these products

3 Responsibilities

3.1 Level 1 qualification

The foundry is responsible for the design and implementation of the level 1 test vehicle (i.e. TESTCHIP). For the special case of a foundry customer driving process development, development of the level 1 test vehicle may be shouldered in whole or in part by the customer. The foundry shall fabricate the qualification silicon, execute the described level 1 tests and create the qualification report. The tests and qualification report may be done by the foundry or third party test vendor. The qualification requirements may be reduced for a derivative process, where the parent process has already been fully qualified at the same location.

3.2 Level 2 qualification

In general, the foundry is responsible for the design and implementation of the Level 2 test vehicle (e.g., SRAM or pilot product). For the special case of a foundry customer driving process development, or where the customer requires TQV data before such a vehicle becomes available, development of the Level 2 test vehicle may be shouldered in whole or in part by the customer. The foundry, customer or third party test vendor may execute the Level 2 (TQV) tests and requisite failure analysis. The foundry will be responsible for suggesting and implementing corrective action based on the failure analysis results. The qualification report shall adhere to the minimum reporting requirements and format described in this document.

While it is expected that a particular foundry methodology may differ from the methods outlined in this document, the wafer foundry should demonstrate to the customer that it has satisfactorily addressed all issues of interest. The wafer foundry should therefore provide a documented procedure and supporting data that provide an assessment of potential failure and wearout mechanisms.

3.3 Reporting Requirements

Specific reporting requirements are included for the tests catalogued in this document. General reporting requirements include appropriate signoff, archiving and revision control, and the inclusion of supporting documents as appropriate.

The Level 1 qualification report shall include: (1) qualification plan, (2) description of the test vehicle including relevant test structure features and dimensions, (3) summary of test methods used, (4) pass/fail criteria, and (5) test results, analysis and model parameters as described in this document.

The Level 2 qualification report shall include: (1) qualification plan, (2) description of the technology qualification vehicle (TQV), (3) test description and specification, (4) pass/fail criteria (5) test results and analysis including failure rates, and (6) FA results.

4 Sample size

In general, data should come from 3 non-consecutive wafer lots, although the use of more lots is not precluded. A wafer lot is a group of wafers processed as a batch through the same or matched equipment in the same processing interval, using the same or matched conditions, materials, and methods. Typical sample sizes per lot are given in the individual test descriptions. Where applicable, confidence limits for each test population should be calculated. A conservative estimate of 40 die per wafer was made in determining sample size for tests that required the usage of all dies on the wafer.

5 Use of packages

Packages with a wire-bonded die that are capable of higher temperatures are generally used for testing of the technology qualification vehicle (TQV) or pilot product. A qualification report for the standard wire-bonding process should be included. Advanced packaging (e.g., BGA, flip-chip or chip-scale) may be substituted where applicable. This, in combination with TC and THB tests will demonstrate the assembly capability of this wafer fab process.

Side brazed ceramic packages are generally required for process wear-out tests performed at package-level at Temperatures greater than 155 °C. Consequently, wafer level testing is recommended wherever possible.

All references to temperature in the following sections imply junction temperature unless otherwise specified.

6 Reference documents

6.1 Industry standard documents

The following reference documents contain provisions that, through reference in this text, constitute provisions of this document. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based in this publication are encouraged to investigate the possibility of applying the most recent editions of the reference documents indicated. For undated references, the latest editions of the reference document referred to applies. Check the JEDEC website at <http://www.jedec.org>.

6.1.1 Reliability assessment methodology

JEDEC JEP70, *Quality and Reliability Standards and Publications*.

JEDEC JEP132, *Process Characterization Guidelines*.

JEDEC JEP143, *Solid State Reliability Assessment and Qualification Methodologies*.

JEDEC JEP122, *Failure Mechanisms and Models for Silicon Semiconductor Devices*.

JEDEC JESD91, *Method for Developing Acceleration Models for Electronic Component Failure Mechanisms*.

JEDEC JESD94, *Application Specific Qualification Using Knowledge Based Test Methodology*

JEDEC JESD659, *Failure-Mechanism-Driven Reliability Monitoring*.

JEDEC JEP131, *Process Failure Mode and Effects Analysis (FMEA)*.

6.1.2 Electromigration, stress migration, and IMD dielectric integrity

ASTM F1260M-96, *Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallization*.

JEDEC JESD33, *Standard Method for Measuring and Using the Temperature Coefficient of Resistance to Determine the Temperature of a Metallization Line*.

JEDEC JESD37, *Standard Lognormal Analysis of Uncensored Data and of Singly Right-censored Data Utilizing the Persson and Rootzen Method*.

JEDEC JESD61, *Isothermal Electromigration Test Procedure*.

JEDEC JESD63, *Standard Method for Calculating the Electromigration Model Parameters for Current Density and Temperature*.

JEDEC JESD87, *Standard Test Structures for Reliability Assessment of AlCu Metallization with Barrier Materials*.

JEDEC JEP139, *Guide for Isothermal Aging Method to Characterize Aluminum Interconnect Metallization for Stress-Induced Voiding*.

JEDEC JEP159, *Procedure for the Evaluation of Low-k/Metal Inter/Intra-Level Dielectric Integrity*

6.1.3 Hot carrier integrity

JEDEC JESD28, *A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress*. See also EIA/JEDEC JESD28-1, *N-channel MOSFET Hot Carrier Data Analysis (addendum on data analysis)*.

JEDEC JESD60, *A Procedure for Measuring P-Channel MOSFET Hot-Carrier-Induced Degradation under DC Stress*. See also JEDEC JESD60-1 (Addendum on data analysis).

6.1 Industry standard documents (cont'd)

6.1.4 Gate oxide integrity

JEDEC JESD35A, *Procedure for Wafer-Level-Testing of Thin Dielectrics*. See also addendum's JESD35-1 (test structures) and JESD35-2 (test criteria).

JESD92, *Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics*

6.1.5 Endurance tests

IPC/JEDEC J-STD-020, *Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices*.

JEDEC JESD22-A101, *Steady State Temperature Humidity Bias*.

JEDEC JESD22-A104, *Temperature Cycling*.

JEDEC JESD22-A108, *Temperature, Bias and Operating Life*.

JEDEC JESD22-A110, *Highly Accelerated Stress Test (HAST)*.

JEDEC JESD22-A113, *Preconditioning of Surface Mount Devices prior to Reliability Testing*.

JEDEC JESD47, *Stress-Test Driven Qualification of Integrated Circuits*.

JEDEC JESD50, *Special Requirements for Maverick Product Elimination*.

JEDEC JESD74, *Early Life Failure Rate Calculation Procedure for Electronic Components*.

JEDEC JESD85, *Methods for Calculating Failure Rates in Units of FITs*.

6.1.6 Electrostatic discharge tests

JESD22-A115, *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)*.

JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds for Microelectronic Components*.

ANSI ESD S5.1, *Electrostatic Discharge Sensitivity Testing – Human Body Model*.

ANSI ESD STM5.2, *Electrostatic Discharge Sensitivity Testing – Machine Model*.

ANSI ESD S5.3.1, *Charged Device Model (CDM) – Component Level*.

ANSI/ESDA/JEDEC JS-001-2012, *ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM)*

6.1.7 Latchup test

JEDEC JESD78, *IC Latch-Up Test*.

6.1.8 E-Test Parameters

ASTM F616-86, *Standard Test Method for Measuring MOSFET Drain Leakage Current*.

ASTM F617-86, *Standard Test Method for Measuring MOSFET Linear Threshold Voltage*.

ASTM F1096-87, *Standard Test Method for Measuring MOSFET Saturated Threshold Voltage*.

6.1.9 Quality standards

EIA-557, *Statistical Process Control Systems*.

EIA-670, *Quality System Assessment*.

ISO 9001:2000, *Quality Management Systems – Requirements*.

JESD671, *Component Quality Problem Analysis and Corrective Action Requirements (Including Administrative Quality Problems)*.

6 Reference documents (cont'd)

6.2 Selected references

Meeker, Q.A. and L.A. Escobar, *Statistical Methods for Reliability Data*, John Wiley, 1998.

Tobias, P.A. and D.C. Trindade, *Applied Reliability*, 2nd Ed., CRC Press, 1995.

Nelson, Wayne, "Accelerated Testing: Statistical Models, Test Plans, and Data Analyses", in *Wiley Series in Probability and Mathematical Statistics-Applied Probability*, John Wiley, 1990.

Amerasekera, E.A. and F.N. Najm, *Failure Mechanisms in Semiconductor Devices*, 2nd Ed., John Wiley, 1997.

Ohring, Milton, *Reliability and Failure of Electronic Materials and Devices*, Academic Press, 1998.

Yue, John, "Reliability", in C.Y. Chang and S.M. Sze (eds.), *ULSI Technology*, McGraw-Hill, 1996, Chapter 12.

Takeda, E. et al, *Hot-Carrier Effects in MOS Device*, Academic Press, 1995.

Amerasekera, E.A. and Charvaka Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley, 1996.

IRPS Conference Proceedings and Tutorials are an excellent source of information on current test methodologies and reliability models. (Web site www.irps.org)

Microelectronics Reliability, Pergamon Press. This journal publishes the proceedings of ESREF, the European equivalent of IRPS, along with frequent review papers.

Abadeer, W.W., IEEE Transactions on Device and Materials Reliability, Vol. 1, No. 1, March 2001, *Reliability Monitoring and Screening Issues With Ultrathin Gate Dielectric Devices*.

7 Qualification test summary table

Clause	Procedure	JEDEC Reference Standard(s)	Other Standards	Qual or Eng
8.1	Electromigration	JESD61, JESD87, JESD33A, JESD37, JESD63, JEP122G	ASTM: F1260-96 EIAJ-986	Q
8.2	Stress Migration (Stress-Induced Voiding)	JEP139, JESD87, JEP122		Q
8.3	Thermal Cycling (Copper Interconnect)	JESD22-A104		Q or E
8.4	Inter/Intra Metal-Dielectric Reliability	JEP159		Q
9.1	DC Hot Carrier Injection	JESD28, JESD60, JEP122	EIAJ-987	Q
10.1	Voltage Ramp Dielectric Breakdown (VRDB) / Charge to Breakdown (QBD)	JESD35		Q
10.2	Time-Dependent Dielectric Breakdown (TDDB)	JESD92, JEP122	EIAJ-988	Q
10.3	Plasma Process Induced Damage (P2ID)	None		Q or E
11.1	Ionic Contamination/ Bias Temperature Stress (BTS)	None		Q or E
11.2	Ionic Contamination/ Triangular Voltage Sweep (TVS)	None		Q or E
11.3	Negative Bias Temperature Instability (NBTI)	JEP122		Q
12.1	Long Term Life Test (HTOL)	JESD22-A108, JESD47, JESD74, JESD85		Q
12.2	Early Life Test	JESD22-A108, JESD47, JESD74, JESD85		Q
12.3	Temperature Cycling (TC)	JESD22-A113, JESD22-A104, JEP122		Q
12.4	Temperature Humidity Bias (THB) or Highly Accelerated Stress Test (HAST)	JESD22-A113, JESD22-A101, JESD22-A110		Q
12.5	Yield Data and Defect Density Calculation	None		Q
12.6	ESD Characterization	JESD22-A114, JESD22-A115, JESD22-C101	ANSI/ESD: STM5.1, STM5.2 and STM5.3	Q
12.7	Latchup Characterization	JESD78		Q
13.1	Process Control Monitor (PCM) Characterization	JEP132	ASTM: F616-86, F617-86 and F1096-87	Q
14.1	Construction Analysis	None		Q

8 BEOL Interconnect Reliability

8.1 Electromigration

Electromigration testing should be done on each unique via level and metal layer (i.e., having any differences in design rules or process parameters from the rest of the metal stack, including the metal and inter-/intra- level dielectric processes. For instance, if metal layers and vias 2-4 have the same design rules and undergo similar processing, testing of metal 2 and connecting vias (lowest similar metal level) will suffice. The worst-case stacked via structure (if known), or each permutation of stacked vias, should be tested separately. Via tests should exercise electron flow both up and down through the via, thus stressing both via-to-metal interfaces.

The method described in this section may have limitations when applied to newer technologies (e.g., Cu/Low K). In such instances, the applicability of the method should be evaluated on a case-by-case basis.

8.1.1 Electromigration test requirements

Reference procedure	ASTM F1260-96, JESD33-A, JESD37, JESD63, and JESD87,
Test structures	Test structures for Al metallization are recommended to be designed for each combination of line and via/contact, per JEDEC JESD87, <i>Standard Test Structures For Reliability Assessment of AlCu Metallization With Barrier Materials</i> . Test structures for Cu can be designed according to JESD87. Structures should be included that allow measuring the influence of current flow direction and reservoir and back-stress effects. However, for Cu metallization with no barrier layer on the top surface, additional structures should be included that have a line width sufficiently larger than the width of the via (e.g., 2-5X) above to prevent contact between the via above and the liner of the test line.
Vehicle	Test structures may be stressed at package or wafer level. For package level tests, ceramic packages should be used.
Sample size and stress conditions	a) In a standard process qualification, samples from at least 2 lots with 2 wafers per lot should be tested for every structure referenced under "Test Structures" above. At least a third lot should be tested if substantial variations are observed between the first two lots. b) Samples from 1 lot are to be used for determination of Black's equation parameters. A minimum of three current densities ($J_1 < J_2 < J_3$) and three temperatures ($T_1 < T_2 < T_3$) are recommended. Current density and temperature values should be within the limits outlined under "Test Method" below. - To determine the activation energy, stress a minimum of three groups at J_2/T_1, J_2/T_2, and J_2/T_3. - To determine the current density exponent, stress a minimum of two additional groups at J_1/T_2 and J_3/T_2, using the J_2/T_2 group from the temperature stresses to complete the current group. c) Sample Size Considerations i) A minimum starting sample size of 15 per experiment (for each test structure for each unique set of test conditions) is required to provide accurate estimation of t_{50} and σ, and a minimum sample size of 20 is recommended. ii) A minimum of 12 valid time-to-fail data points is required (for each test structure for each unique set of test conditions) for determination of t_{50} and σ. If there are less than 12 valid time-to-fail data points for an individual experiment, that experiment must be repeated. iii) No more than 50% of the sample data can be censored, i.e. at least 50% of the samples must be taken to failure. iv) In a multi-cell test, the 50% failure requirement may be waived for the cell with the lowest acceleration, provided the data for all cells can be fit with a common sigma.

8.1 Electromigration (cont'd)

8.2.1 Electromigration test requirements (cont'd)

Test parameters and Failure Criteria	a) Test parameters include stress temperature (T_s), stress current density (J_s) and percent resistance change when the sample fails. Percent resistance change is defined as: $[(R_{\text{INITIAL}} - R_{\text{FINAL}})/R_{\text{INITIAL}}] \times 100$, where R_{INITIAL} is the initial resistance and R_{FINAL} is the final resistance measured at the stress temperature. b) Failure criteria: either a percent resistance change or a leakage limit to an extrusion monitor. The appropriate failure limit (e.g., 2%, 5%, 10% or 20% resistance change, or Amps of leakage current) will depend on the functionality specification for the technology.
Test Method	a) After determining the temperature coefficient of resistance (TCR) and measuring R_{INITIAL}, parts should be subjected to constant-current stressing at 150 °C – 300 °C for Al, and at 250 °C – 400 °C for Cu, in conventional ovens and at current densities ranging from the target J_{MAX} up to five times J_{MAX}, until sufficient parts have failed (see c) and d) in “Sample size and stress conditions” above). R_{FINAL} and the failure time must be recorded for each part that fails. Test structure temperature must be determined from the TCR according to JESD33, and the corrected temperature (oven ambient plus Joule heating) should be used for calculations in b) below. Performing the test at higher temperatures may be suitable in certain cases (e.g., for Cu metallization with a metal cap). b) The test plan should allow for extraction of the activation energy (E_a) and the current density exponent (n) for the Black’s equation model, consistent with JESD63. c) Consistent with ASTM F1260-96, the resistance increase of the test structure and leakage to the extrusion monitor shall be measured within periods that are much shorter than the anticipated duration of the test. Each experiment in the test plan should be continued at least until the number of failures reaches the larger of the following conditions: 1) at least 50% of the samples have failed, or 2) at least 12 samples have failed when the experiment sample size is ≤ 24. d) Failure analysis of representative failure samples is recommended. (If No Failure analysis is performed, data analysis based on % cumulative failure may be misleading when different fail mechanisms are present)
Cautionary Note	The methodology outlined above allows for the derivation of an EM model for the metallization being tested. If the suggested sample requirements and/or the minimum number of allowed failures cannot be produced within a reasonable time, it may not be possible to derive such a model. However, it may be possible to establish a lower bound on lifetime for a given set of stated conditions, and demonstrate that qualification goals are met.
Model to be used	a) The models are described in JEP122G 1. For Al interconnects, see 5.9 2. For Cu interconnects, see 5.10

8.1 Electromigration (cont'd)

8.3.1 Electromigration test requirements (cont'd)

Merit data	Calculate either 1) or 2) using the parameters in the table. 1) Lifetime for a 0.1% fraction failure per structure at the intended maximum current density and intended maximum operating temperature for the technology, using the following formula. $\tau(0.001) = t_{50\text{stress}} \cdot \left(\frac{J_{\text{stress}}}{J_{\text{use}}} \right)^n \exp \left[-3.09\sigma + \frac{E_a}{k} \left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}} \right) \right]$ 2) Maximum current density (J_{MAX} 0.1%) for a per-structure failure fraction of 0.1%, at the intended maximum operating junction temperature and the maximum intended lifetime using the following formula. $J_{\text{MAX}}(0.001) = J_{\text{stress}} \cdot \left\{ \frac{t_{50\text{stress}} \cdot \exp \left(-3.09\sigma + \frac{E_a}{k} \left(\frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}} \right) \right)}{\tau} \right\}^{\left(\frac{1}{n} \right)}$ <table><tr><th>Parameter</th><th>Description</th><th>Units</th></tr><tr><td>T_{use}</td><td>Maximum operating junction temperature plus applicable Joule heating</td><td>°K</td></tr><tr><td>τ</td><td>Maximum power-on lifetime</td><td>hr</td></tr><tr><td>J_{stress}</td><td>Current density during stress</td><td>mA/μm²</td></tr><tr><td>T_{stress}</td><td>Temperature during stress, including Joule heating</td><td>°K</td></tr><tr><td>σ</td><td>Lognormal sigma of the failure distribution</td><td></td></tr><tr><td>$t_{50\text{stress}}$</td><td>Lognormal median time to failure from the failure data</td><td>hr</td></tr><tr><td>E_A</td><td>Activation energy from failure data, as indicated above</td><td>eV</td></tr><tr><td>n</td><td>Current density exponent from failure data</td><td></td></tr><tr><td>k</td><td>Boltzmann Constant = 8.6174 x 10⁻⁵</td><td>eV/°K</td></tr></table> NOTE In formula (1) and (2), the coefficient of σ, -3.09, is the random variable in the Standard Normal Distribution corresponding to 0.1% cumulative fraction (summed from the left side) of the population of each structure being tested. It is only one example to show how to perform these calculations. In reality, chip level failure rate related to EM is a statistical sum of all different structures and their instances in a chip. Therefore, other coefficient values may be considered for specific application requirements and design constraints, and can be chosen case by case or per customer and supplier arrangements. The calculated lifetime, maximum use current density, and chip level failure rate related to EM will be different for other coefficient values.	Parameter	Description	Units	T_{use}	Maximum operating junction temperature plus applicable Joule heating	°K	τ	Maximum power-on lifetime	hr	J_{stress}	Current density during stress	mA/μm ²	T_{stress}	Temperature during stress, including Joule heating	°K	σ	Lognormal sigma of the failure distribution		$t_{50\text{stress}}$	Lognormal median time to failure from the failure data	hr	E_A	Activation energy from failure data, as indicated above	eV	n	Current density exponent from failure data		k	Boltzmann Constant = 8.6174 x 10 ⁻⁵	eV/°K
Parameter	Description	Units																													
T_{use}	Maximum operating junction temperature plus applicable Joule heating	°K																													
τ	Maximum power-on lifetime	hr																													
J_{stress}	Current density during stress	mA/μm ²																													
T_{stress}	Temperature during stress, including Joule heating	°K																													
σ	Lognormal sigma of the failure distribution																														
$t_{50\text{stress}}$	Lognormal median time to failure from the failure data	hr																													
E_A	Activation energy from failure data, as indicated above	eV																													
n	Current density exponent from failure data																														
k	Boltzmann Constant = 8.6174 x 10 ⁻⁵	eV/°K																													
Other data required	a) Line width, thickness, sheet resistance and composition of metal lines, via dimensions and measurements of alignment of via/contact layers to their respective metal layers. b) In the event that failure distributions are bi-modal, or if early failures occur, failure analysis should be provided to compare the failures of the different distributions.																														