JEDEC STANDARD

Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits

JESD100B.01

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS

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Foreword

The purpose of this standard is to promote the uniform use of symbols, abbreviations, terms, and definitions throughout the semiconductor industry.

Where applicable, reference is made to publications of the following organizations:

International Electrotechnical Commission (IEC)
American National Standards Institute, Inc. (ANSI)
Institute of Electrical and Electronics Engineers (IEEE)

The material contained in this standard was formulated under the cognizance of JEDEC JC-10 Committee on Terms, Definitions, and Symbols and approved by the JEDEC Solid State Technology Association Board of Directors.

The text of this standard is based on JESD100-A, which it replaces, and the following JEDEC Board ballots: JCB-94-48, JCB-96-19, JCB-96-67, JCB-97-74, JCB-98-90, JCB-99-06, JCB-99-45, and JCB-99-49. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

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TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS

1 General terms and definitions

accumulator: A register in which one operand of an operation can be stored and subsequently replaced by the result of another operation. (Ref. IEC 824.)

address: (1) A character or group of characters that identifies a register, a particular part of storage, or some other data source or destination. (Ref. ANSI X3.172.)

(2) To refer to a device or a data item by its address. (Ref. ANSI X3.172.)

address register: A register that is used to hold an address. (Ref. IEC 824.)

arithmetic and logic unit (ALU): The part of a processor that performs arithmetic operations and logic operations. (Ref. IEC 824.)

arithmetic unit: The part of a processor that performs arithmetic operations. (Ref. IEC 824.)

NOTE This term is sometimes used for a unit that performs both arithmetic and logic operations.

associative memory: Synonym for "content-addressable memory". (Ref. IEC 748-2.)

baud: A unit of signaling speed equal to the number of discrete conditions or signal events per second. (Ref. ANSI X3.172.)

NOTE For example, one baud equals one bit per second in a train of binary signals or one 3-bit value per second in a train of signals each of which can assume one of eight (2^3) different states.

bit (b): (1) In the binary numeration system, either of the digits 0 or 1. (Ref. ANSI X3.172.)

NOTE Abbreviated form of "binary digit".

(2) The unit of storage capacity that corresponds to a single memory cell.

(bit) slice: A partition of a microprocessor that enables several identical units to be paralleled or cascaded and augmented by control logic to realize the central processing unit.

bit-slice processor: A central processing unit constructed of an array of identical units, each of which operates simultaneously upon one or more adjacent bits. (Ref. IEC 824.)

bit-wide device: A device that has only a single-bit data interface.

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1 General terms and definitions (cont'd)

block: A continuous range of memory addresses. (Ref. IEC 748-2.)

NOTE The number of addresses included in the range is frequently equal to 2^n, where n is the number of bits in the address.

buffer: (1) A routine or storage used to compensate for a difference in the rate of flow of data or in the time of occurrence of events, when transferring data from one device to another. (Ref. ANSI X3.172.)

(2) An isolating circuit used to minimize the effects of a driven circuit on the driving circuit. (Adapted from ANSI/IEEE Std 100 and ANSI X3.172.)

buffer storage: Storage used to compensate for a difference in the rate of flow of data between components of an automatic data processing or communications system, or in the time of occurrence of events in the components. (Adapted from ANSI X3.172.)

bus: A common path along which power or signals travel from one or several sources to one or several destinations. (Adapted from IEC 824.)

busy signal: Synonym for "wait signal"

byte (B): (1) A binary character string operated upon as a unit and usually shorter than a computer word. (Ref. ANSI X3.172.)

NOTE A byte is usually eight bits.

(2) The unit of storage capacity equal to eight bits.

byte-wide device: A device that has a parallel data interface of eight bits, possibly with additional bits appended to provide parity or error-detection capability.

cache memory: A special buffer storage, smaller and faster than main storage, that is used to hold a copy of data or instructions that have been obtained automatically from main storage and are likely to be needed soon by the processor. (Adapted from ANSI X3.172.)

NOTE It is placed between the CPU and main storage to make main storage look like fast memory.

CAS latency (for an SDRAM): Synonym for "read latency".

(central) processing unit (CPU): A functional unit that consists of one or more processors and their internal storage. (Ref. ANSI X3.172.)

chip-enable input: A control input that, when active, permits operation of the integrated circuit and, when inactive, causes the integrated circuit to be in a reduced-power standby mode. (Ref. IEC 748-2.)

NOTE A chip-enable input is a clock or strobe input that significantly affects the power dissipation of the integrated circuit. For example, it may be the cycle control input of a dynamic memory or a power-reduction input of a static memory.

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1 General terms and definitions (cont'd)

chip-select input: A control input that, when active, permits operation of the integrated circuit and, when inactive, prevents input or output of data to or from the integrated circuit. (Ref. IEC 748-2.)

clear: To preset a storage or memory device to a prescribed state, usually that denoting zero. (Ref. IEEE Std 100.)

NOTE In the field of nonvolatile memories, clear conventionally means to set the outputs of the memory to the high logic level.

clear algorithm (for a flash EEPROM): The timed sequence of signals necessary to clear the memory.

clear disturb: The corruption of data in one location caused by the clearing of data at another location.

clock cycle: The time period, generally derived from an oscillator, that is used for sequencing data flow and synchronizing one or more functions. (Ref. IEC 824.)

complex-instruction-set computer (CISC): A microcomputer or microprocessor that performs multiple tasks per complex instruction, usually requiring multiple clock cycles.

content-addressable memory (CAM): A memory that responds with all the data in a storage zone if a portion of that data matches the data used for addressing the memory. (Ref. IEC 748-2.)

control bus: A bus carrying the signals that regulate system operations. (Ref. ANSI X3.172.)

coprocessor: A processing unit that extends the capabilities of its main processor, directly accesses the memory of that processor, and does not operate autonomously. (Ref. IEC 824.)

cycle: (1) A sequence of operations in which one set of events is completed.

(2) Any set of operations that is repeated regularly in the same sequence.

NOTE The operations may be subject to variations on each repetition. (Ref. ANSI X3.172.)

data bar polling: A method, used to determine whether the write operation in a memory is complete, wherein the memory is put into the read mode after initiating the write mode; if writing is complete, the outputs take on the addressed stored data, or if writing is not complete, the specified output(s) take on the complement of the last bit(s) written.

NOTE If writing is not complete: (a) in older devices, normally all outputs take on the complement of the last bits written; (b) in more modern byte-wide memories, only the most significant output takes on the complement of the last bit written; (c) in word-wide memories, the most significant output of the least significant byte, the most significant output of the entire word, or both of these outputs take on the complement of the last bit written.

data bus: A bus used to communicate data internally and externally to and from processing units, storage devices, or peripheral devices. (Adapted from ANSI X3.172.)

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1 General terms and definitions (cont'd)

data change: An event in which at least one bit of data is caused to change.

NOTE This event may be used as a unit of endurance for erasable programmable read-only memories.

data cycle: A cycle in which each bit changes to its opposite state and back to its original state.

NOTE 1 These changes may occur for all bits in parallel or in series, e.g., by page, block, word, byte, or bit.

NOTE 2 This cycle may be used as a unit of endurance for erasable programmable read-only memories.

data-retention mode: A standby or battery mode of operation in which the integrity of stored data is maintained although the supply voltage is below that specified for reading or writing.

data-retention time: Synonym for "retention time".

data rewrite: An operation including one data cycle or at least one data change, in which data is written into an array.

double word: A character string or binary element string that, in a given system, has twice the length of a word.

duplex transmission: Data transmission in both directions simultaneously. (Ref. ANSI X3.172.)

dynamic random-access memory (DRAM): A dynamic memory that permits access to any of its address locations in any desired sequence with similar access time to each location.

dynamic (read/write) memory: A volatile read/write memory in which the cells require the repetitive application of control signals generated inside or outside the integrated circuit to retain stored data. (Adapted from IEC 748-2.)

NOTE 1 The words "read/write" may be omitted from the term when no misunderstanding is likely.

NOTE 2 Each repetitive application of the control signals is normally called a refresh operation or cycle.

NOTE 3 A dynamic memory can use static addressing or sensing circuits.

NOTE 4 Contrast with "static (read/write) memory".

EEPROM redundancy: See "redundancy (in a memory)".

electrically erasable programmable read-only memory (EEPROM): A reprogrammable read-only memory in which the cells at each address can be erased electrically and reprogrammed electrically.

endurance (of a reprogrammable read-only memory): The ability of a reprogrammable read-only memory to withstand data rewrites and still comply with its specifications.

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1 General terms and definitions (cont'd)

erasable programmable read-only memory (EPROM): A reprogrammable read-only memory in which all cells can be simultaneously erased using ultraviolet light, after which the cells at each address can be reprogrammed electrically.

erase: To remove information from a memory. (Ref. IEC 748-2.)

NOTE In the field of electrically erasable programmable read-only memories, "erase" conventionally means the removal of electrons from the floating gate of the memory cell.

erase algorithm (for a flash EEPROM): The timed sequence of signals necessary to erase the memory.

erase disturb: The corruption of data in one location caused by the erasing of data at another location.

erase-program cycle: The event of writing a memory cell from the erased state to the programmed state and back to the erased state.

NOTE This event may be used as a unit of measurement for endurance. Within a sequence, erase-program cycles are indistinguishable from program-erase cycles.

execution time (for an instruction): The time, normally expressed in clock cycles, required to carry out an instruction.

false-write protection: Synonym for "inadvertent-write protection".

field-programmable read-only memory: A read-only memory that, after being manufactured, can have the data content of each memory cell altered. (Ref. IEC 748-2.)

firmware: The program instructions stored in a read-only memory.

NOTE Computer programs stored on disks, including hard drives and CD-ROMs, are customarily referred to as software.

first-in, first-out (FIFO) memory: A memory from which data can be read only in the same order as entered, although not necessarily at the same rate.

fixed-program read-only memory: A read-only memory in which the data content of each cell is determined during manufacture and is thereafter unalterable. (Ref. IEC 748-2.)

flag bit: An information bit that indicates the occurrence of special conditions such as overflow, carry, or interrupt.

flash EEPROM (FEEPROM): An EEPROM in which clearing can be performed only on blocks or on the entire array.

NOTE There are no restrictions on the block architecture in the definition of FEEPROM. The blocks within a device may be of various capacities ranging from a single address to the entire memory array.

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1 General terms and definitions (cont'd)

full-duplex transmission: Synonym for "duplex transmission".

general-purpose register: A register, usually explicitly addressable, within a set of registers, that can be used for different applications, such as an accumulator, an index register, or a special handler of data. (Ref. IEC 824.)

giga (G) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1 073 741 824 (2^{30} or K^3, where K = 1024).

NOTE 1 Contrast with the SI prefix giga (G) equal to 10^9, as in a 1-Gb/s data transfer rate, which is equal to 1 000 000 000 bits per second.

NOTE 2 See note 2 to "mega (M)".

half-duplex transmission: Data transmission in either direction, one direction at a time. (Ref. ANSI X3.172.)

hardware: Physical equipment, as opposed to programs, procedures, rules, and associated documentation. (Ref. ANSI X3.172.)

NOTE Contrast with "software".

high-speed carry: In parallel addition, any procedure for speeding up the processing of carries. (Ref. IEC 824.)

EXAMPLE Standing-on-nines carry.

hold (input) signal: A signal that causes a central processing unit to stop its activity and to relinquish control over the bus until the signal is removed. (Ref. IEC 824.)

inadvertent-write protection: The circuitry used to prevent writing from occurring when the control signals of the memory enter an indeterminate state during power on, power off, or noise transients.

instruction register: A register that is used to hold an instruction for interpretation. (Ref. IEC 824.)

instruction set (of a microprocessor): All the instructions that can be executed by a given microprocessor.

interrupt; interruption: A suspension of a process, such as the execution of a computer program, caused by an event external to that process and performed in such a way that the process can be resumed. (Ref. IEC 824.)

interrupt mask: A central processing unit (CPU) feature that allows the computer to ignore (mask) an interrupt request until the mask bit is disabled.

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1 General terms and definitions (cont'd)

interrupt request: An external signal that requests a temporary suspension of the normal program operation in order to permit processing of a higher-priority operation.

NOTE Multiple interrupt capability requires establishment of an interrupt-priority system.

kilo (K) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1024 (2^{10}).

NOTE 1 Contrast with the SI prefix kilo (k) equal to 10^3, as in a 1-kb/s data transfer rate, which is equal to 1000 bits per second.

NOTE 2 See note 2 to "mega (M)".

last-in, first-out (LIFO) memory: Synonym for "pushdown storage".

logic unit: The part of a processor that performs logic operations. (Ref. IEC 824.)

look-ahead carry: A high-speed carry procedure in which a group of carry digits is formed in parallel from the respective input bits of the two groups that are to be added and, if it exists, from the most significant carry digit that immediately precedes those groups. (Ref. IEC 824.)

machine cycle: The sequence of operations that corresponds to one memory cycle, input/output (I/O) cycle, or equivalent internal operation in a central processing unit (CPU). (Ref. IEC 824.)

NOTE An instruction may require one or more machine cycles for its execution. A machine cycle usually contains more than one clock cycle.

main storage: The part of internal storage into which instructions and other data must be loaded for subsequent execution or processing. (Ref. ANSI X3.172.)

mask-programmed read-only memory: A fixed-program read-only memory in which the data content of each cell is determined during manufacture by the use of a mask. (Ref. IEC 748-2.)

mass storage: Nonvolatile auxiliary storage of large capacity used for storage of data to which infrequent reference need be made.

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1 General terms and definitions (cont'd)

mega (M) (as a prefix to units of semiconductor storage capacity): A multiplier equal to 1 048 576 (2^{20} or K^2, where K = 1024).

NOTE 1 Contrast with the SI prefix mega (M) equal to 10^6, as in a 1-Mb/s data transfer rate, which is equal to 1 000 000 bits per second.

NOTE 2 The definitions of kilo, giga, and mega based on powers of two are included only to reflect common usage. IEEE/ASTM SI 10-1997 states "This practice frequently leads to confusion and is deprecated." Further confusion results from the popular use of a "megabyte" consisting of 1 024 000 bytes to define the capacity of the familiar "1.44-MB" diskette. An alternative system is found in Amendment 2 to IEC 60027-2: *Letter symbols to be used in electrical technology – Part 2:*

Prefixes for binary multipliers

Factor	Name	Symbol	Origin	Derivation
2^{10}	kibi	Ki	kilo + binary: $(2^{10})^1 = 1\ 024$	kilo: $(10^3)^1$
2^{20}	mebi	Mi	mega + binary: $(2^{10})^2 = 1\ 048\ 576$	mega: $(10^3)^2$
2^{30}	gibi	Gi	giga + binary: $(2^{10})^3 = 1\ 073\ 741\ 824$	giga: $(10^3)^3$
2^{40}	tebi	Ti	tera + binary: $(2^{10})^4 = 1\ 099\ 511\ 627\ 776$	tera: $(10^3)^4$

IEC suggests that, in English, the first syllable of the name of the binary-multiplier prefix should be pronounced in the same way as the first syllable of the name of the corresponding SI prefix and that the second syllable should be pronounced as "bee".

memory cell: The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved. (Ref. IEC 748-2.)

memory integrated circuit: An integrated circuit consisting of memory cells and usually including associated circuits such as those for signal amplification and address selection. (Ref. IEC 748-2.)

memory location: A subdivision of a memory, including one or several memory cells, that is the smallest part of the memory that can be addressed.

NOTE The content of a memory location is usually called a bit, a byte, or a word, as appropriate.

memory organization: The arrangement of memory cells, either by geometrical arrangement in rows and columns or by organization of the data to be stored. (Ref. IEEE Std 641.)

microcomputer (µC): A computer system whose central processing unit (CPU) is a microprocessor.

NOTE A basic microcomputer includes a microprocessor, memory, and input/output ports; these may or may not be on the same chip. See also "microcontroller".

microcontroller (MCU): A microcomputer on a single chip.

NOTE A microcontroller is generally dedicated to a single task defined by a fixed program in internal ROM.

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1 General terms and definitions (cont'd)

microprocessing unit (MPU): The name sometimes used for the central processing unit (CPU) of a microcomputer.

microprocessor (integrated circuit) (µP): An integrated circuit capable of all of the following:

a) operating on coded instructions;

b) carrying out, in accordance with the instructions:

1) the acceptance of coded data for processing and/or storage,
2) arithmetic and logical operations on the input data together with any relevant data stored in the internal registers of the microprocessor integrated circuit and/or in external memories, and
3) the delivery of coded data; and

c) accepting and/or delivering signals controlling and/or describing the operation or state of the microprocessor integrated circuit. (Ref. IEC 748-2.)

NOTE The instructions may be fed in, built in, or held in an internal memory.

microprogrammable computer: A computer in which the microprogram (microinstructions) in the read-only memory (ROM) used for instruction decoding can be changed, thus changing the computer's instruction set.

nibble: A binary character string operated upon as a unit and shorter than a byte.

NOTE A nibble is usually four bits.

nibble-wide device: A device that has a parallel four-bit data interface.

nonvolatile memory: A memory in which the data content is retained when power is no longer supplied to it.

NOVRAM: Acronym for "nonvolatile random-access memory". See also "NVRAM".

NVRAM: Abbreviation for "nonvolatile random-access memory". See also "NOVRAM".

output enable: A control input to an integrated circuit that, depending on the logic level applied to it, either permits or prevents the output of data from the device.

NOTE When disabled, the outputs assume a low level, a high level, or a floating (high-impedance) state, depending on the design of the particular circuit.

page: (1) In virtual memory, a fixed-length block that is transferred as a unit between main storage and auxiliary storage. (Adapted from ANSI X3.172.)

(2) A segment of a memory addressed by a subset of its full address field, usually with speed and/or power benefits relative to access by the full address.

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1 General terms and definitions (cont'd)

page mode: An operating mode in which all accesses to a memory occur within a defined page boundary.

NOTE For example, for a dynamic random-access memory, the page may be defined by the row address with the column addresses entered on the active transitions of the column address strobe. See also "static-column page mode".

parallel operation: A processing mode in which operations are performed concurrently in one or more devices. (Ref. ANSI X3.172.)

NOTE Contrast with serial operation.

parallel transmission: The simultaneous transmission on separate channels or bus lines of all the bits necessary to complete a clock cycle.

peripheral equipment: In a data processing system, any equipment, distinct from the central processing unit, that may provide the system with outside communication or additional facilities. (Ref. ANSI X3.172.)

processing unit: Synonym for "central processing unit".

processor: In a computer, a functional unit, consisting of at least an instruction control unit and an arithmetic unit, that interprets and executes instructions. (Adapted from ANSI X3.172.)

program: (1) A sequence of instructions suitable for processing. (Ref. ANSI X3.172.)

(2) To design, write, and test programs. (Ref. ANSI X3.172.)

(3) To enter data into a programmable read-only memory.

NOTE 1 Fixed programming is accomplished during manufacture of the memory, e.g., by using a mask.

NOTE 2 Field programming is accomplished after the manufacturing of the memory device is otherwise complete, e.g., by selectively blowing fuses.

NOTE 3 The programming of an electrically programmable read-only memory is accomplished by injecting electrons into the floating gates of selected cells.

program-erase cycle: The event of writing a memory cell from the programmed state to the erased state and back to the programmed state.

NOTE This event may be used as a unit of measurement for endurance. Within a sequence, program-erase cycles are indistinguishable from erase-program cycles.

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1 General terms and definitions (cont'd)

programmable logic array (PLA): An array of logic elements whose interconnection pattern can be programmed (usually mask-programmed, sometimes user-programmed) to perform specific logic functions.

NOTE The PLA is typically a large set of AND gates driving several OR gates.

programmable read-only memory (PROM): A field-programmable read-only memory that can have the data content of each memory cell altered only once.

pseudostatic (random-access) memory (PSRAM): A random-access memory whose internal structure is a dynamic memory with refresh control signals generated internally, in the standby mode, so that it can mimic the function of a static memory.

NOTE In practice, unlike so-called self-refresh DRAMs, PSRAMs have nonmultiplexed address lines and pinouts similar to those of SRAMs.

pushdown stack: Synonym for "pushdown storage".

pushdown storage: Storage in which data are ordered in such a way that the next data element to be retrieved is the most recently stored. (Ref. IEC 824.)

NOTE The method is "last-in, first-out".

quad word: A character string or binary element string that, in a given system, has four times the length of a word.

random-access memory (RAM): A memory that permits access to any of its address locations in any desired sequence with similar access time to each location. (Adapted from IEC 748-2.)

NOTE The term "random-access memory", as commonly used, denotes a read/write memory with unlimited data rewrite capability and similar read and write times.

read: To acquire or to interpret data from a storage device, from a data medium, or from another source. (Ref. ANSI X3.172.)

read disturb: The corruption of data caused by reading the memory.

read latency (for an SDRAM): The number of clock cycles occurring between the registration of a read command and the active clock transition coincident with the availability of the first resultant output data.

read-only memory (ROM): A memory in which the contents are intended to be read only and not to be altered during normal operation. (Ref. IEC 748-2.)

NOTE Unless otherwise qualified, the term "read-only memory" implies that the data content is determined by the structure of the memory and is unalterable.

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