

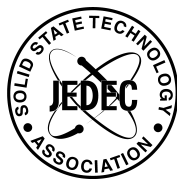
JEDEC STANDARD

Index of Terms and Abbreviations Defined in JEDEC Publications

JEP120-A (Revision of JEP120)

MAY 2000

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



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INDEX OF TERMS AND ABBREVIATIONS DEFINED IN JEDEC PUBLICATIONS

(Formulated under the cognizance of JC-10 Committee on Terms, Definitions, and Symbols.
The concept for this publication was approved under Council Ballot JCB-94-53.)

1 Purpose

This publication provides an index of terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

This publication should be used in conjunction with the latest issues of JEDEC Publication No. 104, *Reference Guide to Letter Symbols for Semiconductor Devices*, and ANSI/IEEE Std 100, *Dictionary of Electrical and Electronics Terms*.

2 How to use

For ease of use, terms are arranged in strict alphabetical order without regard to spaces or hyphenation; numerals are treated as if they were spelled out. Usually, terms are shown as they appear in the source document. An exception has been made for transistor and thyristor terms from JESD77. There, many terms are located by symbol rather than alphabetically and the same basic concept appears repeated with different adjectives. To reduce redundancy in this index, many terms taken from JESD77 are shown with the following adjectives removed:

ac, collector- base, collector- emitter, common-base, common-collector, common-drain, common-emitter, common-source, dc, emitter- base, large-signal, open-circuit, short-circuit, small-signal, static, etc.

After each term, the JEDEC publication and clause (section) or subclause (subsection) is shown where the definition, and, in many cases, the abbreviation or symbol for the term may be found.

Titles of all referenced documents are given in the back of this publication. When more than one reference is cited for a term, users are cautioned to use the proper referenced document for the definition to be applied for any specific device.

Note that definitions contained in an informative annex (appendix) are not a formal part of a standard but are included for information only.

Term	Document	Clause
A		
A.....	see acceleration factor	
A.....	see address inputs	
A or a.....	see anode terminal	
abbreviation	JESD77-B	1.1
abbreviation	JESD99-A	2.1.1
absolute accuracy error	JESD99-A	2.5.2.4
absolute maximum rating	JESD77-B	2.1
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acceleration factor (A)	JEP122	3
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access time	JESD100-B	2.2
ac controller	JESD14.....	3.1
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accumulator.....	JESD100-B	1
accuracy.....	EIA-557-A	A
accuracy.....	JEP132	B
accuracy, long-term.....	see instability, long-term	
ac terminal.....	JESD14.....	5.1
ac test	JESD12-1B	3
ac test	JESD99-A	1.2
activation energy.....	JEP122	3
active circuit element	see circuit element, active	
active component (of a hybrid integrated circuit)	see component, active (of a ...)	
active desiccant	J-STD-033	5
active device	JESD99-A	1.2
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active-pulldown output	JESD99-A	2.2.6
active-pullup output.....	JESD99-A	2.2.6
active substrate	see substrate, active	
actual time to fail	JESD61.....	4
ac unbalance voltage	JESD99-A	2.4.5
ac	see also "How to Use"	
ADC.....	see analog-to-digital converter	
A/D converter (ADC)	see analog-to-digital converter	
address	JESD100-B	1
address data input/output (ADQ)	JESD21-C.....	2.1.3
address inputs (A)	JESD21-C.....	2.1.2
address latch enable (AL)	JESD21-C.....	2.1.4
address register	JESD100-B	1
administrative problem	JESD671-A	5
ADQ	see address data input/output	
advance-information document.....	JEP103-A.....	–
affected customer.....	JESD48.....	3
AGC range	see automatic gain control range	
air ionizer	JESD625-A	4

Term	Document	Clause
AL.....	see address latch enable	
alignment mark.....	see registration mark	
“A” limit.....	JESD99-A.....	2.2.2
“A” limit high-level input voltage.....	see high-level input voltage, “A” limit	
“A” limit low-level input voltage.....	see low-level input voltage, “A” limit	
ALU.....	see arithmetic and logic unit	
ambient temperature.....	JESD61.....	4
ambient temperature.....	JESD77-B.....	2.2
ambient temperature.....	EIA-323.....	D (3)
A-mode.....	J-STD-035.....	2.1
analog gate.....	JESD99-A.....	2.5.1
analog integrated circuit.....	see integrated circuit, analog	
analog microcircuit.....	see microcircuit, analog	
analog resolution (of a linear or nonlinear ADC).....	see resolution, analog (of a ...)	
analog resolution (of a linear or nonlinear DAC).....	see resolution, analog (of a ...)	
analog settling time (of a DAC).....	see settling time, analog (of a ...)	
analog signal.....	see signal, analog	
analog-to-digital converter (ADC).....	JESD99-A.....	2.5.2.1
analog-to-digital processor.....	JESD99-A.....	2.5.2.1
analysis of variance.....	see anova	
analyst.....	JESD38.....	1.4a
angular luminous intensity.....	JESD77-B.....	5.3.2
anode.....	EIA-282-A.....	1.1
anode.....	JESD77-B.....	2.1
anode-cathode on-state voltage.....	JESD77-B.....	6.2.2
anode-cathode voltage.....	JESD77-B.....	6.1.1
anode current.....	JESD77-B.....	2.1
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anode-side junction-to-case thermal resistance.....	JESD77-B.....	6.1.2
anode-side (partial) junction-to-case thermal resistance.....	JESD77-B.....	6.1.2
anode terminal.....	EIA-282-A.....	1.1
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anode terminal (A, a).....	JESD77-B.....	2.1
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anode terminal (of a unidirectional triode thyristor) (A).....	JESD77-B.....	6.1.1
anode voltage (of a unidirectional diode thyristor).....	see anode-cathode voltage	
anode voltage (of a unidirectional triode thyristor).....	see anode-cathode voltage	
anova.....	JEP132.....	B
ANOVA.....	see variance components analysis	
antistatic material.....	JESD625-A.....	4
antistatic property.....	EIA-541.....	2.2.1
AOQ.....	see average outgoing quality	
apparent activation energy.....	JEP122.....	3
application-specific integrated circuit (ASIC).....	JESD99-A.....	1.2
approved customer agent.....	JESD48.....	3
approved supplier agent.....	JESD48.....	3
area (a).....	JEP119.....	4.10
arithmetic and logic unit (ALU).....	JESD100-B.....	1



Term	Document	Clause
arithmetic unit.....	JESD100-B	1
array density	JESD12-1B	4
array density (of a gate array)	JESD99-A	1.3
array, logic	JESD99-A	1.2
ART	see auto-load read transfer	
artificial intelligence.....	JEP132	B
artwork	JESD99-A	1.2
ASIC.....	see programmable application specific device	
ASIC.....	see application-specific integrated circuit	
assembly, microelectronic.....	JESD99-A	1.2
associative memory	JESD100-B	1
asymmetrical gate turn-off thyristor.....	see thyristor, (asymmetrical) gate turn-off	
asymmetrical reverse-blocking triode thyristor.....	see thyristor, reverse-blocking triode, asymmetrical	
asymmetry, full-scale (of a DAC with bipolar analog range)	JESD99-A	2.5.2.2
asynchronous circuit	JESD12-1B	3
asynchronous circuit	JESD99-A	1.2
ATTF	see actual time to fail	
attribute data	EIA-557-A	A
attribute memory select (RG)	JESD21-C.....	2.8.4
audit	EIA-554.....	3.3
audit	EIA-557-A	A
audit	JESD659-A	4.1
AUP	JEP130	2
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automatic gain control range (AGC range)	JESD99-A	2.4.2
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available gates	JESD12-1B	4
available gates (in a gate array).....	JESD99-A	1.3
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avalanche diode operating in the TRAPATT mode.....	see TRAPATT diode	
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average current.....	EIA-282-A	1.2
average current.....	JESD77-B	2.1
average dark current density	JESD99-A	2.7.5
average forward voltage.....	EIA-282-A	5.6.6.1
average noise factor	JESD77-B	2.2
average noise factor	JESD99-A	2.4.10
average noise figure	JESD77-B	2.2
average noise figure	JESD99-A	2.4.10



Term	Document	Clause
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average pulse duration	JESD77-B	2.2
average rectified output current	EIA-282-A	1.2
average rectified output current	JESD77-B	3.1.2
average reverse current.....	EIA-282-A	5.6.3.1
average voltage	EIA-282-A	1.2
average voltage	JESD77-B	2.1
AWT	see auto-load write transfer	
axial luminous intensity	JESD77-B	5.3.2
axis of measurement.....	JESD77-B	5.3.1
B		
B.....	see byte	
B or b.....	see base	
B or b.....	see base terminal	
b	see bit	
BA	see bank address	
Bxxx	JESD21-C	2.4.3
background charge	JESD99-A	2.7.2
back-side substrate view area	J-STD-035	2.3
back sputtering.....	see sputter cleaning	
backward diode.....	JESD77-B	3.3.1
backward traceability	JESD50.....	4.4
balanced amplifier	JESD99-A	2.4.1
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ball contact.....	see contact, bump	
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ball-grid array (BGA)	JESD95-1	14.2
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bandwidth, unity gain	JESD99-A	2.4.3
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base current	JESD77-B	4.1.2
base cutoff current	JESD77-B	4.1.2
base (of a package)	JESD99-A	1.2
base-1 peak voltage.....	JESD77-B	4.2.2
base plane	EIA-308-A	4.4
base plane	JESD95-1	4.2.1
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base region, functional	JESD77-B	4.1.1
base region, (physical).....	JESD77-B	4.1.1
base supply voltage	JESD77-B	4.1.2



Term	Document	Clause
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base terminal (B).....	JESD77-B	4.2.1
base	see also "How to Use"	
basic dimension	JESD95-1	2.2
battery voltage detect (BD)	JESD21-C	2.8.1
baud	JESD100-B	1
BBD	see bucket-brigade device	
BCxxx series	JESD54.....	2
BCCD	see bulk-channel charge-coupled device	
BCCD	see buried-channel charge-coupled device	
BCD	see bipolar-and-CMOS-and-DMOS	
BD	see battery voltage detect	
BDRAM	see burst DRAM	
beam lead	JESD99-A	1.2
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behavioral description	JESD99-A	1.3
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BiCMOS series.....	JESD55.....	2
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bidirectional thyristor surge protective device	JESD77-B	7.2.1
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binomial distribution	EIA-557-A	A
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bipolar-and-FET (BiFET) technology	JESD99-A	1.2
bipolar-and-MOS (BiMOS) technology.....	JESD99-A	1.2
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bipolar technology	JESD77-B	2.1

Term	Document	Clause
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bistable logic function.....	JESD99-A	2.3.1
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bit plane	JESD21-C	2.5.1
bit slice	JESD100-B	1
bit-slice processor	JESD100-B	1
bit wide	JESD21-C	2.5.2
bit-wide device	JESD100-B	1
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blackbody	JESD77-B	5.1.1
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"B" limit	JESD99-A	2.2.2
"B" limit high-level input voltage	see high-level input voltage, "B" limit	
"B" limit low-level input voltage.....	see low-level input voltage, "B" limit	
block.....	JESD100-B	1
blocking.....	EIA-282-A	1.2
blocking.....	JESD77-B	2.1
blocking period (of a rectifier circuit element)	EIA-282-A	1.3
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block write, no mask (BW)	JESD21-C	2.6.18
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bond, chip	JESD99-A	1.2
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bond shear	JESD22-B116	2.3
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bond, wedge.....	JESD99-A	1.2
bond, wire.....	JESD99-A	1.2
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Term	Document	Clause
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boundary scan	JESD99-A	1.2
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breakdown.....	JESD10.....	1.2
breakdown.....	JESD24.....	1.2
breakdown.....	JESD77-B	2.1
breakdown current	EIA-282-A	1.2
breakdown current	JESD77-B	2.1
breakdown current	JESD77-B	6.1.2
breakdown current	JESD77-B	7.1.2
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breakdown region.....	JESD10.....	1.2
breakdown region.....	JESD24.....	1.2
breakdown region.....	JESD77-B	2.1
breakdown region.....	JESD77-B	7.2.1
breakdown region (of a TSPD).....	JESD66.....	3.1.2
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breakdown voltage	EIA-282-A	1.2
breakdown voltage	JESD10.....	1.2
breakdown voltage	JESD24.....	1.2
breakdown voltage	JESD77-B	2.1
breakdown voltage	JESD77-B	3.1.2
breakdown voltage	JESD77-B	4.1.2
breakdown voltage	JESD77-B	4.3.2
breakdown voltage	JESD77-B	4.4.2
breakdown voltage	JESD77-B	7.1.2
breakdown voltage	JESD77-B	7.2.2
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breakover current.....	JESD77-B	7.2.2
breakover point	JESD77-B	6.1.1
breakover point	JESD77-B	7.2.1
breakover voltage	JESD77-B	6.1.2
breakover voltage	JESD77-B	7.2.2
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bridge rectifier circuit.....	EIA-282-A	1.3
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bucket-brigade device (BBD)	JESD99-A	2.7.1
buffer	JESD99-A	2.5.1
buffer	JESD100-B	1
buffered.....	JESD13-B	2.2
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buffer storage	JESD100-B	1
built-in electric field (in a transition region).....	JESD77-B	2.1
bulk-channel charge-coupled device (BCCD).....	JESD99-A	2.7.1



Term	Document	Clause
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burst DRAM (BDRAM)	JESD21-C.....	2.4.2
bus	JESD100-B	1
bus driver	JESD99-A.....	2.5.1
bus receiver	JESD99-A.....	2.5.1
busy (BY)	JESD21-C.....	2.1.9
busy signal	JESD100-B	1
BW	see block write, no mask	
BW	see bandwidth	
BWNM.....	see block write with new mask	
BWOM.....	see block write with old mask	
BY	see busy	
byte (B).....	JESD100-B	1
byte identifier (x)	JESD21-C.....	2.9.17
byte mode enable (BG)	JESD21-C.....	2.1.7
byte-wide	JESD21-C.....	2.5.3
byte-wide device	JESD100-B	1

C

C	see output clock	
C or c.....	see collector	
C or c.....	see collector terminal	
c	see accept number	
CA	see column address	
CA	see command/address	
cache memory.....	JESD100-B	1
CAM	see content-addressable memory	
capability	EIA-557-A	A
capability	EIA-599-A	4
capability	JEP132	B
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capability index	EIA-557-A	A
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carrier	J-STD-033	5

Term	Document	Clause
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CAS	see column enable	
case	JESD99-A	1.2
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case nonrupture current, peak	see peak case nonrupture current	
case nonrupture I2t value	JESD77-B	6.1.2
case temperature	JESD77-B	2.2
CAS latency	JESD100-B	1
catastrophic failure	JEP134	6
cathode	EIA-282-A	1.1
cathode	JESD77-B	2.1
cathode current	JESD77-B	2.1
cathode (of a current-regulator diode)	JESD77-B	3.5.1
cathode-side junction-to-case thermal resistance	JESD77-B	6.1.2
cathode-side (partial) junction-to-case thermal resistance	JESD77-B	6.1.2
cathode terminal	EIA-282-A	1.1
cathode terminal (K, k)	JESD77-B	6.2.1
cathode terminal (K, k)	JESD77-B	2.1
cathode terminal (of a unidirectional diode thyristor) (K)	JESD77-B	6.1.1
cathode terminal (of a unidirectional triode thyristor) (K)	JESD77-B	6.1.1
cause and effect diagram	EIA-557-A	A
cause and effect diagram	JEP132	B
caution label	JEP124	4.5
CBR	see internal refresh	
CC	see leaded chip carrier	
CC	see leadless chip carrier	
CC	see chip carrier	
CCD	see charge-coupled device	
CCLK	see command clock	
CCLK\	see command clock bar	
CD	see card detect	
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