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Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters

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GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS

(From JEDEC Council Ballot JCB-95-10 formulated under the cognizance of JC-15 Committee on Electrical and Thermal Characterization Techniques for Electronic Packages and Interconnects)

1 Scope

This measurement guideline is intended to describe the way to establish and prescribe the way to report the conditions in measurements of electrical parameters of individual leads in semiconductor packages, so that the results are reproducible from site to site.

This document describes the "standard test environment", a set of conditions semiconductor package test fixtures must meet so that they emulate the application environment for the semiconductor device.

The standard methodology is described for deriving lumped model inductance, mutual inductance, capacitance and lead to lead capacitance for semiconductor package leads. This guideline pertains to packages in which lead-to-lead spacing is relatively small as compared to lead-to-ground-plane spacing, as is the case in packages with leadframes, TAB packages and some ball grid array packages. This guideline does not attempt to cover semiconductor packages that contain internal power and ground planes, such as often found in ceramic multilayer packages. This guideline also does not deal with aspects related to measurement of internal distribution of inductances and capacitances in package leads; it only deals with methodology to measure integral parameter values. The methodology described in this document is restricted to lossless leads, where the assumption is that the energy loss in a lead caused by radiation ohmic resistance is negligible.

The measurement instrumentation is described in generic form, to enable wider range of instruments to be used with this guideline.

Several test procedures are suggested outside the standard methodology, where somewhat lower accuracy is obtained in return for a much simplified measuring procedure.

In conjunction with description of test environment, instrumentation, and measurement procedures, this measurement guideline prescribes the reporting of factors relevant in model parameter measurement, necessary to reproduce the measurement results from site to site.

2 Introduction

The characterization of model parameters for semiconductor package leads has been notorious for the lack of repeatability of modeling and of testing between sites. This lack of repeatability has been caused less by inaccuracy of basic test instrumentation, but more by lack of uniform conditions in test fixtures and by the diversity of methods applied. Thus, the intent for test methodology prescribed by this guideline is to ensure the reproducibility of uniform test conditions to be used at various test sites. As test conditions influence electrical parameter values, they must, to a large extent, emulate the application environment in which semiconductor devices are ultimately used.

3 Definitions

No new definitions are given in this document.

4 Standard test environment

4.1 General considerations

The values of all electrical parameters characterized by procedures described in this document depend on the electrical environment surrounding the package. This environment will typically change from application to application. This document will describe standard test environment for measurement of single lump electrical parameters, a configuration of the test apparatus which most closely approximates the typical electrical environment in existence at the time this document was written.

Specification of value of an electrical parameter will imply the assumption that the value in question was derived with the package immersed in the standard test environment. There could be circumstance when it is desirable to derive single lump electrical parameters in environments other than standard, such as in cases when a user's electrical environment is atypical and parameter values are desired in such environment. In such exceptional cases, specification of parameters values must be accompanied with the description of electrical environment in detail sufficient to reproduce parameter values to desired accuracy.

4.2 Standard test environment implementation

An instance of semiconductor package standard test environment is illustrated in figure 1A. The standard test environment comprises the package under test, positioned above a conductive metal plane (ground plane), so that the distance between the body of the package and the ground plane is the same as the distance between the package and the ground plane in a circuitboard this package would be mounted on in an application. Should the final application require a layer of dielectric material positioned between the ground plane and the package, equivalent dielectric material should be deployed in the test apparatus to reproduce such environment. Package leads that need to be connected to ground during the test are to contact the ground plane. There should be provisions to isolate leads from the ground plane either by virtue of depressions in the surface of the ground plane or by virtue of separation with a dielectric layer. The test signals are brought to the contact electrodes using controlled impedance transmission lines with constant characteristic impedance. A number of alternative ways to accomplish this is illustrated in figure 1B and figure 1C. The ground plane should be made from nonferromagnetic metal, such as brass or copper, sufficiently thick to overcome skin effect manifestations at frequencies of test signals used in the measurement process. For a lead over a ground plane, the measured inductance will increase when the skin depth exceeds the thickness of the metal comprising the ground plane. The skin depth is given by

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}}$$

where f is the frequency at which the skin depth is δ , μ is the magnetic permeability and σ is the conductivity of the ground plane metal. In case of copper, the skin depth will be 8.3 mm at 60 Hz, and 8.3 μm (or 0.00033 inch) at 60 Mhz. This indicates that ground planes implemented in conventional circuitboard technology will provide consistent measurements for frequencies of test signals exceeding 50 Mhz.

Outside the ground plane, there should be no conductive or ferromagnetic objects within the distance where they could significantly influence the results of measurements. The proximity of an electrically conductive plane (ground plane) will have significant influence on model parameter values for leads in some packages. The intent is for the standard test environment to facilitate generation of electrical model values which will faithfully simulate a packaged semiconductor device in an application. A typical application will have a conductive plane either at the surface the device is mounted on or within 0.2 to 0.5 mm within such surface.