

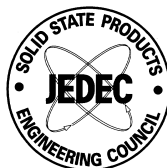
EIA/JEDEC PUBLICATION

Guide for Standard Probe Pad Sizes and Layouts for Wafer-Level Electrical Testing

EIA/JEP128

NOVEMBER 1996

**ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT**



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Published by

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Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201

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GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER-LEVEL ELECTRICAL TESTING

(From JEDEC Ballot JCB-96-27, formulated under the cognizance of JC14.2 Committee on Wafer-Level Reliability)

1 Scope

This guide applies to double- and single-column arrays of metal probe pads, on a semiconductor wafer or chip, that are electrically connected to one or more test structures.

The use of this guide will make necessary only two standard wafer-probe cards, one with a 1-by-16 and the other with a 2-by-16 standard array of probe tips to make contact with probe pads.

This guide is intended, in particular, to facilitate and expedite wafer-level electrical testing by laboratories participating in interlaboratory experiments conducted by JC-14.2 Committee.

This guide is intended, in general, to facilitate and expedite wafer-level electrical testing of test structures when using a wafer-probe card to make electrical contact to these structures.

The use of this guide will impose some restrictions on how test structures may be grouped within and near the area defined by the array of pads.

2 Introduction: significance and use

It is useful to have a standard for the size and layout of the probe pads of test structures that are to be electrically characterized or tested at the wafer level. Having such a standard design affords efficient and cost-effective use of wafer-probe stations because its widespread use leads to the need for a minimum number of probe cards and card changes to accommodate the various test structures that may need to be tested.

The use of a standard for the layout of probe pads is important for conducting interlaboratory experiments to evaluate or develop standard measurement methods that involve test-structure measurements or tests.

When a probe card required by a test structure is not readily available, manual probing is an option that presents significant potential for damage to the test structure. Damage to structures involved in interlaboratory experiments can lead to serious delays in the conduct and analysis of such experiments.