

EIA/JEDEC STANDARD

Thermal Test Chip Guideline (Wire Bond Type Chip)

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1 Introduction

(From JEDEC Council Ballot JCB-96-25 formulated under the cognizance of JC-15.1 Committee on Thermal Characterization).

1.1 Purpose

The purpose of this document is to provide a design guideline for thermal test chips used for integrated circuit (IC) package thermal characterization. The intent of this guideline is to minimize the differences in data gathered due to nonstandard test chips.

1.2 Scope

The thermal test chips described in this document will apply to single and multiple chip devices. These are designs using standard semiconductor wafer fabrication processes and can be used with a wide variety of industry standard packages. These test chips can operate in a static mode in which constant power is continuously supplied to the device while monitoring the temperature through the measurement of a Temperature Sensitive Parameter (TSP). They can also operate in a transient mode in which the power supply and the TSP are monitored as a function of time (t). This guideline covers test chips meant to be wire bonded to the package external leads.

1.3 Rationale

The thermal resistance for a specific device varies with many factors. The chip size, location and size of the power dissipation device(s), and location of the temperature sensor(s) will directly affect the thermal test results. It is essential to standardize thermal test chip design guideline in order to provide meaningful measurement results. This allows semiconductor suppliers to compare different packages over a wide variety of conditions, such as power levels and air flows. It will also help the users to estimate their active device junction temperature under actual operating conditions by allowing them to extrapolate the results of a defined standard condition.

1.4 References

This document contains the guideline for thermal test chip design as a subset of JEDEC methodology for component package thermal measurement. The associated details of test method, environment and test board are given in JEDEC documents [1] - [4]. It is also recommended to read the SEMI test standards ([5] - [9]) and the related documents [10] - [12].

[1] JESD 51

Methodology for the Thermal Measurement of Component Packages
(Single Semiconductor Device)

[2] JESD 51-1

Integrated Circuit Thermal Measurement Method - Electrical Test Method
(Refer to Annex A for a list of terminology and symbols applicable to this document).